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Modification of Schottky Barrier Properties of Ti/p-type InP Schottky Diode by Polyaniline (PANI) Organic Interlayer

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***Abstract*—The electrical properties of Ti/p-type InP Schottky diodes with and without polyaniline (PANI) interlayer was investigated using current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements. The barrier height of Ti/p-type InP Schottky diode with PANI interlayer was higher than that of the conventional Ti/p-type InP Schottky diode, implying that the organic interlayer influenced the space-charge region of the Ti/p-type InP Schottky junction. At higher voltages, the current transport was dominated by the trap free space-charge-limited current and trap-filled space-charge-limited current in Ti/p-type InP Schottky diode without and with PANI interlayer, respectively. The domination of trap filled space-charge-limited current in Ti/p-type InP Schottky diode with PANI interlayer could be associated with the traps originated from structural defects prevailing in organic PANI interlayer.**

***Index Terms*—Schottky diode, PANI, InP, barrier height, interface state density**

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I. INTRODUCTION

With the advancement in the semiconductor technology, Indium phosphide (InP) and its alloys have become more and more attractive semiconductor materials for the applications in high speed optoelectronic devices and high power microwave devices because of its direct bandgap and high mobility [1-3]. For instance, InP based Schottky devices are one of the most requisite elements for microwave circuits. Schottky diodes are the majority carrier devices that offer the advantage of faster reverse recovery without the minority-carrier stored charge which is observed in p-n rectifiers and p-i-n rectifiers. This property makes it particularly suited for applications in the high frequency area. Generally the performance and reliability of Schottky diodes are strongly influenced by the interface quality between the metal and semiconductor surface. Practically, most of the Schottky diodes are not intimate metal-semiconductor contacts; rather they boast a thin interfacial layer between the metal and semiconductor unless carefully fabricated. This interfacial layer between the metal and semiconductor results in a higher barrier height and ideality factor than those of intimate metal-semiconductor structure. Previously, it was reported that introduction of an organic film between the metal and inorganic semiconductor was effective in modifying the Schottky barrier properties [4, 5]. This modification is often attributed to the formation of a dipole layer between the semiconductor and the organic film even though the organic-inorganic interface appears abrupt

and unreactive [6, 7]. Until now, several attempts have been made to realize a modification and continuous control of the barrier height of InP-based Schottky devices using organic interlayer [8-12]. For instance, Gűllű. [8] fabricated the Al/n-InP Schottky diodes with deoxyribo nucleic acid (DNA) biopolymer as interlayer and demonstrated that the barrier heights could be tuned by varying the thickness of DNA biopolymer interlayer. Aydin et al. [10] reported that an increase in barrier height and ideality factor could be attributed to the modification of the Al/p-type InP interface by poly (3,4-ethylene dioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) interlayer. Reddy et al. [12] investigating the electrical properties of Au/poly(methyl methacrylate) (PMMA)/n-type InP Schottky structure at different annealing temperatures using *I–V* and *C–V* methods, showed that the interface state density and series resistance can give a significant effect on the electrical properties of the Au/PMMA/n-type InP Schottky diode. Among the various conducting polymers, polyaniline (PANI) has received greater attention due to its advantages over other conducting polymers such as the simplicity of its preparation from cheap materials, superior stability to air oxidation, and controllable electrical conductivity by doping [13-15]. Despite prominent features of PANI, however, its utilization as interlayer to improve the Schottky barrier properties of InP-based Schottky devices has not been explored yet, though the employment of PANI interlayer is expected to widen the range of their device applications. In this work, we fabricated Ti/p-type InP Schottky diode with PANI interlayer and investigated its electrical properties using current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics. The Ti has been used as a Schottky contact metal because of its improved adhesion to the semiconductor and its low work function that can provide high barrier heights for p-type semiconductors [3, 16]. It will be shown that the introduction of PANI interlayer in-between Ti film and InP substrate leads to an increase in barrier height and a decrease in interface state density. It will be further shown that at higher voltages, the carrier transport of Ti/p-type InP Schottky diode with PANI interlayer is governed by the trap-filled space-charge-limited current associated with the traps originated from structural defects prevailing in organic PANI interlayer.

II. EXPERIMENT

A schematic of the Ti/p-type InP Schottky diode with PANI interlayer is represented in the inset of Fig. 1. Zn doped p-type InP (100) wafers with a resistivity of 0.44 - 0.58 Ω·cm were used as a starting material. The wafers were initially degreased with organic solvents like trichloroethylene, acetone, and methanol by means of ultrasonic agitation for 5 min in each step, to remove the undesirable impurities, followed by rinsing in deionized (DI) water. Then, the samples were etched with HF (49%) and H_2O (1:10) to remove the native oxide from the substrate. The 50 nm-thick Pt film was sputter-deposited on the back side of the InP wafer as an Ohmic contact and then annealed at 350 °C for 1 min in N_2 atmosphere. PANI powder with a conductivity of 2 - 4 S/cm (purchased from Sigma Aldrich) was used in this work. Prior to the deposition of PANI films and Schottky electrodes, above surface cleaning and etching processes were performed again. For forming Schottky contacts, 20 nm-thick PANI and 40 nm-thick Ti films were sequentially evaporated on the cleaned front side of InP wafer through a metal shadow mask with an area of 500 × 500 μm^2. All evaporation processes were carried out under a vacuum pressure of 7×10^{-7} torr. In the present work, we fabricated the metal contacts using metal shadow masks very carefully in order to minimize the physical and chemical damages of PANI occurring during standard photolithography process and is feasible for the investigation of forward and reverse *I-V* characteristics [17, 18]. For comparison purposes, the conventional Ti/p-type InP Schottky diodes were fabricated under similar process conditions. The *I–V* and *C–V* measurements were performed at room temperature using precision semiconductor parameter analyzer (Agilent 4156C) and precision LCR meter (Agilent 4284A), respectively.

III. RESULTS AND DISCUSSION

Fig. 1 shows the *I–V* characteristics of Ti/p-type InP Schottky barrier diodes with and without PANI interlayer measured at room temperature. For both devices, the linear part of the semi-log *I–V* curve for the forward bias voltage range (- 0.1 ~ - 0.3 V) was clearly visible. This indicates that the carrier conduction of Ti/p-type InP

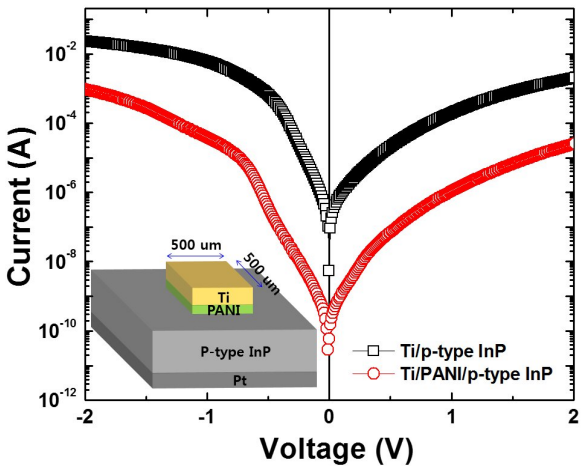

Fig. 1. *I–V* characteristics of Ti/p-type InP Schottky diodes with and without PANI interlayer. The inset shows the Schematic of Ti/p-type InP structure with PANI interlayer.

Schottky barrier diodes with and without PANI interlayer is limited by the thermionic emission regime. According to the thermionic emission theory, the current through Schottky contact is described by the following equation [19, 20]:

$$I = I_0 \exp\left(\frac{q(V - IR_S)}{nkT}\right)\left[1 - \exp\left(-\frac{q(V - IR_S)}{kT}\right)\right] \quad (1)$$

where V is the applied voltage across the junction, R_s is the series resistance, q is the charge of electron, n is the ideality factor, T is the room temperature, k is the Boltzmann constant and I_0 is the saturation current obtained from intercept of the plot of ln(I) versus V at V=0 and is given by [21, 22]:

$$I_0 = AA^{**}T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right) \quad (2)$$

A is the diode area, A^{**} is effective Richardson's constant equal to 60 $Acm^{-2}K^{-2}$ for p-type InP [10], and Φ_{b0} is the barrier height whose value is obtained from the value of I_0 using [19, 20]:

$$\Phi_{b0} = \frac{kT}{q}\ln\left(\frac{AA^{**}T^2}{I_0}\right) \quad (3)$$

The ideality factor can be determined from slope of the linear region of the forward bias ln(I) versus V using [19, 20]:

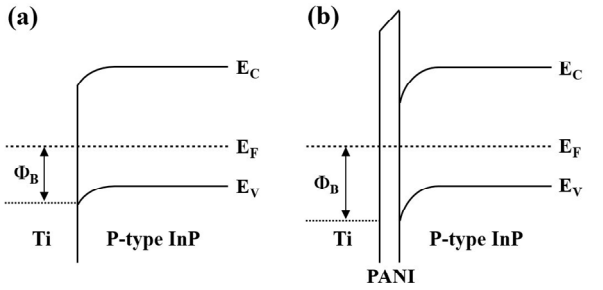

Fig. 2. Schematic energy band diagram of (a) Ti/p-type InP, (b) Ti/PANI/p-type InP structure.

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \quad (4)$$

The barrier heights extracted from the Ti/p-type InP Schottky diodes with and without PANI interlayer were determined to be 0.81 and 0.64 eV, respectively. Namely, the barrier height of Ti/PANI/p-type InP Schottky diode was higher than that of Ti/p-type InP Schottky diode. This indicates that the introduction of PANI interlayer influenced the interfacial potential barrier of the Ti/InP Schottky junction, resulting in a modification of the effective barrier height, as shown in Fig. 2 [6, 23, 24]. Namely, PANI interlayer can act as a physical barrier between Ti film and p-type InP substrate for preventing their direct contact, causing a substantial shift in the work function of a metal and in the electron affinity of a semiconductor. In particular, both devices exhibited an ideality factor deviating from the value of unity, of which values were 1.72 and 1.49 for Ti/p-type InP Schottky diodes with and without PANI interlayer, respectively. The ideality factor values were obtained in the range of 0.01 – 0.1 V. This deviation of the ideality factor from unity could be associated with the presence of a wide distribution of low-Schottky barrier patches caused by a laterally inhomogeneous barrier [25, 26]. Furthermore, when comparing to Ti/p-type InP Schottky diode, the higher value of the ideality factor in Ti/PANI/p-type InP Schottky diode could be attributed to secondary mechanisms such as interface dipoles caused by PANI interlayer, a specific interface structure or fabrication-induced defects at the interface [27, 28]. Additionally, the relatively high reverse leakage current was observed in Ti/p-type InP Schottky diodes with and without PANI interlayer. This could be a large number of native defects prevailing in InP substrate [29, 30]. Since these defects

are conductive, they can serve as the leakage path of current through Schottky junction. Therefore, irrespective of employing PANI interlayer, the both device showed high leakage current in the reverse bias region, resulting in their poor rectification behavior [31].

The forward bias *I–V* characteristics of the Schottky diodes deviated considerably from linearity at sufficiently large voltages due to the effect of series resistance and the presence of interface states. In order to accurately determine the series resistance and other Schottky parameters such as the barrier height and ideality factor, Cheung's functions were employed. Cheung's function can be expressed as [32]:

$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + IR_S \tag{5}$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^{**}T^2}\right) \tag{6}$$

Fig. 3 represents the plots of d*V*/d(ln*I*) versus *I* for Ti/p-type InP Schottky diode without and with PANI interlayer. A plot of d*V*/d(ln*I*) versus *I* is linear for the data in the nonlinear region of the forward bias *I–V* characteristics with the slope giving the series resistance and y-axis intercept yields the ideality factor following Eq. (5). From linear fit to data of Fig. 3, the series resistance and ideality factor were found to be 100 Ω and 2.32 for Ti/p-type InP Schottky diode, and 5.70 kΩ and 2.90 for Ti/PANI/p-type InP Schottky diode, respectively. The plots of H(*I*) versus *I* for Ti/p-type InP Schottky diode with and without PANI interlayer are shown in Fig. 4. Similar to the plot of d*V*/d(ln*I*) versus *I*, *H(I)* versus *I* linearly increased with increasing *I*. According to Eq. (6), a linear curve fitting of the data yields series resistance from the slope, and barrier height from the ordinate using the value of ideality factor obtained from Eq. (5). The series resistance and barrier height extracted from the plot of *H(I)* versus *I* plot were obtained as 109 Ω and 0.61 eV for Ti/p-type InP Schottky diode and as 6.0 KΩ and 0.77 eV for Ti/PANI/p-type InP Schottky diode. The values of series resistance calculated from the plots of d*V*/d*(lnI)* versus *I* were almost identical to those from the plots of *H(I)* versus *I*, implying the consistency of cheung's method. It should be noted that the series resistance of Ti/PANI/p-type InP Schottky diode was much higher than that of Ti/p-type InP Schottky diode.

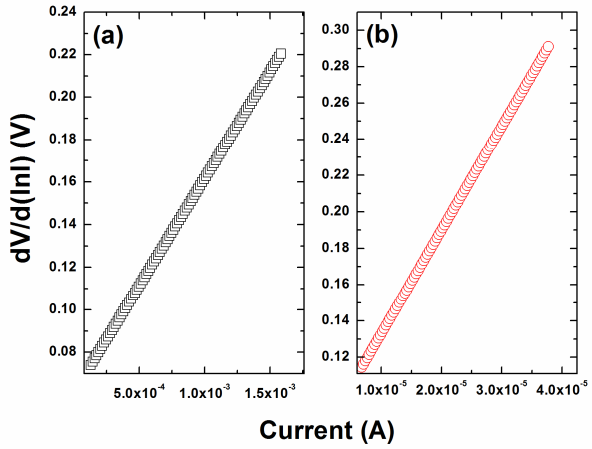

Fig. 3. Plots of d*V*/d(ln*I*) as a function of *I* taken from the (a) Ti/p-type InP, (b) Ti/PANI/p-type InP Schottky diodes.

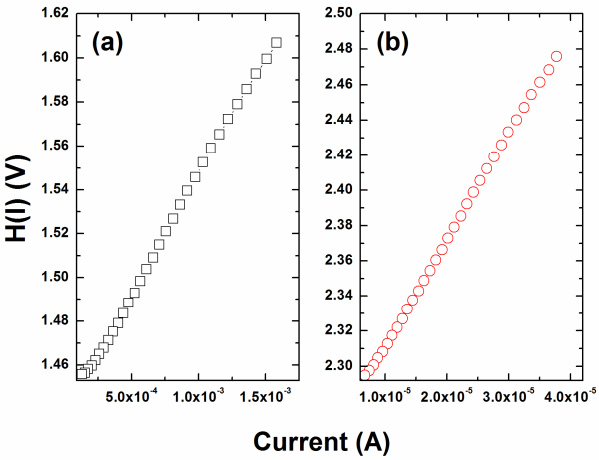

Fig. 4. Plots of H(*I*) as a function of *I* taken from the (a) Ti/p-type InP, (b) Ti/PANI/p-type InP Schottky diodes.

This indicates that the series resistance is a current limiting factor for the Ti/PANI/p-type InP Schottky diode. In other words the voltage drop across the PANI interlayer is likely to retain forward current conduction in the Ti/PANI/p-type InP Schottky diode.

Norde proposed an alternative method for the determination of barrier height and series resistance for the Schottky diode. The Norde function is defined as [33]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^{**}T^2}\right) \tag{7}$$

where γ is an integer greater than ideality factor. In this method, the function F(*V*) is plotted against the applied voltage and obtained it's minimum. The barrier height

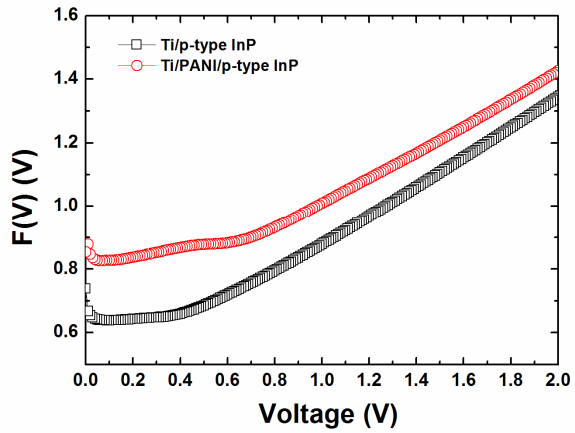

Fig. 5. Norde plot of Ti/p-type InP Schottky diodes with and without PANI interlayer.

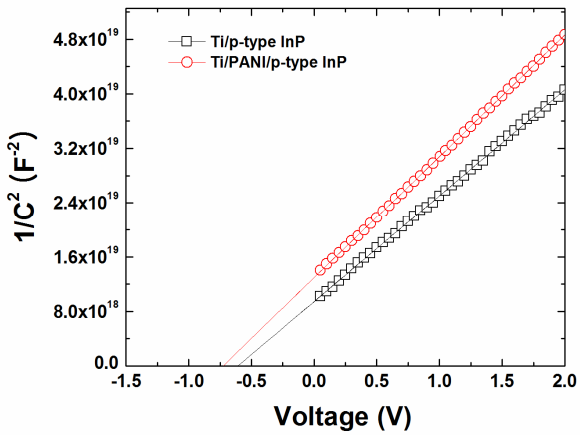

Fig. 6. Plot of $1/C^2$–V taken from Ti/p-type InP Schottky diodes with and without PANI interlayer.

can be determined using [33]:

$$\Phi_{b0} = F\left(V_{\min}\right) + \frac{V_{\min}}{\gamma} - \frac{kT}{q} \tag{8}$$

where $F(V_{\min})$ is the minimum point of $F(V)$ and $V_{\min}$ is the corresponding voltage. Fig. 5 shows the Norde plot for the Ti/p-type InP Schottky diode with and without PANI interlayer. The values of the series resistance can be estimated from Norde's function as [33, 34]:

$$R_S = \frac{kT\left(\gamma - n\right)}{qI_{\min}} \tag{9}$$

where $I_{\min}$ is the current corresponding to the voltage $V_{\min}$. The values of barrier height and series resistance were calculated to be 0.66 eV and 14 kΩ for Ti/p-type InP Schottky diode and 0.83 eV and 37 MΩ for Ti/PANI/p-type InP Schottky diode, respectively. There is a difference in the values of barrier height and series resistance obtained from the Norde method and forward bias ln(I)–V, Cheung's method. Such a difference in the values obtained from the three methods may be attributed to the extraction from the different regions of the I-V plot. Cheung functions are applied only to the nonlinear region in the high voltage section of the forward bias I–V characteristics, while Norde's functions are applied to full forward bias region of the I–V characteristics of the junction [25]. Further, the Norde method is not a suitable method for rectifying junctions with high ideality factors, which are not compatible with the pure thermionic emission theory. Hence, the values of the barrier height and series resistance obtained from Norde method are higher than those obtained from other methods.

Fig. 6 represents the room temperature $1/C^2$–V plot of the Ti/p-type InP Schottky barrier diode with and without the PANI interlayer. The C-V data were measured at a frequency of 1MHz. The straight lines obtained from the $1/C^2$–V plots are consistent with the Schottky-Mott model [35], which assumes that the carrier concentration is constant through the depletion width of the Schottky junction. The C–V relationship for a Schottky barrier diode is given as [19]:

$$\frac{1}{C^2} = \left(\frac{2}{\varepsilon_S q N_d A^2}\right)\left(V_{bi} - \frac{kT}{q} - V\right) \tag{10}$$

where V_{bi} is built-in potential. ε_s is the semiconductor permittivity of p-type InP ($12.5\varepsilon_o$, where ε_0 is the permittivity of the free space), A is the area of the Schottky barrier contact and q is the charge of electron, respectively. The x-intercept of the plot of $1/C^2$ versus V gives the diffusion potential (V_o). The V_o is related to V_{bi} by the equation $V_{bi} = V_o + kT/q$, where T is the absolute temperature. The barrier height can be obtained from the equation $\Phi_{b(C\text{-}V)} = V_{bi} + V_n$ where V_n is potential difference between the Fermi level and the top of the valance band of p-type InP which can be estimated by knowing the carrier concentration N_A and is obtained from the equation $V_n = (kT/q)\ln(N_V/N_A)$, where N_V is the density of effective states in the valance band of p-type InP given by $N_V = 2(2\pi m^* kT/h^2)^{3/2}$, where $m^* = 0.078\ m_o$ and its

value is $N_V = 1.11\times10^{19}$ cm^{-3} [3]. From $1/C^2$–V plots, the barrier heights were determined to be 0.86 and 0.99 eV for the Ti/p-type InP Schottky diodes without and with PANI interlayer. It is noted that the barrier heights obtained from the C–V measurements were higher than those obtained from the I–V method. The barrier heights obtained from the I–V and C–V methods are not always the same because of the different nature of the measurements. The difference between the barrier heights measured from I–V and C–V methods could be associated with the spatial inhomogeneity of the barrier heights having low and high Schottky barrier height patches along the interface [35]. Generally, in the I–V measurement, the current across the Schottky interface depends exponentially on the barrier height and thus is sensitive in the detailed barrier distribution at the interface. The current preferentially flows through the lower barrier height region, leading to an underestimation of the barrier height in the I–V method. While the C–V method yields the average barrier height of the whole diode [28]. Thus the barrier height obtained from the I–V method is significantly lower than the weighted arithmetic average of Schottky barrier heights obtained from the C–V method [36].

The downward concave curvature of the forward bias I–V characteristics at sufficiently large voltages has been attributed to the presence of the interface states (N_{ss}) which are in equilibrium with the semiconductor, apart from the effect of R_s [18]. In this region, the ideality factor n is rather controlled by the interface states and the series resistance. The energy distribution of the interface state density can thus be determined from forward bias I–V data by taking into account the bias dependence of the ideality factor and barrier height. The interface states refers to the imperfections at the semiconductor surface like dangling bonds at the surface, other types of defects and impurities unintentionally incorporated during the processing steps, or the unintentionally formed native oxide during the subsequent processing steps that may give rise to oxide trapped charges and interface trapped charges. The expression for the density of interface states (N_{ss}) proposed by Card and Rhoderick as [25]:

$$N_{SS} = \frac{1}{q}\left\{\frac{\varepsilon_i}{\delta}\left[n(V)-1\right]-\frac{\varepsilon_S}{w_D}\right\} \tag{11}$$

where W_D is the space charge width, ε_s is the permittivity of the semiconductor, ε_i is the permittivity of the interface layer, of which thickness is δ, and $n(V)=V/(kT/q)\ln(I/I_0)$ is the voltage dependent ideality factor. For, a p-type semiconductor, the energy of the interface state (E_{ss}) with respect to the top of the valance band (E_V) at the surface of the semiconductor is given by [25]:

$$E_{SS} - E_V = q\Phi_e - qV \tag{12}$$

where V is the applied voltage drop across the depletion layer and Φ_e is the effective barrier height given by [17]:

$$\Phi_e = \Phi_b + \beta V \tag{13}$$

where
$$\beta = \frac{d\Phi_e}{dV} = 1-\frac{1}{n(V)} \tag{14}$$

The energy distribution of the N_{ss} were determined from the forward bias I–V data (Fig. 1) using the voltage-dependent values of ideality factor and other parameters in Eq. (11). Fig. 7 shows the values of N_{ss} as a function of E_{ss} -E_V for the Ti/p-type InP Schottky diodes with and without PANI interlayer. The values of N_{ss} were varied in the range of 2.14×10^{13} eV^{-1} cm^{-2} in (0.62 - E_V) eV to 5.65×10^{14} eV^{-1} cm^{-2} in (0.32 - E_V) eV for the Ti/p-type InP Schottky diode and varied from 2.47×10^{11} in (0.75 - E_V) eV to 2.29×10^{13} eV^{-1} cm^{-2} in (0.39 - E_V) eV for the Ti/PANI/p-type InP Schottky diode. It can be observed that the N_{ss} decreased exponentially from midgap towards the top of the valence band. Further, at any specific energy, the N_{ss} of Ti/PANI/p-type InP Schottky diode was lower than that of the Ti/p-type InP Schottky diode. This indicates that the PANI interlayer was effective in the reduction of N_{ss} in the Schottky diode. It is well known that the insertion of an organic interlayer in-between the metal and semiconductor modifies the interface properties of the Schottky junction even though the organic/inorganic interface appears abrupt and unreactive [6, 7]. A decrease in the interface state density of the Ti/PANI/p-type InP structure could be responsible for an increase in barrier height and hence the reduction in the leakage current [37]. Generally, the presence of an interfacial thin layer separating the semiconductor and the metal causes the net charge of the gap states along with its image charge on the surface of the metal forming

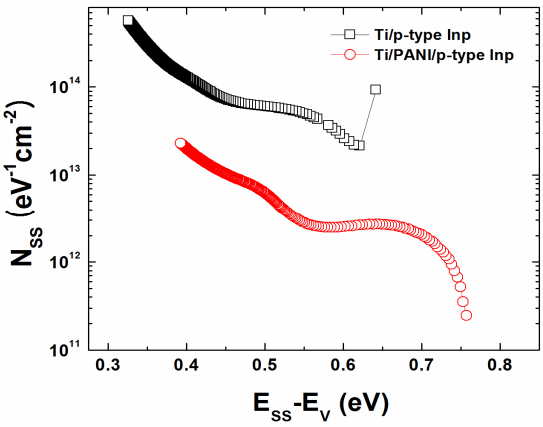

Fig. 7. Plots of N_{ss} as a function of E_c - E_{ss} extracted from the Ti/p-type InP Schottky diodes with and without PANI interlayer. N_{ss} was derived from forward *I*-*V* characteristics.

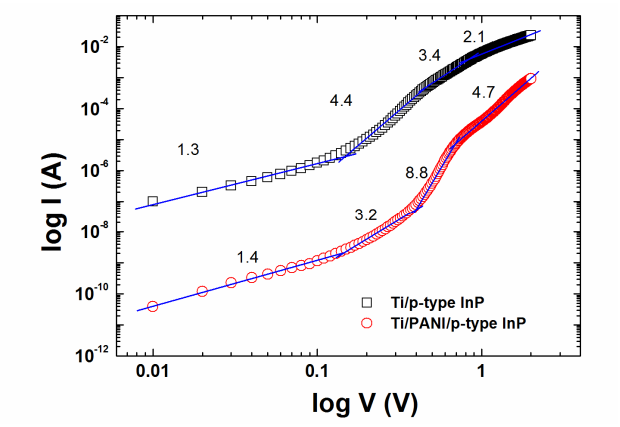

Fig. 8. Forward log *I* –log *V* characteristics of the Ti/p-type InP Schottky diodes with and without PANI interlayer.

a dipole layer that will alter the energy barrier, implying the strong dependency of the barrier height on the surface states density [38].

An investigation of the current transport mechanism through the Ti/p-type InP Schottky diodes with and without PANI interlayer was performed using the plot of log *I*–log *V* as shown in Fig. 8. In general, the log *I*–log *V* plot shows a power-law dependence of the current as $I \propto V^m$, and the value of the exponent *m* can be calculated from the slope of the linear fit to log *I*–log *V* plot. From Fig. 8, it can be observed that for both devices, there existed four different regions (indicated as region-I, region-II, region-III and region-IV) having different slopes. In region-I, the slopes were found to be 1.4 and 1.3 for the Ti/p-type InP Schottky diode with and without PANI interlayer, respectively. These values were close to unity, indicating a linear dependence of the current as $I \sim V$. In other word, for both devices, the current transport of region-I follows the Ohm's law in which the current is controlled by the thermally activated carriers rather the injected carriers [39]. For Ti/p-type InP Schottky diode without PANI interlayer, there was an exponential increase of current in region-II and region-III with the values of *m* being obtained as 4.4 and 3.4 in region-II and region-III, respectively. Such a power-law dependence ($m > 2$) indicates that the current transport mechanism could be attributed to space-charge-limited current controlled by the traps distributed exponentially in energy. At higher voltages (region-IV), the slope of Ti/p-type InP Schottky diode without PANI interlayer tended to decrease ($m = 2.1$). This implies that Ti/p-type InP Schottky diode without PANI interlayer approached the trap-filled limit regime at high injection level, where most of traps were occupied by injected carriers, followed by the creation of a field impeding further injection caused by the accumulation of space charge near the electrode. Namely, in higher voltage region (region-IV), Ti/p-type InP Schottky diode without PANI interlayer behaved as if there are no traps in it, and its carrier transport was governed by trap free space-charge-limited current, where current varies as the square of the voltage [40]. Similarly, Ti/p-type InP Schottky diode with PANI interlayer exhibited the power law relation having $m > 2$ in the region-II and region-III, which was indicative of the predomination of space-charge-limited current. However, unlike Ti/p-type InP Schottky diode without PANI interlayer, the slope in region-IV of Ti/p-type InP Schottky diode with PANI interlayer was much higher than 2 in spite of high injection level, implying that space-charge-limited current still predominated even at higher voltages. This is due to numerous traps originated from structural defects prevailing in organic PANI interlayer caused by its non-uniformity and sub atomic structure [41, 42].

IV. Conclusions

PANI interlayer was employed to modify the Schottky barrier properties of Ti/p-type InP Schottky diode. The barrier height of Ti/p-type InP Schottky diode with PANI interlayer was higher than that without PANI interlayer. This increase in barrier height could be attributed to the fact that the organic interlayer increased the effective

barrier height by influencing the space-region of InP. The introduction of the PANI interlayer led to the reduction of the interface state density in the Ti/p-type InP Schottky diode. The analysis of the forward log *I*–log *V* characteristics revealed that the domination of carrier transport by Ohmic conduction at lower voltage, controlled by the thermal activation of intrinsic carriers. At higher voltages, the carrier transport was governed by trap free space-charge-limited current in Ti/p-type InP Schottky diode. However, the carrier transport in Ti/p-type InP Schottky diode with PANI interlayer was dominated by the trap filled space-charge-limited current at higher voltages due to the traps originated from structural defects prevailing in organic PANI interlayer.

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