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Simulation Study on Silicon-Based Floating Body Synaptic Transistor with Short- and Long-Term Memory Functions and Its Spike Timing-Dependent Plasticity

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***Abstract*—In this work, a novel silicon (Si) based floating body synaptic transistor (SFST) is studied to mimic the transition from short-term memory to long-term one in the biological system. The structure of the proposed SFST is based on an n-type metal-oxide-semiconductor field-effect transistor (MOSFET) with floating body and charge storage layer which provide the functions of short- and long-term memories, respectively. It has very similar characteristics with those of the biological memory system in the sense that the transition between short- and long-term memories is performed by the repetitive learning. Spike timing-dependent plasticity (STDP) characteristics are closely investigated for the SFST device. It has been found from the simulation results that the connectivity between pre- and post-synaptic neurons has strong dependence on the relative spike timing among electrical signals. In addition, the neuromorphic system having direct connection between the SFST devices and neuron circuits are designed.**

***Index Terms*—Neuromorphic system, synaptic transistor, short- and long-term memory, spike timing-dependent plasticity (STDP)**

I. INTRODUCTION

Recently, there are great interests in realizing artificial synapses based on the Hebbian learning for the brain-like computing architectures [1-10]. This is because a synapse is believed to make a great contribution to many cognitive functions such as perception and memory in a biological system [11-16]. However, one of the strong candidates for artificial synapse, the memristor, is a two terminal device and needs extra selection components to interact with both pre- and post-synaptic neurons circuits [8-10]. Moreover, memristors are implemented by the non-silicon devices and have difficulty in being co-integrated with the conventional complementary metal-oxide-semiconductor (CMOS) architectures.

In this work, we propose a novel silicon (Si)-based floating body synaptic transistor (SFST) that has both short- and long-term memory capabilities in a single device due to two separated gates as illustrated by Fig. 1(a). Each gate is used to make the short- and long-term memories respectively. The short- and long-term memories are mimicked through the floating body effect and hot carrier injection. The transition from short-term memory to long-term memory can be conducted through repetitive applying of input pulses. It is also demonstrated that the STDP behaviours are successfully

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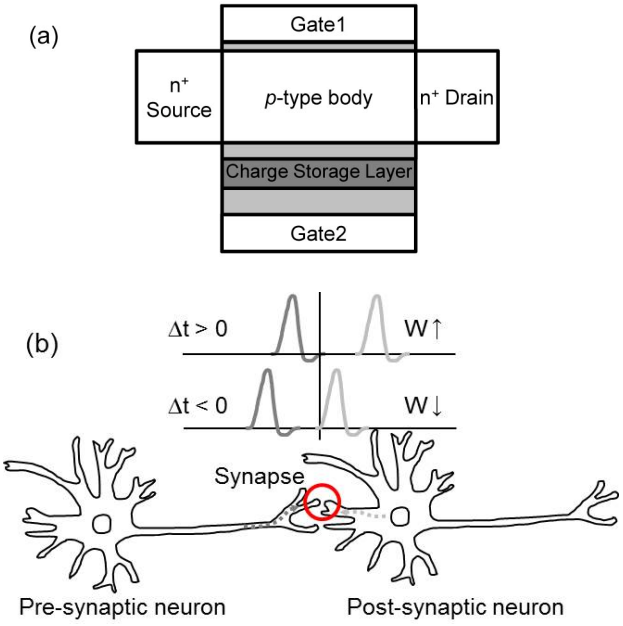

Fig. 1. Schematic view illustrating (a) the proposed Si-based synaptic transistor, (b) how the biological synaptic weight is changed by timing difference of pre- and post-synaptic spikes.

realized by the proposed SFST device. On top of that, the SFST has the strong merit as it can directly receive backpropagation signal from post-synaptic neuron circuit without any additional switching components.

Fig. 1(b) shows the STDP action in the biological system, where the synaptic weight (W) is changed depending on the relative timing difference between pre- and post-synaptic spikes with backpropagation in the biological system [17-19]. In a similar way, the conductivity of the proposed device should be strengthened or weakened according to the relative input spike timing.

II. Fabrication and Device Design

The fabrication process flow of the device with independent two gates is shown in the Fig. 2. The hard mask stack was deposited and active patterns etched. The 1st gate (G1) stack was formed where the active region was etched through dry oxidation and the deposition of doped poly-Si and 50 nm medium temperature oxide (MTO) sidewall spacer made after deposition and dry etch process. Then a silicon fin was formed using dry etch process. The fin width was controlled by the thickness of MTO and thin fin needed for floating body effect which provides the device with short-term memory

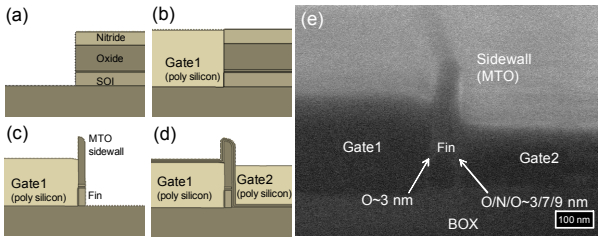

Fig. 2. Critical fabrication steps of proposed device and cross-sectional SEM image (a) Hard mask stack was deposited and etched, (b) G1 formation by CMP process, (c) Fin formation using MTO sidewall spacer, (d) G2 formation through CMP and etch-back process, (e) Cross-sectional SEM image after separating two gates successfully.

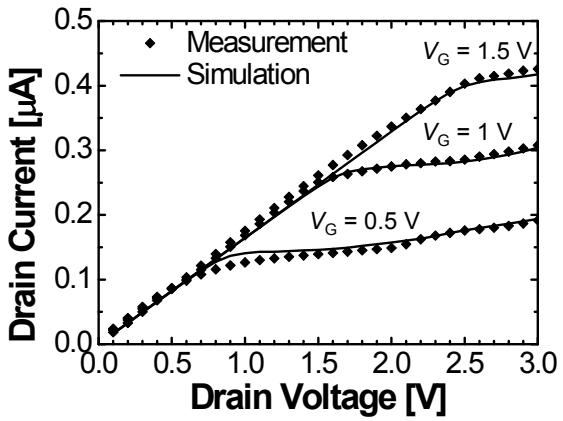

Fig. 3. Comparison of measured and simulated output characteristics.

capability. Then the second gate (G2) stack comprised of oxide / nitride / oxide / doped poly-silicon was deposited over the fin and the G1. The charge storage layer makes the device have the long-term memory capability. Two gates were separated through chemical-mechanical planarization (CMP) and etch-back process. Fig. 2(e) shows that these two gates were successfully separated by following above mentioned process steps. The fabrication details were described elsewhere [20].

A 2-dimensional (2-D) technology computer-aided design (TCAD) simulation tool was used to demonstrate that the learning mechanism of the biological system was realized by the SFST [21]. The long-term memory capability is realized by the charge storage layer and G2 placed on the other side of G1 across the channel of a floating body. Consequently, the simulated device structure appeared to be a double-gate transistor with 50 nm body thickness and 3 nm gate oxide thickness as same as the experimental conditions. N^+ peak doping concentration was As 1×10^{21} cm^{-3} (Gaussian distribution)

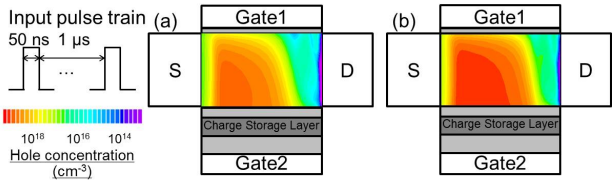

Fig. 4. Simulated hole concentration in the body region after (a) the first input pulse, (b) the sixth input pulse.

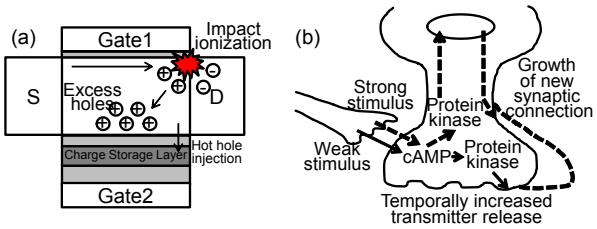

Fig. 5. Schematic views of how short- and long-term memories are formed in (a) the SFST, (b) a biological synapse.

at source/drain regions and the silicon body was doped with B 1×10^{18} cm^{-3}. Multiple models were included in each simulation, such as Shockley-Read-Hall generation and recombination model, Selberherr's impact ionization model [22], and the hot carrier injection model based on Tam's equation [23]. Especially, impact ionization and mobility parameters were experimentally calibrated for more accurate electrical estimation in the simulations results. Fig. 3 shows an overlay of the measured output characteristics and simulated ones under the same conditions. It is well-fitted and gives a guarantee of the accuracy of following simulation results.

III. Simulation Study on Synaptic Learning Mechanism

In the designed device structure and under the given process conditions, it has been verified that the transition from short-term memory to long-term memory occurs when input pulses with a time width of 50 ns and a repetition interval (T_i) of 1 μs were applied. This is not the unique solution but one of the possible time-dependent input schemes leading to the transition. The bias conditions for the memory transition were $V_{G1} = V_D = 2$ V, and $V_{G2} = -2$ V (here, V_{G1}: the 1st gate voltage, V_D: drain voltage, and V_{G2}: the 2nd gate voltage). When input pulses are fed to the device only a few times, the operation of the SFST can be approximated to that of the floating body [24-26]. Fig. 4 shows that excess holes were generated by impact ionization and accumulated near the G2. The accumulation of holes resulted in the increase of the conductivity for a short time since these impact-generated holes increased the potential of the floating body, which corresponds to the short-term potentiation of a biological synapse [12, 14].

As the pulsing was repeated many times, however, the operation mode of the SFST changed significantly. The accumulated hole density rose as the number of input pulses (N) increased since the repetition interval was too short enough for the generated holes to be fully recombined with electrons. Fig. 4 shows that the hole concentration in the floating body region was rapidly increased as N increased. The hole concentration after the sixth input pulse was much higher than after the first input pulse. This results in the fact that the body potential is increased by the accumulated holes with the input pulses, hence increasing the output current, I_D, of the SFST. At the moment when the source-to-body junction is forward-biased due to the accumulated holes, the impact ionization occurs near the back-side gate with higher probability, and the generated hot holes begin to enter the charge storage layer over the energy barrier of gate dielectric near the drain end.

After this event, the SFST is operated like a programmed flash memory cell having charges trapped in the charge storage layer ($Q_{trapped}$), which emulates the biological function of transition from short-term memory to long-term memory in a synapse as shown in Fig. 5 [12, 14]. The excess holes can be compared to the temporally increased cAMP in a biological system because both of them decay without the next input or serotonin and the long-term memory arises when the accumulation of both of them exceeds threshold points. Also, the hot hole injection to the charge storage layer corresponds with the growth of a biological synapse because they bring out the long-term increase in channel conductance and biological synaptic weight, respectively.

Fig. 6(a) shows that the hot hole injection into the charge storage layer starts from the seventh input signal pulsing. It is noteworthy that the transition in the device occurs without any change in the bias condition. It depended on the timing scheme only. Fig. 6(b) shows the retention of stored information with N under the read bias condition. The data reading was conducted at $V_D = 0.1$ V which is assumed to be small enough to minimize the interruption of the device field and carrier distributions.

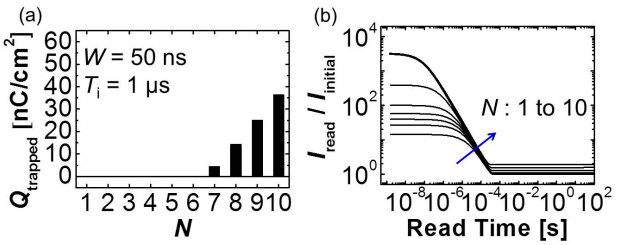

Fig. 6. SFST device operation (a) Simulated trapped charges in the charge storage layer as a function of N, (b) read retention characteristics according to the number of the applied pulses with T_i of 1 μs.

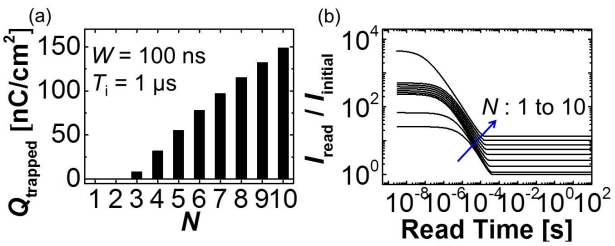

Fig. 7. Simulated learning characteristics with pulse width of 100 ns (a) trapped charges, (b) read retention characteristics.

In Fig. 6(b), $I_{read}/I_{initial}$ is defined as the ratio between the learned state where hot carriers are injected to the charge storage layer and the initial state where there is no carrier injection. When the number of input pulses (N) was no more than 7, the information was lost in several milliseconds. On the other hand, if N was increased above 7, long-term memory was formed and the stored information remained for more than 100 seconds. The flat tails of the upper four curves (N = 7~10) indicate that the information was stored into a long-term memory.

In order to examine the effect of input pulses on the synaptic learning, input pulses with longer width of 100 ns and the same T_i of 1 μs were applied to the SFST at first. The transition to long-term memory occurred at the third input signal pulsing as shown in Fig. 7(a) and (b). It is earlier than when the pulse width is 50 ns. Understandably, this comes from the fact that more excess holes are generated in a single pulse with longer width compared with shorter one.

In addition, the time response of the SFST to different T_i was also studied in depth. For an input with a shorter interval (T_i = 0.1 μs), the transition needed fewer number of input pulses than when T_i = 1 μs as shown in Fig. 8(a). This is because the next input for the shorter interval is applied to the SFST while more excess holes are remaining in the floating body. Moreover, for an input

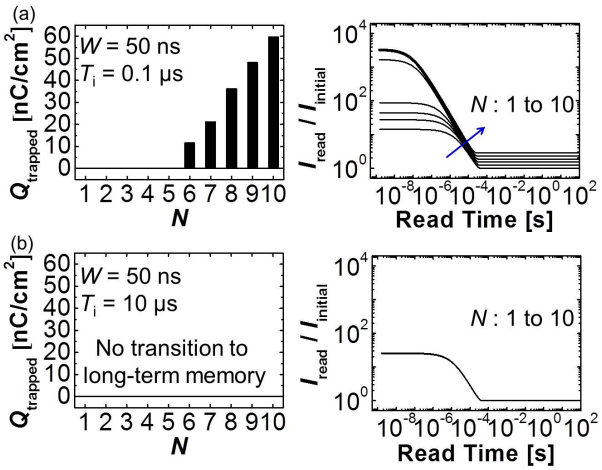

Fig. 8. Simulated learning operations of the SFST according to the number of the applied pulses with T_i of (a) 0.1 μs, (b) 10 μs.

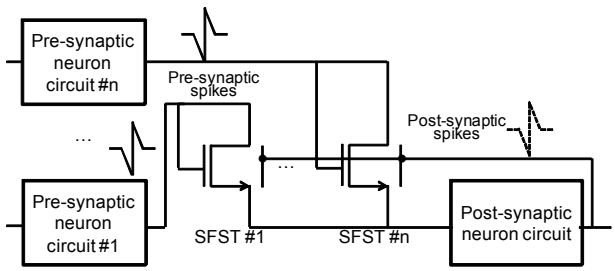

Fig. 9. Simple circuit diagram of the neural network.

with a longer interval (T_i = 10 μs), hole injection did not occur in spite of the increased N as shown in Fig. 8(b). Furthermore, there was no transition from short-term memory to long-term memory because the hole concentration in the floating body decreases back to the initial value during the increased time interval between pulses, which obviously realizes time-dependent synaptic learning of the biological system through an electronic system.

IV. Connection with Pre- and Post-synaptic Neuron Circuits and Spike Timing-Dependent Plasticity Characteristics

The neuromorphic system composed of the proposed devices and neuron circuits was designed as shown in Fig. 9. The pre-synaptic spikes are applied to V_{G1} and V_D of the SFST devices and the post-synaptic spikes are applied to V_{G2} of the SFST devices. The best part of this design is the fact that the SFST devices are able to

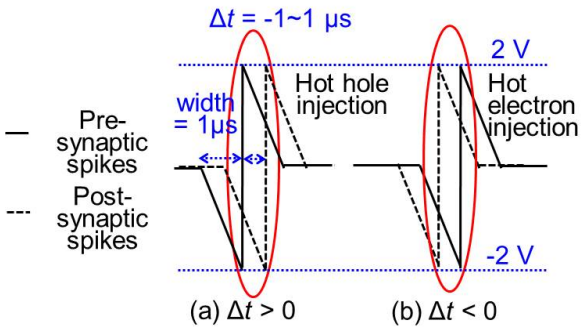

Fig. 10. Timing diagrams of biasing scheme to mimic pre- and post-synaptic spikes with (a) positive, (b) negative Δt.

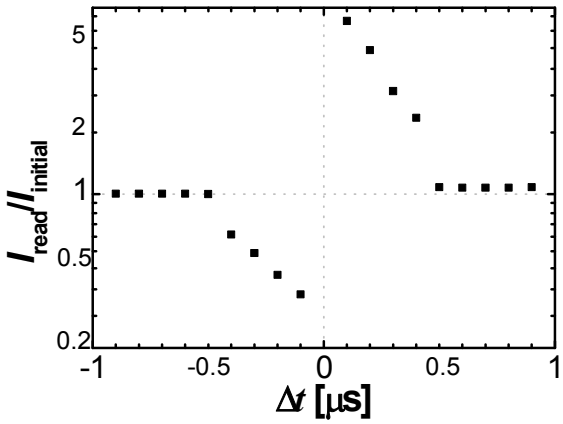

Fig. 11. Simulated STDP characteristics of the SFST after 10 triangular spikes. The direction of the synaptic change is determined only by Δt.

interact with both pre- and post-synaptic neuron circuits directly. It is much simpler compared with neuromorphic system using the memristor as a synaptic device. This is because the memristor is a two-terminal device and requires enormous switching component to receive signals from post-synaptic neuron circuits [8-10].

STDP characteristics were emulated with time difference (Δt) between pre- and post-synaptic spikes. Spikes with T_i of 1 μs and duration of 0.5 μs were applied to the device ten times. In case of positive Δt, hot hole injection occurs by the same mechanism explained previously since negative V_{G2} is applied while impact ionization rate is high due to large V_D as shown in Fig. 10(a). However, hot electrons generated by the impact ionization begin to enter the charge storage layer with a negative Δt because V_{G2} is positive while large V_D is applied as shown in Fig. 10(b). This is analogous to the depression process in the biological systems. It is noticeable that these contrasting results are obtained by nothing but the spike timing scheme.

Fig. 11 depicts the conductivity of the channel after 10 spikes as a function of Δt. It is confirmed that the obtained STDP characteristics bear great deal of resemblance with those of the biological synapses [15, 16]. Regardless of the polarity of Δt, smaller $|\Delta t|$ substantially increases potential difference between drain and G2, which results in the increase of hot carrier injection rate. For this reason, the $I_{read}/I_{initial}$ shows a large deviation from the unity near $\Delta t = 0$ in Fig. 10.

V. CONCLUSIONS

In this study, a novel Si electronic device realizing the most fundamental synaptic functions of learning and inference in the biological system has been proposed with a proper set of operation schemes. Floating body effect and hot carrier injection have been used to implement the short- and long-term memories and transition between them with a single Si transistor. The learning process realized by the SFST device was dependent on the frequency of input pulse, in a very similar manner how the real synapse works. By employing an appropriate biasing and timing schemes, STDP characteristics have been successfully emulated by the SFST device. Furthermore, the SFST devices are able to be directly connected with both pre- and post-synaptic neurons circuits owing to two separated gates.

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