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VCO Design using NAND Gate for Low Power Application

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Abstract—**Voltage controlled oscillator (VCO) is widely used circuit component in high-performance microprocessors and modern communication systems as a frequency source. In present work, VCO designs using the different combination of NAND gates with three transistors and CMOS inverter are reported. Three, five and seven stages ring VCO circuits are designed. Coarse and fine tuning have been done using two different supply sources. The frequency with coarse tuning varies from 3.31 GHz to 5.60 GHz in three stages, 1.77 GHz to 3.26 GHz in five stages and 1.27 GHz to 2.32 GHz in seven stages VCO respectively. Moreover, for fine tuning frequency varies from 3.70 GHz to 3.94 GHz in three stages, 2.04 GHz to 2.18 GHz in five stages and 1.43 GHz to 1.58 GHz in seven stages VCO respectively. Results of power consumption and phase noise for the VCO circuits are also been reported. Results of proposed VCO circuits have been compared with previously reported circuits and present circuit approach show significant improvement.**

Index Terms—**CMOS, delay stage, noise, nand gate, power consumption**

I. INTRODUCTION

Phase locked loops (PLLs) are the commonly used circuit component in modern communication and high speed RF circuits. These circuits have extensive application in frequency synthesis, clock and data recovery [1, 2]. VCO (voltage controlled oscillator) is the important building block PLL circuit. The most vital requirements for VCO are small phase noise and a large output frequency range. Other main considerations are low cost, simplicity of integration and higher packaging density. Further, low power and small phase noise oscillators are the essential part in variety of application like radar and wireless communication systems. The performance of VCO significantly affects the execution of telecommunication or data transmission network. Data rates are escalating at very fast speed with each generation of integrated circuit and communication technology. In recent years low power consumption and high output frequency range have become the crucial performance parameter for VCO circuit design. There are two elementary types of VCO configuration: one is ring based and the other is inductor-capacitor (LC) based VCO. LC tank based VCO are used in many communication applications due to simplicity of achieving highest frequency and little phase noise. Precise fabrication techniques are required in order to obtain the high quality factors (Q) of inductors and varactor in inductor capacitor based oscillators. Further, inductor and capacitor combination on integrated circuits is responsible for more layout area which further reduces the packaging density [3-5]. On the other side, CMOS ring oscillators circuits are more suitable because of high output frequency, lesser power consumption and having no prerequisite of chip inductors [6, 7]. In ring based VCO circuits design output of the final delay cell is given as feedback to input of first delay stage. Block diagram of VCO with single ended delay stages is shown in Fig. 1.

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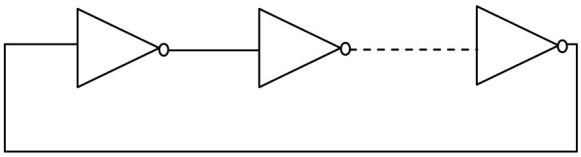


Fig. 1. VCO having single ended delay stages.

A phase change of 2π and unity voltage gain is provided by inverter delay cells linked in ring topology. Each delay cell offers a phase shift of π/N, where N is total number of delay stages. Remaining π phase shift is provided by the dc inversion of the inverter. The odd numbers of delay stages have been used for dc inversion. Frequency of oscillation of VCO is given by $f_o = \frac{1}{2N t_d}$, here 'N' is the total number of delay stages in the ring path and t_d is delay of each cell [8-10].

Many delay cell designs are reported in literature for VCO design including multiple-feedback loops, dual-delay paths and single ended delays [11-19]. Performance of these delay cells largely affects the performance of VCO circuit. Low power consumption, minimum chip area, low noise, high output frequency and ease of tuning are the demanding design parameters in VCO circuit design [20-25]. Further, higher level of integration and lesser power consumption makes the CMOS based ring oscillators a better candidate for on chip systems. The rising demands of transportable devices have further added the research efforts towards low power circuit designs. Power consumption in CMOS based circuit is separated as: dynamic, static power and leakage power. Dynamic power comprise the power dissipated during the switching or clock event, whenever a node voltage of gate makes a logic transition from low to high level or high to low level. In CMOS circuits, both NMOS and PMOS transistor may on simultaneously for a small time of switching time thus form a straight current path between the power supply and ground terminal. This current does not add to charging of node capacitances in the circuit and this current is responsible for short circuit power dissipation. In CMOS VLSI circuits leakage current also add to overall power consumption even when the transistor are not doing any switching event. The power dissipation in any VLSI system due to the above three sources can be managed at different levels of the general design process. Circuit level design methodologies greatly affect the total power dissipation of CMOS circuits. In present work power consumption of CMOS ring based VCOs have been reduced at circuit level. New VCO circuits have been designed using combination of three transistor NAND gate and a CMOS inverter. Efforts have been made to decrease the power consumption with high output frequency.

The paper is structured as: in section II, delay cells with three transistors NAND and CMOS inverter have been reported. Further, design of three, five and seven stages voltage controlled oscillators circuits have been reported in this section. In section III results of proposed circuits have been described and compared with the earlier reported circuits. Finally, Section IV concludes the work.

II. CIRCUIT DESCRIPTION

Combination of three transistor NAND gates and CMOS inverter has been employed for designing the new VCO circuits. A three transistor NAND gates as shown in Fig. 2(a) have been used as inverter. Delay stage having NAND gate comprises of two PMOS transistors and one NMOS transistor. One of NAND gate terminal is connected to logic 1 (high level) and feedback signal is applied to other terminal so NAND gate works as an inverter circuit without having direct path between ground terminal and supply terminal (V_{dd}). The circuits are designed in 0.18 μm CMOS technology. The gate lengths (L_n & L_p) of all NMOS and PMOS transistors is taken as 0.18 μm. Width (W_n) of NMOS transistor (N1) is taken 0.25 μm. Width (W_p) of transistors P1 and P2 are taken as 1.25 μm. Further for CMOS inverter section width of PMOS (W_p) and NMOS (W_n) are taken as 1.0 μm and 0.5 μm respectively. Fig. 2(b) shows the output waveform of NAND gates and adequate level has been achieved.

The output frequency of VCO has been controlled through the two different ways. In first method voltage source V_1 is connected to one input of NAND and has been varied from 0.9 V to 1.6 V. This varying voltage is controlling the coarse tuning of VCO. Further, in second methodology the V_{dd} supply has been varied from 1.5 V to 2.2 V. This varying voltage controls the fine tuning of VCO. A 3-stage VCO as shown in Fig. 3(a) comprise of

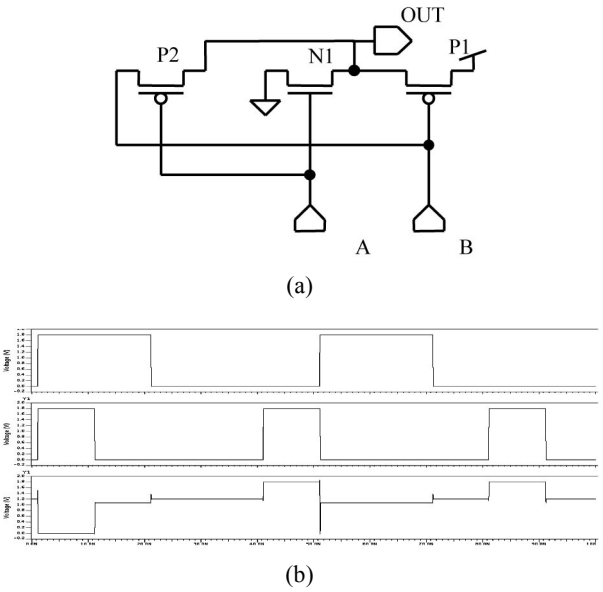


Fig. 2. (a) NAND gate circuit, (b) output waveform.

two NAND gate and a CMOS inverter delay cell. A 5-stage VCO as shown in Fig. 3(b) have been designed with four NAND delay cells and one CMOS inverter cell. A seven stage VCO has been designed with six stages of NAND and one CMOS inverter shown in Fig. 3(c). Different odd combinations of these delay stage may be used as per the need of the VCO output frequency range. Straight path between supply and ground has been eliminated in VCO designs as a result of which leakage power is reduced and the VCO designs shows power saving. Proposed VCO circuits are more power proficient and require less area as compared to usual NOR, NAND, XOR and XNOR gate circuits.

III. RESULTS AND DISCUSSIONS

Results have been taken in TSMC 0.18µm CMOS

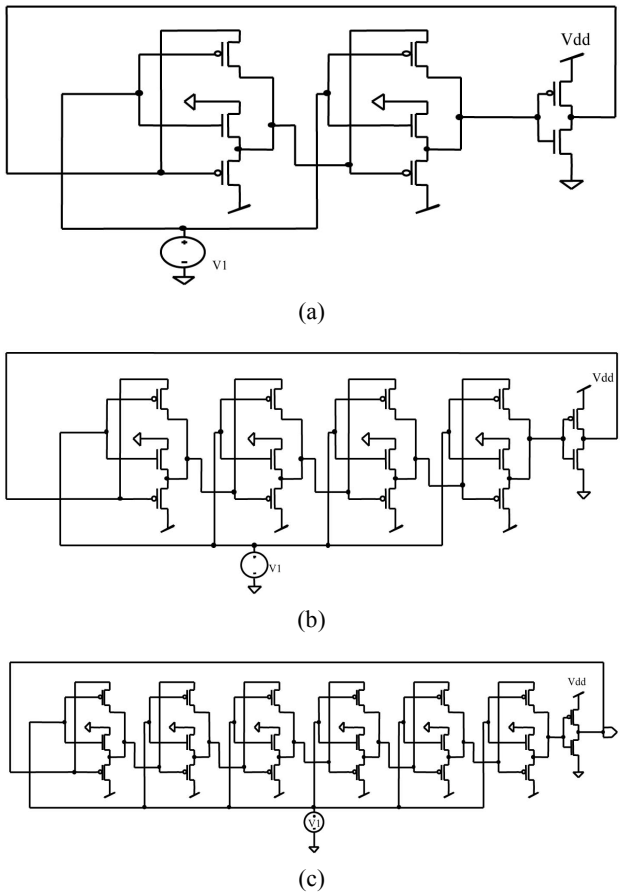


Fig. 3. (a) 3-stage, (b) 5-stage, (c) 7-stage VCO.

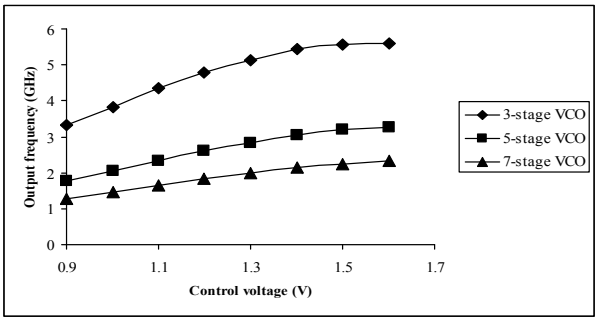
technology. Table 1 is showing the results of 3, 5 and 7 stages VCOs with coarse tuning by altering the voltage of V1 source. Fig. 4(a) and (b) shows frequency and power consumption deviation for three, five and seven stages VCO circuits. Fig. 5 is showing the output waveforms of 3, 5 and 7-stages VCOs with control voltage of 1.5 V. Table 2 illustrates the results of 3, 5 and 7-stages VCO with fine tuning by varying the V_{dd} from 1.5 V to 2.2 V. Fig. 6(a) and (b) shows frequency and

Table 1. VCO frequency and power consumption with coarse tuning

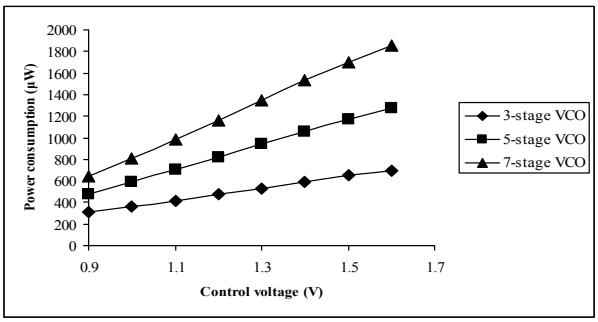
Control Voltage (V)	3-stage VCO		5-stage VCO		7-stage VCO	
	Frequency (GHz)	Power (µW)	Frequency (GHz)	Power (µW)	Frequency (GHz)	Power (µW)
0.9	3.31	310.75	1.77	477.91	1.27	644.95
1.0	3.81	361.98	2.06	585.67	1.46	809.28
1.1	4.33	416.58	2.34	699.57	1.64	982.54
1.2	4.77	473.82	2.59	818.12	1.83	1162.40
1.3	5.13	532.86	2.84	939.39	1.99	1346
1.4	5.42	592.32	3.04	1060.40	2.13	1528.60
1.5	5.56	649.33	3.19	1175.40	2.25	1701.60
1.6	5.60	689.70	3.26	1276.30	2.32	1853.30

Table 2. VCO frequency and power variation with fine tuning

Control Voltage (V)	3-stage VCO		5-stage VCO		7-stage VCO	
	Frequency (GHz)	Power (μW)	Frequency (GHz)	Power (μW)	Frequency (GHz)	Power (μW)
1.5	3.70	226.75	2.04	403.21	1.43	579.72
1.6	3.79	267.20	2.05	459.34	1.45	651.50
1.7	3.79	312.25	2.06	520.10	1.44	727.90
1.8	3.81	361.98	2.06	585.67	1.46	809.28
1.9	3.84	416.40	2.10	656.15	1.48	895.79
2.0	3.87	475.48	2.11	731.57	1.53	987.49
2.1	3.90	539.19	2.15	811.89	1.56	1084.40
2.2	3.94	607.47	2.18	897.09	1.58	1186.50



(a)



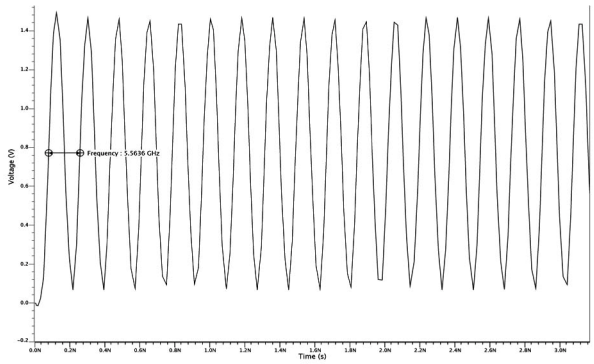
(b)

Fig. 4. (a) Frequency, (b) power variations with coarse tuning.

power deviation for 3,5 and 7-stages VCO with fine tuning. Fig. 7 illustrate output waveforms of three, five and seven stages VCO at V_{dd} of 1.8 V.

Table 3 shows results of phase noise performance for 3,5 and 7-stages VCO with coarse and fine tuning.

In proposed circuits, power consumption is increased with addition of delay stages whereas output frequency is showing decreasing trend. Target applications of the proposed circuit are low voltage, low power wireless communication systems. Coarse tuning method find applications in multi band wireless communication systems. Fine tuning method can be used in those applications where power is of prime concern and



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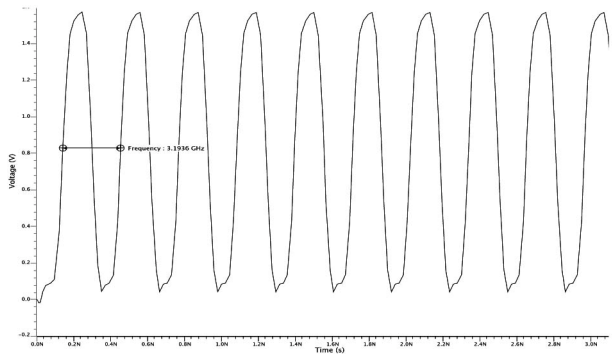

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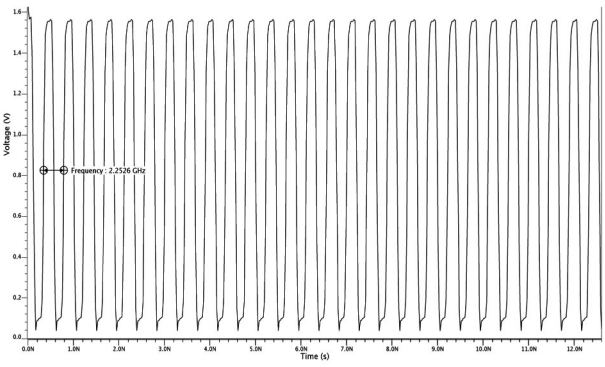
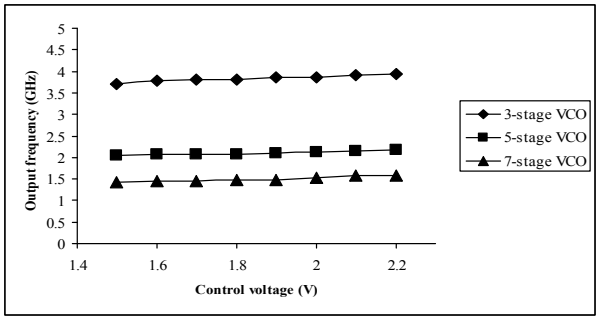
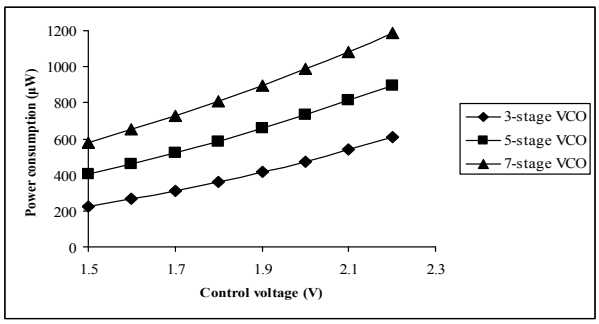


(c)

Fig. 5. Waveforms (a) 3-stage, (b) 5-stage, (c) 7-stage VCO with coarse tuning.



(a)



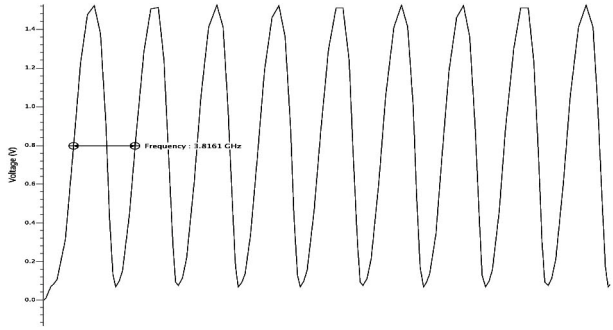
(b)

Fig. 6. (a) Frequency, (b) Power variations with fine tuning.

operating frequency range is limited such as wireless sensor nodes (WSN). Ultra low power wireless sensor network also needs high frequency and low power devices to monitor and control life environments. A comparison with previously reported circuits in terms of output frequency range, power consumption and phase noise is presented in Table 4. Proposed circuit's is showing better results in terms of output frequency and power consumption.

IV. CONCLUSIONS

New designs of CMOS ring oscillator using the combination of three transistor NAND gate delay stage and CMOS inverter delay stage have been reported in this work. The proposed VCOs achieves the output frequency from 3.318 GHz to 5.604 GHz in three stages, 1.77 GHz to 3.26 GHz in five stages and 1.27 GHz to 2.32 GHz in seven stages design for the coarse tuning mode. The output frequency varies from 3.70 GHz to 3.94 GHz in three stages, 2.04 GHz to 2.18 GHz in five stages and 1.43 GHz to 1.58 GHz in seven stages design in fine tuning mode. Phase noise results of proposed VCO circuits also show compliance with earlier reported



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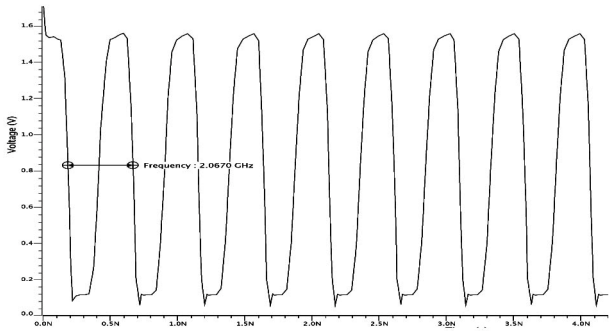

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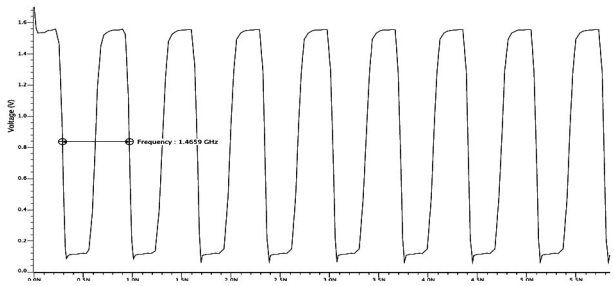

(c)

Fig. 7. Waveforms (a) 3-stage VCO, (b) 5-stage VCO, (c) 7-stage VCO circuits.

Table 3.

VCO Circuit	Phase Noise (coarse tuning) (dBc/Hz)	Phase Noise(fine tuning) dBc/Hz
Three delay stage VCO	-77.60@1 MHz	-80.28@1 MHz
Five delay stage VCO	-84.77@1 MHz	-82.39@1 MHz
Seven delay stage VCO	-87.94@1 MHz	-88.30@1 MHz

circuits. Proposed designs have been compared with earlier designs in terms of output frequency, power and phase noise. Significant improvements in output frequency and power consumption have been obtained in the proposed VCO circuits.

Table 4. Comparison of VCO performances

VCO designs	Frequency (GHz)	Technology (μm)	Supply voltage (V)	Power	Phase Noise (dBc/Hz)
[8]	0.39 to 1.41	0.18	1.8	12.5 mW	-80 @600 KHz
[13]	1.57 to 3.57	0.090	1.8	16.8 mW	- 90.01 @600 kHz
[15]	0.65 to 1.6	0.18	1.8	39 mW	-
[17]	0.186 to 1.576	0.18	1.8	11.38	-
[23]	3.125	0.18	1.8	12.6	-
[24]	0.381 to 1.15	0.35	3.3	7.48	-
3-stag VCO (Coarse tuning)	3.31 to 5.60	0.18	1.8	310.75 to 689.70 μW	-77.60@1 MHz
5-stage VCO (Coarse tuning)	1.77 to 3.26	0.18	1.8	477.91 to 1276.3 μW	-84.77@1 MHz
7-stage (Coarse tuning)	1.27 to 2.32	0.18	1.8	644.95 to 1853.3 μW	-87.94@1 MHz

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