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A Recessed-channel Tunnel Field-Effect Transistor (RTFET) with the Asymmetric Source and Drain

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***Abstract*—Tunnel field-effect transistor (TFET) is a promising candidate for the next-generation electron device. However, technical issues remain for their practical application: poor current drivability, short-channel effect and ambipolar behavior. We propose herein a novel recessed-channel TFET (RTFET) with the asymmetric source and drain. The specific design parameters are determined by technology computer-aided design (TCAD) simulation for high on-current and low *S*. The designed RTFET provides ~446× higher on-current than a conventional planar TFET. And, its average value of the *S* is 63 mV/dec.**

***Index Terms*—Tunnel filed-effect transistor (TFET), ambipolar, recessed-channel TFET**

I. INTRODUCTION

Tunnel field-effect transistor (TFET) has been regarded as a promising candidate for future enery-efficient device because it can achieve steep subthreshold swing (S) [1-4]. However, there are several impediments for its commercialization: relatively low on-current (I_{on}) due to its limited band-to-band tunneling (BTBT) junction area defined by shallow inversion layer, unwanted ambipolar leakage current (I_{amb}) due to BTBT at drain junction [5] and short-channel effect (SCE) such as drain-induced barrier thinning (DIBT) [6] and source-to-drain direct tunneling. During last decade, several studies have been carried out to address those technical issues, especially for high on-off current ratio (I_{on} / I_{off}) [3, 7-9]. Among them, the device structure, which feature BTBT perpendicular to the channel direction, are very attractive in terms of high I_{on} and low S becuase their BTBT junction area (A_t) and barrier width (W_t) are defined by geometrical design parameters [3, 9]. On the other hand, the recessed-channel structure is very helpful to address SCE with the help of increased physical channel length.

In this manuscript, we propose a recessed-channl TFET (RTFET) with the asymmetric source / drain to improve I_{on} / I_{off}. It has a seletive epitaxial-silicon (Si) layer to obatain small W_t and a recessed channel to suppress SCE. Its large gate-to-source overlap (i.e., large A_t) can increase the I_{on}, where non-overlapped gate-to-drain can reduce I_{amb} effectively. The characteristics of proposed device are examined by technology computer-aided design (TCAD) simulation, Atlas Silvaco V5.19.20. The nonlocal BTBT model is enabled in order to account tunneling mechanism based on Wentzel-Kramer-Brillouin approximation.

II. DEVICE STRUCTURE AND PROCESS

The structure of RTFET with the asymmetric source / drain is depicted in Fig. 1. It features epitaxial-Si layers between the source and gate dielectric and recessed channel to reduce SCE. In addition, source / drain doping profiles are different to each other based on a particular purpose (will be discussed). Fig. 2 shows a comparison of transfer characteristics between RTFET and planar TFET.

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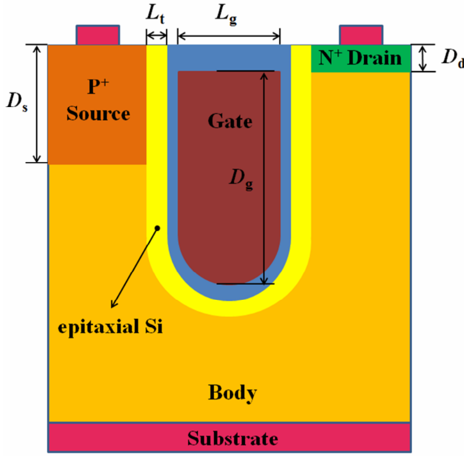


Fig. 1. Schematic diagram of RTFET with asymmetric source / drain.

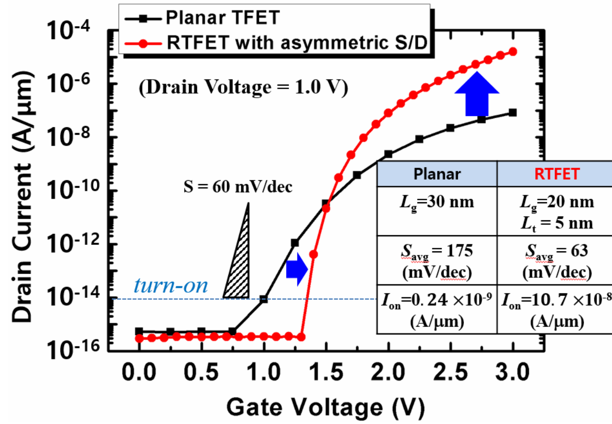
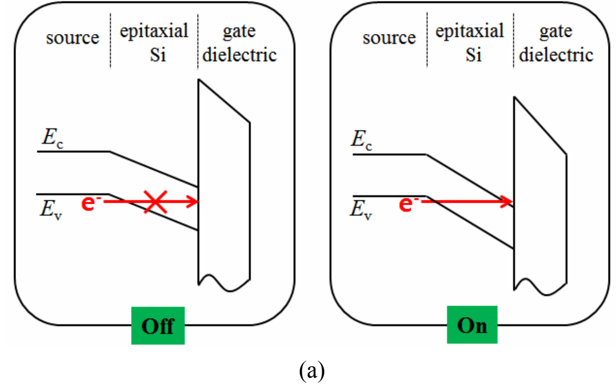


Fig. 2. Transfer characteristics of planar TFET and RTFET. The equivalent oxide thickness (EOT) for gate dielectric and source / drain doping concentrations are 2 nm and 1×10^{20} / 5×10^{19} cm^{-3}, respectively.

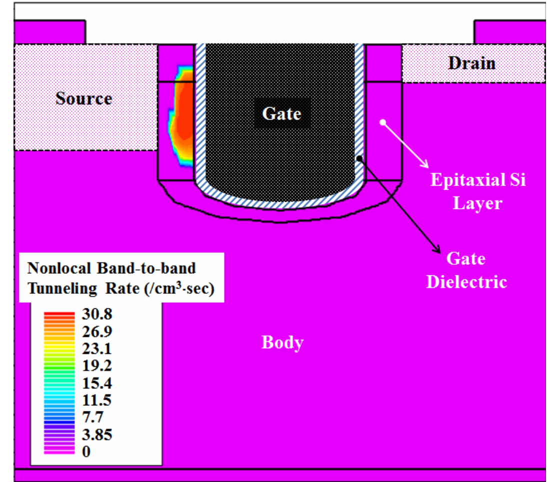
Table 1. Parameters of the baseline of designed device

Metal gate work-function	4.6 eV
Physical gate length (L_g)	20 nm
EOT of gate dielectric	2 nm
Recess depth of gate (D_g) in RTFET	50 nm
Junction Depth in planar TFET	20 nm
Depth of source junction (D_s) in RTFET	20 nm
Depth of drain junction (D_d) in RTFET	0 nm
Thickness of epitaxial Si (L_t) in RTFET	5 nm
N-type source doping concentration	1×10^{20} cm^{-3}
P-type drain doping concentration	5×10^{19} cm^{-3}
Body doping concentration	1×10^{15} cm^{-3}
Epitaxial Si doping concentration in RTFET	1×10^{15} cm^{-3}

Key parameters of devices for simulation are summarized in Table 1. A turn-on voltage ($V_{turn\text{-}on}$) is defined as gate voltage (V_g) when drain current (I_D) is



(a)



(b)

Fig. 3. (a) Conceptual energy band diagram of RTFET from source to gate, (b) Two-dimensional contour plot of electron BTBT rate for RTFET.

10^{-14} A/μm. An average S (S_{avg}) indicates a reciprocal of mean ratio of change in the log(I_D)-V_g curve when I_D increases from 10^{-14} A/μm to 10^{-9} A/μm. Lastly, I_{on} is extracted for $V_g = V_{turn\text{-}on} + 0.7$ V.

As indicated in Fig. 2, RTFET has two distinct advantages over planar TFET. First, the S_{avg} of RTFET is far smaller than that of planar TFET. In the case of RTFET, maximum W_t is fixed by epitaxial-Si thickness (L_t). As depicted in Fig. 3(a), the BTBT is not occurred until the conduction band edge (E_C) at the interface of epitaxial Si / gate dielectric is aligned with the valence band edge (E_V) at the source [3]. Consequently, RTFET has higher BTBT probability at $V_{turn\text{-}on}$, resulting in more abrupt on / off transition than planar TFET.

Second, RTFET shows ~446× higher I_{on} than planar TFET. The BTBT of planar TFET occurs through the thin inversion layer. On the other hand, in the case of RTFET, the tunneling occurs through the epitaxial Si

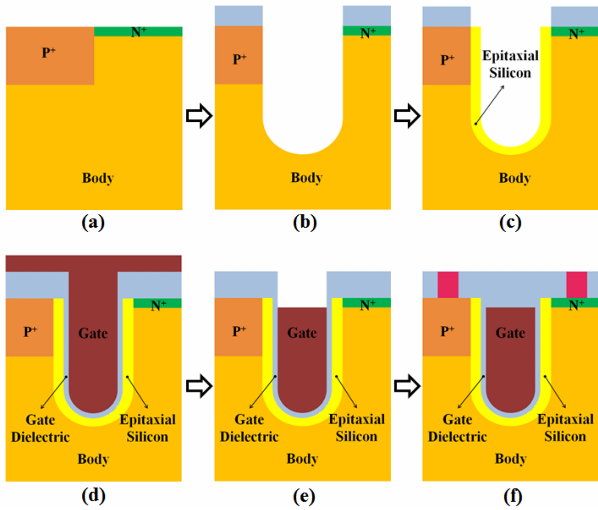


Fig. 4. Key process flow of the proposed RTFET with the asymmetric source and drain.

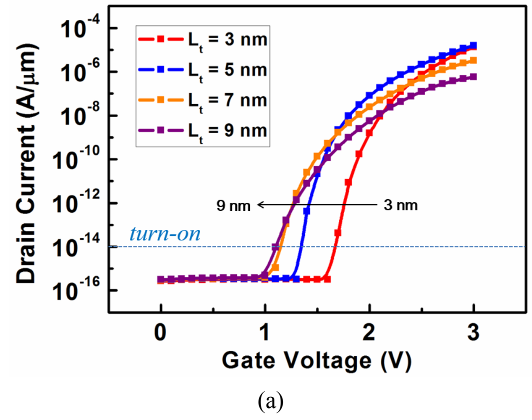
layer at the source / gate overwrapped region as shown in Fig. 3(b). Therefore, in order to achieve excellent current drivability, A_t can be increased by increasing source junction depth.

Fig. 4 shows cross-sectional illustration of process flow for RTFET with the asymmetric source / drain. (a) First, deep source and shallow drain regions are formed by sequential ion implantations. (b) It is subsequently etched to from recessed-channel region (i.e., trench) with the help of hard-mask layers followed by (c) epitaxial-Si layer growth in low temperature to suppress dopants diffusion from the source to epitaxial-Si region. An abrupt tunnel junction is achievable by using epitaxial-Si layer. (d) Gate dielectric and gate material are deposited. (e) After etch-back process to adjust gate depth (D_g), (f) conventional back-end processes are performed for contact metal lines.

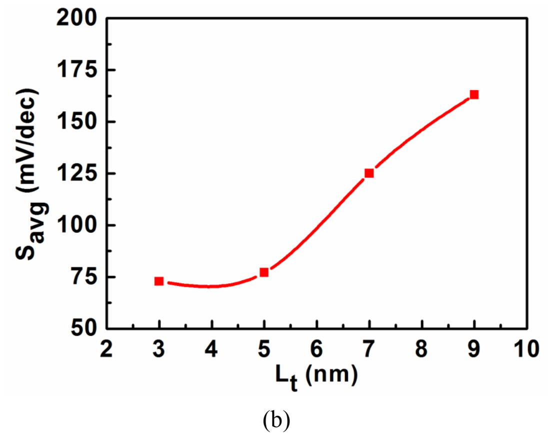
III. DEVICE CHARACTERISTICS STUDY

From now on, the effects of various device parameters such as L_t, depth of source junction (D_s), depth of drain junction (D_d) and D_g on electrical characteristics of RTFET are discussed. The default parameters used in this study are listed in Table 1, while drain voltage (V_d) is fixed at 1.0 V.

First, the dependency of device performance on the L_t has been simulated. Fig. 5(a) and (b) shows transfer curves and S_{avg} as a function of L_t, respectively. As L_t



(a)



(b)

Fig. 5. (a) Transfer curves, (b) S_{avg} with the variation of L_t.

increases from 3 to 9 nm, $V_{turn\text{-}on}$ decreases and S_{avg} increases. In the case of large L_t, even if the E_V of the source is aligned with the E_C of epitaxial-Si at gate dielectric interface, W_t is still large. In other words, BTBT current is not high enough to turn on the device and just remains to leakage current (i.e., $I_D < 10^{-8}$ μA/μm) [2]. A smaller L_t is preferred for the lower S_{avg}. Because there is a trade-off in terms of $V_{turn\text{-}on}$ increase as L_t decreases, it is concluded that optimum L_t is 5 nm for RTFET.

Second, the influences of D_s and D_d are investigated. Fig. 6 shows the current drivability depending on D_s. The I_{on} is linearly increased as D_s increase. As D_s changes from 10 to 40 nm, I_{on} is increased from 0.7 to 32.7 μA/μm. It is mainly attributed to the lower tunneling resistance with the help of the wider A_t [2]. Fig. 7 shows transfer curves with the various D_d. The D_d has no influence on I_{on} and $V_{turn\text{-}on}$ which are dominated by BTBT at the source junction. On the other hand, the change of D_d significantly impacts on the I_{off} with negative gate voltage. Fig. 7 (b) shows the effect of D_d

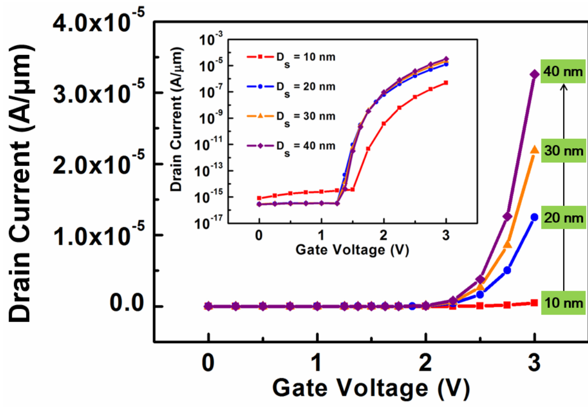


Fig. 6. Transfer characteristics with the variation of D_s.

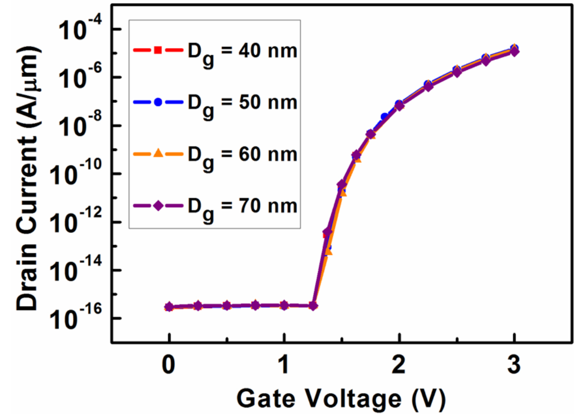
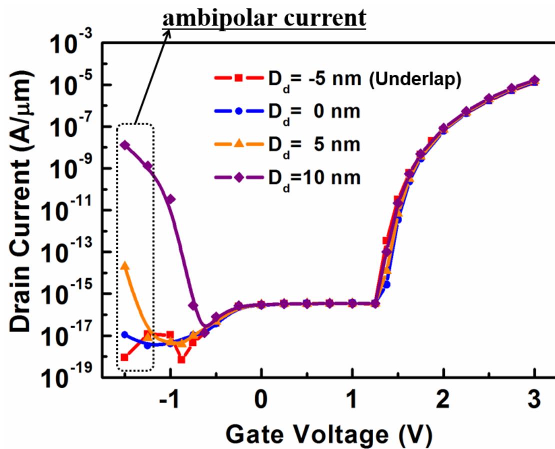
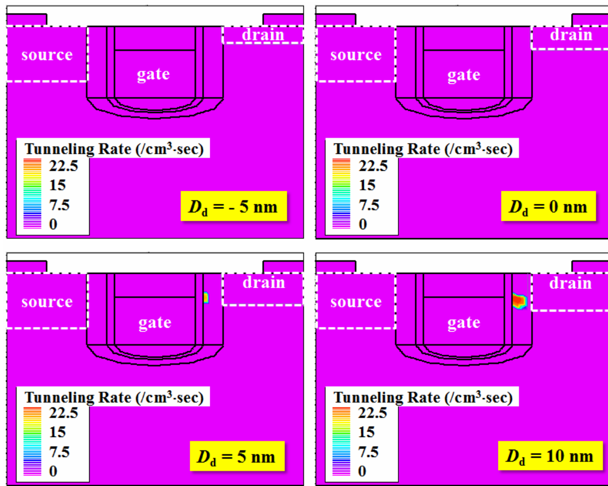


Fig. 8. Transfer curves with the variation of D_g.



(a)



(b)

Fig. 7. (a) Transfer characteristics, (b) two-dimensional contour plots of BTBT rates at drain junction for V_g = -1.5 V depending on the D_d.

on the BTBT at drain junction, i.e., ambipolar behavior. As the D_d increase, the gate-to-drain overlapped region is increased, resulting in I_{amb} increase. As a result, a RTFET with shallow or underlapped drain junction is required. In other words, an asymmetric source and drain profile is necessary to achieve both high I_{on} and low I_{off}.

Third, the dependency of device characteristic on the D_g has been studied. The D_g impacts neither the subthreshold characteristic nor I_{on} as indicated in Fig. 8. The recessed channel shields the electric field from the drain to prevent it from influencing tunneling barrier near the source region. As a result, the proposed RTFET has the stable subthreshold characteristic. Also, since I_D of TFETs is dominated by tunneling resistance at source junction which is generally much larger than channel resistance as is well known, the change of channel length seldom effect on the I_{on} [reference]. Therefore, even if recess depth of gate increases by extending source-gate overlapped region, the current drivability can be successfully boosted without the area penalty.

V. SUMMARY

In this work, we proposed a new design of recessed-channel tunnel FET with asymmetric source and drain. Using epitaxial silicon layer along with recessed-channel, it features lower subthreshold swing than planar TFET due to the small fixed-tunneling distance. The effects of various device parameters have been investigated by simulation study. Deep source junction profile can increase the on-current without a penalty of area. Also, we can effectively suppress a leakage current from ambipolar behavior by non-overwrapped gate-to-drain junction profile. Therefore, it is expected that an RTFET having asymmetric source and drain will be one of the most promising candidate for a next-generation transistor.

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