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Quantum Simulation Study on Performance Optimization of GaSb/InAs nanowire Tunneling FET

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***Abstract*—We report the computer aided design results for a GaSb/InAs broken-gap gate all around nanowire tunneling FET (TFET). In designing, the semi-empirical tight-binding (TB) method using sp3d5s* is used as band structure model to produce the bulk properties. The calculated band structure is cooperated with open boundary conditions (OBCs) and a three-dimensional Schrödinger-Poisson solver to execute quantum transport simulators. We find an device configuration for the operation voltage of 0.3 V which exhibit desired low sub-threshold swing (< 60 mV/dec) by adopting receded gate configuration while maintaining the high current characteristic (I_{ON} > 100 μA/μm) that broken-gap TFETs normally have.**

***Index Terms*—Tunneling field effect transistor, GaSb, InAs, nanowire, quantum transport**

I. INTRODUCTION

Reducing the size of metal-oxide-semiconductor field effect transistors (MOSFETs) has been traditional way to speed up the switching while having increased integration density followed by reduction of the cost in producing logic circuit chips. But the increased transistor number density increases power loss to heat that should be cooled by appropriate package methods. However, the MOSFET scaling recently has entered the regime of air cooling capacity limitation (~100 Wcm^{-2}) that means no further scaling down is possible unless a suitable and cost effective cooling method is invented or the power loss is dramatically reduced without losing its performance. Because reduction of (active/standby) power loss is synonymous with reduction of operation voltage, the above stated problem changes to make MOSFETs have equivalent level of on state current with lowered operation voltage than before. To speak in device physics terminology, the subthreshold swing (S) should be lowered compared to the conventional MOSFET. But the biggest obstacle has come before us at this stage, that is SS intrinsically has lower limit of 60 mV/dec at room temperature due to the physical limitation of the drift-diffusion carrier conduction mechanisms that the conventional MOSFETs have. Therefore it has been a long time issue to find a device having S smaller than 60 mV/dec to meet the aforementioned need.

Among the new devices invented to break through the S limitation problem, tunneling field-effect transistors (TFETs) have emerged as the most promising candidates [1]. TFETs often have the source-channel-drain structure of p-i-n (n-type) or n-i-p (p-type) operated in reverse bias, where the carrier conduction take place by band-to-band tunneling (BTBT) between the source and the channel. Although TFET can have a S smaller than 60 mV/dec, there is a critical drawback comes from its conduction mechanism (BTBT), that is the relatively small high on current (I_{ON}) than the conventional drift-diffusion type MOSFETs. In order to put TFETs as an powerful contender for logic application circuit industry, it is known that I_{ON} should be larger than at least 100 μA/μm while S lower than 60 mV/dec [1].

There are lots of TFET types that have been proposed

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and among such various types, TFETs with a broken gap at source/channel junction have attracted much attention for a candidate to overcome low I_{ON} issue [2-6]. However, none of these reports have approved the capability to achieve the required conditions for I_{ON} and S. The difficulty in getting both conditions at once comes from the fact that the two device output parameters are generally proportion to each other.

It has been revealed that doping density optimization (apart from doping profile engineering) in source/channel junction region cannot effectively control S but only can control I_{ON} [6-8]. One of powerful means other than that is to managing S for a given nanowire is to modify the location that dominant BTBT takes place by gate edge position optimization. In this work, we perform full-bands (obtained by the tight-binding method) atomistic quantum transport simulations of GaSb/InAs broken-gap nanowire TFET and try the optimization of the device performances by adopting recessed gate configuration to achieve the desired I_{ON}(>100 μA/μm) and S(<60 mV/dec).

II. SIMULATION METHODS

Because relatively accurate BTBT calculations are required in nanometre sized TFET simulation, we have performed full 3-D atomistic quantum transport simulations based on tight-binding approximation instead of using the much simpler one-dimensional Wentzel-Kramers-Brillouin approximation. The full quantum transport simulation of the device is performed with the tool named NEMO5 [9]. In this tool, the band structure of the GaSb and InAs is obtained by solving the Schrödinger equation through the nearest-neighbor tight-binding method (sp3d5s* with considering spin-orbit coupling) and transport of carriers is modeled within the wave function formalism with open boundary conditions and effective masses [10] which is computationally much more efficient than NEGF method [11]. Carrier densities are calculated by self consistently coupling multi-slab based Schrödinger equation [6] and Poisson equation. Carrier scattering effects are not considered because effective mean free path of carriers in the channel is normally larger than 10 nm so that carrier transport becomes near ballistic. Thus in this case, carrier mobility degradation as gate bias increases which is mainly due to interface carrier scattering does not appear.

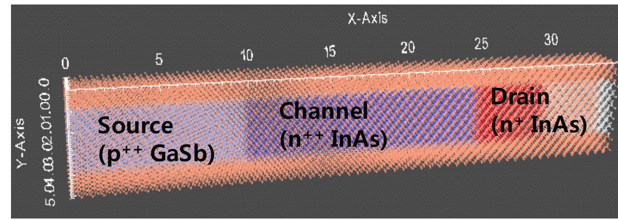

Fig. 1. The cross sectional view of the full-3D atomistic simulation structures for GaSb/InAs hetero-junction GAA nanowire TFET.

Fig. 1 shows the simulation geometry of the InAs/GaSb gate all around (GAA) nanowire considered in this paper. The wire is composed of a 10 nm p-doped GaSb source region (variable doping densities), a 15 nm n-doped InAs channel (N_D = 1×10^{15} cm^{-3}), and a 10 nm n-doped InAs drain (N_D = 1×10^{18} cm^{-3}). The drain region has two 5 nm sub-regions to control drain side doping profile because leakage current can be dominated by drain side band-to-band tunneling current. The carrier transport direction (wire axis direction) is <100> and the diameter of the wire is tested from 3 nm to 5 nm. The gate insulator is modeled to have 1 nm thickness, infinite barrier height, and dielectric constant of 25 that is the value of HfO_2 [12]. Thus the insulator only roles as electric field divider while ignoring wave-function penetration into the dielectric and dielectric/channel interface effects.

III. SIMULATION RESULTS

In Fig. 2, we show I_D-V_{GS} curves for different drain voltages (V_{DS}). Here, the diameter of the wire is 3 nm, the p-type dopant density in GaSb is 1×10^{19} cm^{-3}, the n-type dopant density in InAs channel is 1×10^{19} cm^{-3}, and n-type dopant density in InAs drain is 1×10^{18} cm^{-3}. From the comparisons between I_D at V_{GS} = 0.5 V, we can see, unlike drain current saturation phenomenon shown in the conventional MOSFETs, the apparent proportionality relationship between drain current and drain voltage. Unusually enough, for V_{DS} = 0.1 V, the drain current decreases as V_{GS} increases beyond 0.3 V. This is because a high gate voltage makes the band in the channel lower than the drain so that a conduction barrier is formed at the channel/drain junction. More specifically, because TFETs adopt p-i-n or n-i-p junction instead of p-n-p or n-p-n junction that the conventional MOSFETs have, there

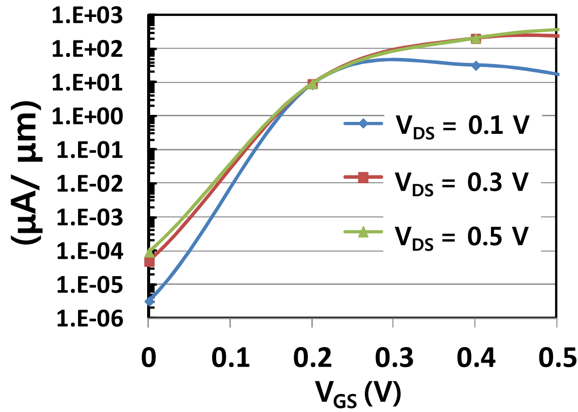

Fig. 2. I_D-V_{GS} curves for GaSb/InAs gate all around nanowire TFET. Here, the p-type dopant density in GaSb is 1×10^{19} cm^{-3}, the n-type dopant density in InAs channel is 1×10^{19} cm^{-3}, and n-type dopant density in InAs drain is 1×10^{18} cm^{-3}.

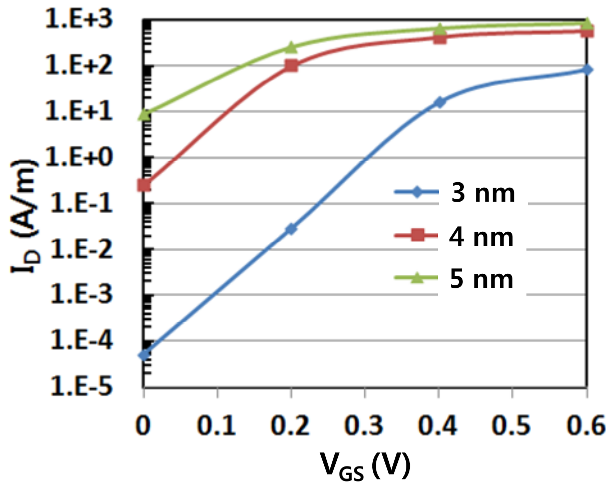

Fig. 3. I_D-V_{GS} curves (V_{DS} = 0.3 V) of GaSb/InAs GAA nanowire TFET for different nanowire diameters. The dopants are the same as in FIG. 2.

is relatively smaller band offsets for TFETs between channel and drain thus it is much easier to form a barrier at the junction.

Fig. 3 shows I_D-V_{GS} curves variation (V_{DS} = 0.3 V) with respect to the nanowire diameter (3 nm~5 nm) for the same dopant densities as in Fig. 2. The gate electrode (work function = 4.3 eV) is assumed to have 10 nm width and expand from the source-channel junction (x = 10 nm) and x = 20 nm position (as shown in Fig. 4, gate position 2). It can be seen the huge increase in I_D as the diameter increases. This is caused by decrease of the effective mass and increase of the density of states as the diameter increases. The effective mass of electrons in InAs differs from the bulk value (0.023 m_0) due to

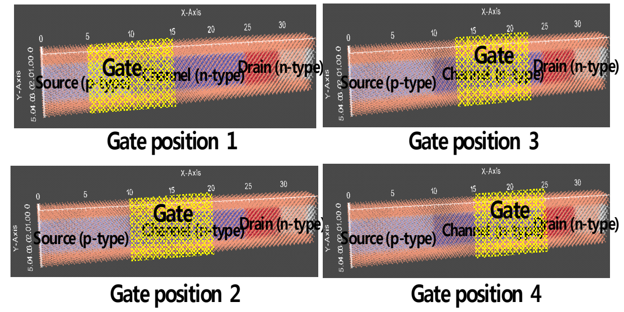

Fig. 4. GaSb/InAs GAA nanowire TFET with different gate positions. The position (from the source electrode) of source side gate edge (red line) are 5 nm, 10 nm, 12.5 nm, and 15 nm in numbering order with 10 nm gate length. The GaSb source doping density is 5×10^{19} cm^{-3} , the n-type dopant density in InAs channel is 5×10^{19} cm^{-3}, and the n-type dopant density in InAs drain is 1×10^{18} cm^{-3}.

quantum confinement effect. Specifically, the effective electron mass in InAs varies from 0.12 m_0 (3 nm diameter) to 0.069 m_0 (5 nm diameter). It should be noted that although I_D is greatly increased as the diameter increases, due to the increased total path ($\propto$ diameter) of BTBT and diminished gate controllability, the leakage current (I_D @V_{GS} = 0 V) also dramatically increases and this makes the sub-threshold swing be unacceptably far larger than 60 mV/dec (S varies from 73 mV/dec to 137 mV/dec as the diameter changes from 3 nm to 5 nm).

As a matter of fact, the need to increase I_{ON} of TFETs has made source and channel doping densities as high as possible, however, the increase of doping also increases leakage current and S as well. Thus, the main goal of the TFET design is, like any other MOSFETs, optimization to get large I_{ON} while keeping as low I_{OFF} as possible to have S smaller than 60 mV/dec. There can be largely two knobs that control the device performances in nanowire structure with a given materials combination. One is doping density profile engineering and the other is electrode (gate) structural optimization. Because the former was tried for the same material condition as ours [6], which was found to have inherent limit in reducing the leakage current, we apply the latter idea with 3 nm diameter nanowire by optimizing the gate position. The whole simulations are carried out with the diameter of 3 nm since it only shows a S near 60 mV/dec as shown in Fig. 3. The four simulated structures of different gate positions are shown in Fig. 4. The resulting I_D-V_{GS} curves (for the GaSb source doping density is 5×10^{19} cm^{-3} , the n-type dopant density in InAs channel is

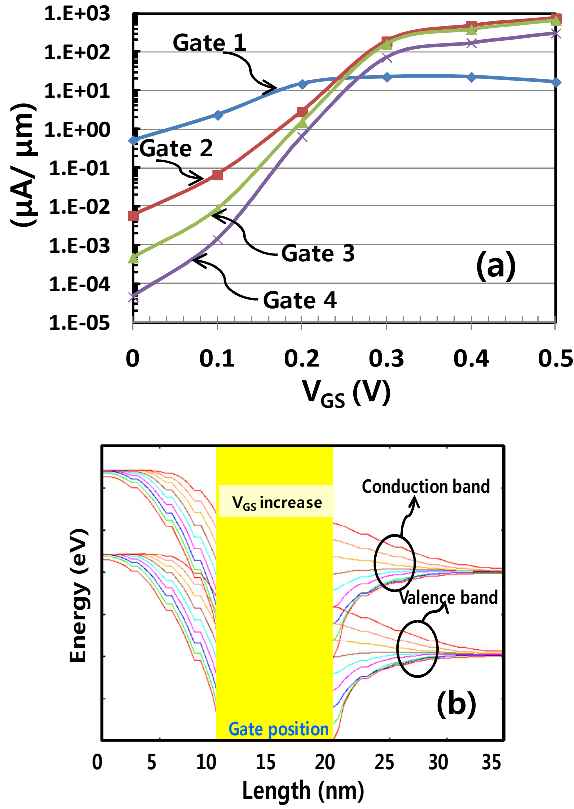

Fig. 5. (a) GaSb/InAs GAA nanowire TFET with different gate positions. The position (from the source electrode) of source side gate edge (red line) are 5 nm, 10 nm, 12.5 nm, and 15 nm in numbering order with 10 nm gate length. The GaSb source doping density is 5×10^{19} cm^{-3}, the n-type dopant density in InAs channel is 5×10^{19} cm^{-3}, and the n-type dopant density in InAs drain is 1×10^{18} cm^{-3}, (b) Energy band alignment change with respect to gate bias for the gate position 2 case.

5×10^{19} cm^{-3}, and the n-type dopant density in InAs drain is 1×10^{18} cm^{-3}) are plotted in Fig. 5(a) and band alignment variations with respect to V_{GS} for gate position 2 case is shown in Fig. 5(b), and the corresponding device performance parameters are listed in Table 1. As can be seen in Fig. 5(a), small modifications of gate edge position make dramatic changes in transfer curves. Specifically, I_{OFF} decreases up to 104 orders (5.2×10^{-1} $\rightarrow 4.6\times10^{-5}$ μA/μm from the Gate position 1 to the Gate position 4) as the gate is recessed 7.5 nm toward the drain while I_{ON} decreases only fractionally (230→190→160→72 μA/μm from the Gate position 1 to the Gate position 4) but still remain around at 100 μA/μm and of course this leads to lower S (124→61→45→38 mV/dec from the Gate position 1 to the Gate position 4) which is defined with the steepest slopes for each curve. Comparing with the conventional gate position that the

Table 1. Device Performance summary

	Gate 1	Gate 2	Gate 3	Gate 4
I_{ON} (μA/μm)	23	190	160	72
I_{OFF} (μA/μm)	5.2×10^{-1}	5.8×10^{-3}	4.7×10^{-4}	4.6×10^{-5}
I_{ON}/I_{OFF} ratio	4.4×10^{1}	3.3×10^{4}	3.4×10^{5}	1.6×10^{6}
S(mV/dec)	124	61	45	38

gate edge coincides with the source to channel junction, only 2.5 nm recession of gate edge position from the source/channel junction toward the drain side (from the Gate position 2 to the Gate position 3) make I_{OFF} decrease about 10 times ($5.8\times10^{-3}\rightarrow4.7\times10^{-4}$ μA/μm) while I_{ON} decrease only small amount (190→160 μA/μm) and S enter into the lower limit domain of it (61→45 mV/dec). The explanation of the huge dependence on the gate position can be deduced from the following approximate equation for BTBT probability [1]

$$T \propto \exp\left(-\frac{4\lambda\sqrt{2mE_g^{\,3}}}{3q\hbar\left(E_g+V\right)}\right). \quad (1)$$

Here, λ is the potential screening length, m is the effective mass of electron, E_g is the band gap of source material, and V is the applied voltage. Because λ is determined by both the channel geometry and the gate position at source side, the BTBT probability varies as gate position varies. As can see in the equation, large λ makes the BTBT probability low and it results in low I_{ON} and I_{OFF}. With the given E_G and the operation voltage V, the optimal λ to maximize I_{ON}/I_{OFF} ratio exists and this again means existence of the optimal gate position for the specific TFET which for our case of GaSb/InAs nanowire, the optimal gate position is the Gate position 3 (2.5 nm moved from the source/channel junction toward the drain side) in Fig. 4. This result with the optimal gate position is the best simulated performance level of nanowire TFETs ever reported that meet the requirements for TFETs (I_{ON} > 100 μA/μm and S < 60 mV/dec) for the operation voltage of 0.3 V tested in this work.

IV. CONCLUSION

We have performed 3-D atomistic simulations of n-type GAA nanowire TFET which has broken-gap GaSb/InAs hetero source/channel junction in it. We designed the device by optimizing the position of source side gate edge in which BTBT occurs to achieve the goals of high I_{ON} (> 100 μA/μm) and low S (< 60 mV/dec) at the same time. The results showed that devices with gate positioned at ~2.5 nm apart from the source/channel junction to drain side is much better than conventionally used configuration (gate edge coincides with the junction). Adoption of the recessed gates makes it possible that, by only slightly increasing BTBT barrier at V_{GS} = 0 V, I_{OFF} significantly decreases while I_{ON} decreases only a small fraction of the original value to get a S lower than 60 mV/dec. Finally, we have found two recessed gate configurations that show remarkable performances of I_{ON} = 160 μA/μm with S = 45 mV/dec and I_{ON} = 72 μA/μm with S = 38 mV/dec for gate edge located at 2.5 nm and 5 nm from the junction respectively which are far better than the performance with the conventional gate configuration. The variation of the I_{ON}/I_{OFF} ratio with respect to the gate position should be explained by the screening length variation with respect to that of which the detailed theoretical investigations can be made for the future work.

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