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An Integrated High Linearity CMOS Receiver Frontend for 24-GHz Applications

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Abstract—**Utilizing a standard 130-nm CMOS process, a RF frontend is designed at 24 GHz for automotive collision avoidance radar application. Single IF direct conversion receiver (DCR) architecture is adopted to achieve high integration level and to alleviate the DCR problem. The proposed frontend is composed of a two-stage LNA and downconversion mixers. To save power consumption, and to enhance gain and linearity, stacked NMOS-PMOS g_m-boosting technique is employed in the design of LNA as the first stage. The switch transistors in the mixing stage are biased in subthreshold region to achieve low power consumption. The single balanced mixer is designed in PMOS transistors and is also realized based on the well-known folded architecture to increase voltage headroom. This frontend circuit features enhancement in gain, linearity, and power dissipation. The proposed circuit showed a maximum conversion gain of 19.6 dB and noise figure of 3 dB at the operation frequency. It also showed input and output return losses of less than -10 dB within bandwidth. Furthermore, the port-to-port isolation illustrated excellent characteristic between two ports. This frontend showed the third-order input intercept point (*IIP3*) of 3 dBm for the whole circuit with power dissipation of 6.5 mW from a 1.5 V supply.**

Index Terms—**CMOS, RF frontend, IF direct conversion receiver (IF-DCR), low noise amplifier (LNA), downconversion mixer**

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I. INTRODUCTION

Nowadays, road traffic crashes have become a major global concern. To enhance safety, automotive radar devices are now installing on many transport and luxury passenger vehicles. Automotive radars are utilized in advanced cruise control (ACC) systems, which can provide information for driver, and actuate a motor vehicle's accelerator and/or brakes to control its distance separation behind another vehicle. Radar-based driver assistance systems also have other important functions such as collision warning systems, blind-spot monitoring, lane-change assistance, rear cross-traffic alerts and back up parking assistance, collision mitigation systems and vulnerable road user detection. The receiver for the automotive radar system operates in the band of 24 GHz frequency. Direct conversion receiver (DCR) is the best candidate among the various receiver architectures due to the low cost and low power issues. However, large dc offset, LO leakage, 1/f noise, and I/Q mismatch are the bottlenecks of DCR receiver [1, 2].

To alleviate these problems, single intermediate frequency (IF) DCR architecture has been proposed with the advantage of both the super-heterodyne and DCR architectures [3]. In this receiver type, at first, the incoming signal is converted to IF and then again it is converted to baseband frequency. This operation alleviates the specifications of the receiver back-end and enables the analog-to-digital conversion at low frequencies [4]. For this operating frequency, there have been literatures developing the radar receiver [5-7] and many of them were realized in CMOS technology due to its low cost, technology scaling and high inerrability level.

In this paper, a low-power, high-linearity and fully

integrated receiver frontend is designed in 130-nm CMOS technology for 24 GHz automotive radar application. The proposed circuit is based on single IF DCR architecture and thus is suitable for silicon integration. The remaining of this paper is organized as follows. In section II, the structure of the receiver frontend will be described. Design and analysis for CMOS circuit blocks will be presented in section III. Section IV shows the results and comparison with other published works. Section V summarizes and concludes this work.

II. Proposed Receiver Frontend Architecture

The main wireless receiver task is to detect the desired modulated signals. Wireless receivers have to perform several functions such as tuning to the wanted signal carriers, filtering out the undesired signals, and amplifying the desired signal to compensate for power losses occurring during transmission. However, there are several receiver architectures, and the heterodyne and the direct conversion are the most popular.

Typically, a heterodyne receiver translates the desired input RF signal to one or more preselected intermediate frequencies before modulation [8]. In this architecture, image rejection and IF filters are vital to avoid folding of interfering signals. Because of presence of several bulky and expensive RF/IF filters, the heterodyne architecture is not suitable for monolithic integration. Enforced by the trends to the cost and size of the RF frontend, alternative heterodyne architecture has been proposed. For instance, direct conversion technique converts the RF signals to the IF-zero baseband in the first frequency downconversion. Therefore, the receiver frontend can be realized in low cost and low power architecture due to the unnecessary off-chip IF filters. Despite superior performances of direct conversion architecture, it suffers from the dc offset and LO leakage which leads to complicate the design and implement of individual blocks in order to relax the specifications of system.

A modified IF receiver architecture is adopted as a compromise between the heterodyne and the direct conversion to have immunity against flicker noise, dc offset, I/Q mismatch and to achieve higher integration. The block diagram of the proposed receiver frontend is illustrated in Fig. 1. First, LNA amplifies the incoming RF signal at 24 GHz. Then the amplified signal is down-converted to a low IF of 10 MHz by the first and second mixer stages. It is noted that the quadrature LO signals required for the second mixer are generated by dividing the first LO signal by 2.

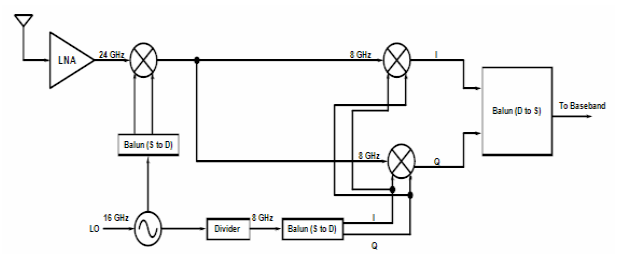

Fig. 1. Proposed 24 GHz receiver frontend.

The unwanted image signal can be attenuated at least 20 dB by exploiting narrow band characteristic which is provided in the input port of LNA. A LO frequency of 16 GHz is applied to the first mixer to generate signals at an IF band of 8 GHz. Furthermore, the finite bandwidth of receiver frontend leads suppressing of the spurious band of 40 GHz which is generated by the first mixer stage. A divided-by-2 extended true-single-phase-clock (E-TSPC) frequency divider is also designed to provide the quadrature LO signals required for the second mixer stage. Therefore, the output signals of the second mixer stage are located at 10 MHz. In order not to use off-chip components such as buffer, balun and filters, an active balun is adopted to perform three tasks as follows: (i) convert the differential output of the second mixer to single-ended output for simulation of the frontend performances; (ii) match the output ports of the whole circuits to 50-Ω to achieve S_{22} of less than -10 dB; (iii) filter out the undesired image and spurious signals.

III. Design and Analysis of CMOS Circuit Blocks

1. LNA

A low noise amplifier (LNA) is typically the first active block in the receive path of communication transceivers [9]. The LNA's performance has a direct impact on the linearity, noise figure and power consumption of the entire frontend system [10]. Therefore, tradeoffs for the noise figure, gain and

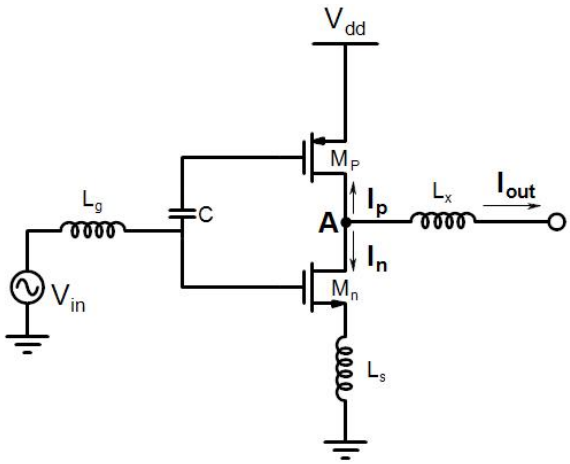

Fig. 2. Schematic of the proposed complementary push-pull LNA.

linearity have to be taken into account to find the suitable LNA configuration. Among the RF designers, common source and cascode topologies are the most popular configurations in CMOS technology. At high frequencies, if stability, gain and reverse isolation are taken into consideration, the latter is preferred. However, the degradation of noise figure at high frequencies is the disadvantage of this configuration. To satisfy the LNA tradeoffs, a complementary push-pull (CPP) [11] topology is chosen using PMOS and NMOS transistors which are stacked on top of one another as shown in Fig. 2. This stacked topology is the most efficient method to maximize the transconductance (g_m) by a fixed dc current, and it enhances the LNA gain compared to a single common source stage. In CPP topology, the main problem is that at high frequencies the parasitic capacitances cause to degrade the bandwidth and input impedance matching due to the Miller effect. To relax this problem, source inductive degeneration (SID) and series-peaking techniques are adopted.

For input impedance matching, the gate inductance (L_g), NMOS source inductance (L_s) and parasitic capacitances of NMOS and PMOS transistors form a multiselection LC ladder to achieve desired input return loss (e.g. S_{11}<-10 dB).

For further analysis, Fig. 3 shows the small-signal model of the proposed inverter. Z_{in2} is the impedance can be seen from point A toward the following stages (i.e. inductor (L_x), mixers, balun) and Z_{in3} is the impedance looking from the coupled source terminal of single balanced mixer. Generally, due to the existence of C_{gdt} = C_{gdn} + C_{gdp}, the output impedance effects on the input impedance, and LNA is assumed to be bilateral two-port network. Due to the small value of overlap capacitance C_{gdt}, the Miller effect can be neglected in the practical design. By this assumption, the LNA functions as a unilateral two-port network and the total transconductance of the proposed LNA can be written in Eq. (1).

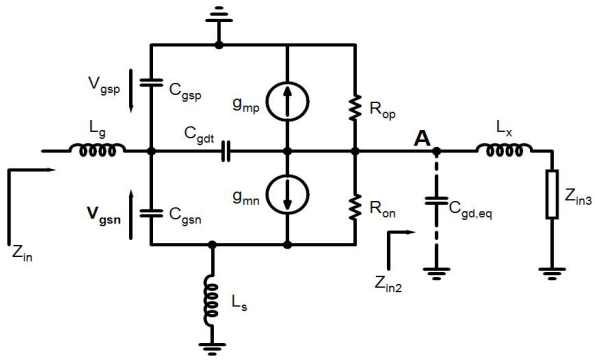

Fig. 3. Schematic of the proposed complementary push-pull LNA.

$$g_{m,LNA} = \frac{g_{mn}}{1 + j\omega L_s g_{mn}} + g_{mp} \tag{1}$$

where g_{mn} and g_{mp} are the transconductance of NMOS and PMOS, respectively.

According to Fig. 3, the voltage gain ($A_{v,LNA}$) of the LNA is expressed in Eq. (2).

$$A_{v,LNA} = g_{m,LNA}[((1 + j\omega L_s g_{mn})R_{on}) \,\|\, R_{op} \,\|\, Z_{in2}] \tag{2}$$

where R_{on} and R_{op} are the intrinsic output resistances of NMOS and PMOS, respectively.

The input impedance of the proposed LNA can be calculated using the small-signal circuit as given in Eq. (3)[1].

$$Z_{in} = j\omega L_g + [(j\omega L_s + \frac{1}{j\omega C_{gsn}} + \frac{g_{mn}L_s}{C_{gsn}}) \,\|\, \frac{1}{j\omega C_{gsp}}] \tag{3}$$

[1] Although, the input impedance of the bilateral LNA (existence of C_{gdt}) is so complicated and time-consuming, but it is provided in Eq. (4).

$$Z_{in} = \frac{s^2 C_{gsn} L_s R_{on} + sL_s(g_{mn}R_{on}+1) + (g_{mn}R_{on}+1)R_{on}}{s^3 L_s C_{gsn} C_{gdn} R_{on} + s^2(L_s C_{gsn} + L_s C_{gdn} g_{mn} + L_s C_{gdn} - C_{gsn} C_{gdn} R_{on}) - s(C_{gsn} + C_{gdn} + g_{mn} R_{on} C_{gdn})} \,\|\, \frac{s(R_{op}C_{gsp}) + g_{mp}R_{op} + 1}{s^2 C_{gsp} C_{gdp} R_{op} + s[(g_{mp}R_{op}+1)C_{gdp} + C_{gsp}]} \,\|\, Z_{in2} \tag{4}$$

where ω is the operation frequency, C_{gsn} and C_{gsp} are the parasitic capacitance of the NMOS and PMOS, respectively.

An inter-stage peaking inductor (L_x, series peaking technique) is inserted to isolate the stages from each other. As shown in Fig. 3, the parasitic capacitance of the inverter topology and following mixer along with L_x form a π section LC filter network at the resonance frequency of 24 GHz to boost gain and bandwidth. By this technique and choosing proper L_x value, the LNA gain roll-off at RF frequency will be compensated, and relatively flat gain can be achieved.

Due to the possible large interference signals at the input of the LNA, it has to provide high linearity, thus preventing the intermodulation tones created by the interference signal corrupting the carrier signal [12]. Thus, special attention has to be paid to the linearity performance of the LNA in the wireless transceiver design. The proposed CPP topology also addresses simultaneous minimization of the second- and third-order transcondactance of nonlinear coefficients g_{m2} and g_{m3}, respectively. By concurrently incorporating the well-known property of g_{m3} in weak and strong inversion regions, and the symmetric property of second-order nonlinear coefficient (g_{m2}) around sweet-spot, g_{m3} crosses zero in moderate inversion region [13]. The transfer function of NMOS and PMOS are described in Eqs. (5, 6).

$$i_n = g_{m1n}v_{gsn} + g_{m2n}v_{gsn}^2 + g_{m3n}v_{gsn}^3 + \ldots \quad (5)$$

$$i_p = -g_{m1p}v_{gsp} + g_{m2p}v_{gsp}^2 + g_{m3p}v_{gsp}^3 + \ldots \quad (6)$$

where g_{m1} is the main transconductance of the MOSFET, g_{m2} is the second-order nonlinear coefficient obtained by the second-order derivative of the dc transfer characteristic, and g_{m3} is the third-order nonlinear coefficient obtained by the third-order derivative of the dc transfer characteristic.

Since v_{gsp} is a function of v_{gsn}, it can be expanded into power series of v_{gsn} expressed in Eq. (7).

$$v_{gsp} = c_1 v_{gsn} + c_2 v_{gsn}^2 + c_3 v_{gsn}^3 \quad (7)$$

From the bias circuit theory, it is clear that the c_1 has positive value and the c_2 and c_3 values are negligible.

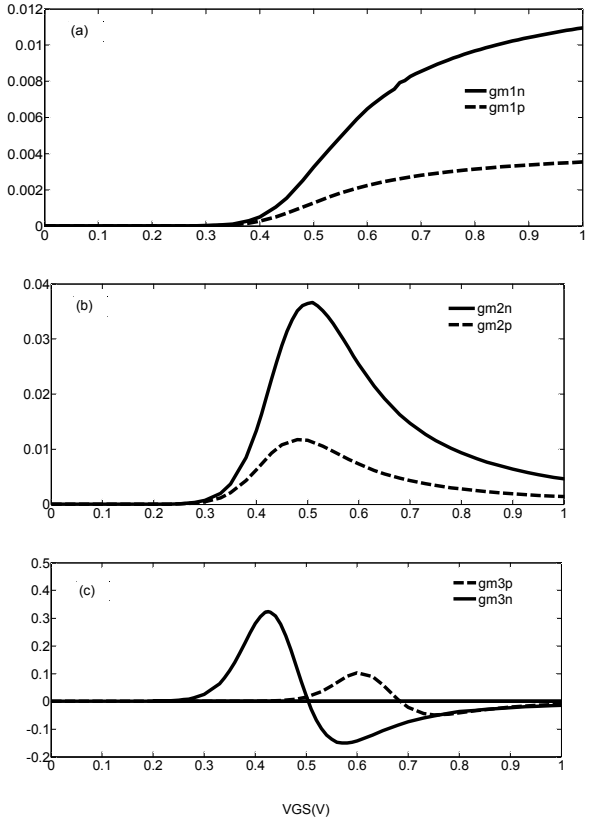

Fig. 4. (a) Simulated g_{m1n} and g_{m1p}, (b) Simulated g_{m2p} and g_{m2p}, (c) Simulated g_{m3n} and g_{m3p}.

As can be seen in Fig. 2, we have

$$i_{out} = i_n - i_p = (g_{m1n} + g_{m1p})v_{gsn} + (g_{m2n} - g_{m2p})v_{gsn}^2 + (g_{m3n} + g_{m3p})v_{gsn}^3 \quad (8)$$

Fig. 4 shows the simulated drain currents and their derivatives with respect to V_{GS} for NMOS and PMOS transistors operating in the strong inversion region. The third-order nonlinear coefficients of NMOS and PMOS transistors are shown in Fig. 4(c). As can be seen, gate bias voltages and sizes of the transistors are chosen to align the positive peak of the PMOS transistor with the negative peak of the NMOS, resulting in the g_{m3} with almost zero value.

The IIP3 of a nonlinear device is defined in Eq. (9) [11].

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \quad (9)$$

By using CPP configuration and choosing appropriate gate voltages and sizes of transistors, IIP3 of the LNA can be improved. With a simple analysis, the proposed technique can boost g_{m1} as shown in Fig. 4(a) and it can reduce g_{m3}. Therefore, CPP technique can highly improve linear performance of the LNA in the frequency range.

2. Mixer

The simplified schematic diagram of conventional I/Q mixer is shown in Fig. 5(a). It is composed of two cascased mixers, and each mixer consists of voltage to current (V-I) converter, Gilbert cell and current to voltage (I-V) converting trans-resistor. As can be seen the V-I converting transconductor converts the applied input voltage signal to current which is steered by the first mixer switch. The first mixer converts the high frequency current signal to IF signal. Then the translated signal at the output of the first mixer is reconverted to voltage by the I-V trans-resistor converter. The second V-I converter, again converts the IF voltage signal to current for the chopping function. The second Gilbert cell mixer converts IF current signal to baseband one, and ultimately the second I-V converting trans-resistor converts the steered current to voltage at the output port. High power consumption and low linearity are bottlenecks of this traditional architecture. The former comes from cascode structure in the first and second stages, and the latter is due to the existence of I-V and V-I converters. Fig. 5(b) illustrates the proposed circuit to alleviate drawbacks of the conventional architecture. Firstly, to avoid selection of cascode topology, a folded structure has been chosen. Folded mixers have become popular structure for high linearity and low-voltage operation. It is possible to avoid stacking transistors with a folded mixer [14]. However, folding the circuit adds additional current branches. By utilizing folded structure, the voltage headroom will be also increased. Furthermore, the first V-I converter is deleted and replaced by a CPP topology which functions as an LNA to increase the linearity and gain.

Secondly, the first mixer is realized using PMOS transistor. Having PMOS switches in LO stage helps to achieve same overdrive voltage and consequently similar linearity performance with lower power consumption compared to the case using NMOS transistors [15].

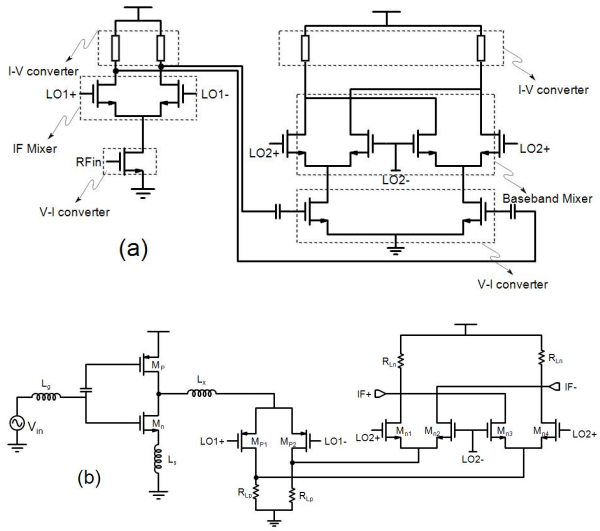

Fig. 5. (a) Conventional mixer with two stage, (b) Proposed mixer using folded architecture.

Finally, the first and the second I-V converting trans-resistor are realized in resistor to avoid employing inductor which leads to occupy large die area. Moreover, the second V-I converter is removed and this causes the double balanced mixer connects directly to the first switch mixer.

Low power consumption and low voltage operation are two essential requirements for mixers. Low voltage mixers are challengeable because traditional mixers rely on stacking multiple transistors [16]. In addition, circuits designed with MOS transistors biased in subthreshold region operate with lowered voltage headroom, resulting in smaller power supply and further reduced dc power dissipation [17]. Thus, the proposed mixer switches are biased in subthreshold region to reduce the power consumption. Furthermore, Fig. 6 clearly depicts that by biasing the switch transistors in weak inversion region, a gain enhancement of 10 dB will be yielded in comparison with biasing in strong inversion region.

There is another benefit to operate the mixer transistors in subthreshold inversion region. With this assumption that all switch transistors have constant transconductance (g_m) in subthreshold inversion; the noise performance will be significantly improved compared to strong inversion. There are two types of noise in RF frontend. Firstly, flicker noise which is inversely proportional to transistor size, and a weakly inverted transistor will be considerably larger than a strongly inverted transistor. Secondly, thermal noise will

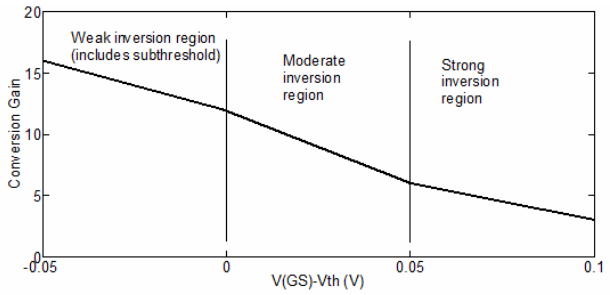

Fig. 6. Conversion gain versus mixer transistor regions.

be reduced because the value of the drain thermal noise factor (γ) which is approximately 25% smaller in weak inversion [18]. Meanwhile, in subthreshold region the required LO signal power is expected to be smaller, and it leads to reduce the dc power consumption of LO signal generator.

3. Frequency Divider

Frequency divider is the most challengeable stage in the receiver frontend and must be carefully designed to meet the speed specifications and to keep power consumption at a low level, simultaneously. Current-mode-logic (CML) latches have been utilized in conventional high speed flip-flop (FF)-based divider which has a large capacitance load. This not only increases the power consumption of the whole circuit, but also confines the operating frequency and current-drive ability. To reduce power consumption, the true-single-phase-clock (TSPC) divider was emerged. However, its operation was confined to the low frequency range. Ultimately, extended TSPC (E-TSPC) divider is designed for high speed and low power consumption. E-TSPC divider cancels the transistor with stacked structure so that all transistors are free from the body effect. Thus, they are more suitable for high operating frequency applications with low power supply [19].

Fig. 7 displays the proposed E-TSPC which is composed of three PMOSs and three NMOSs. Their aspect ratios are obtained by employing the classical domino logic scaling [20]. The sizes of the transistors are chosen in a way to achieve good matching at the expense of operating frequency and dynamic power consumption.

The input and output results of the frequency divider are shown in Fig. 8. As can be seen, the divider not only

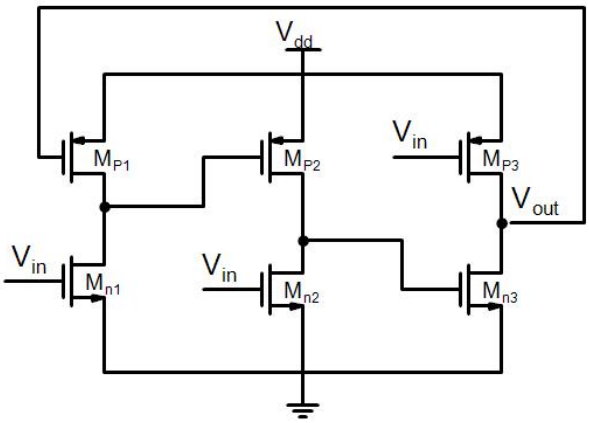

Fig. 7. Divided-by-2 E -TSPC frequency divider.

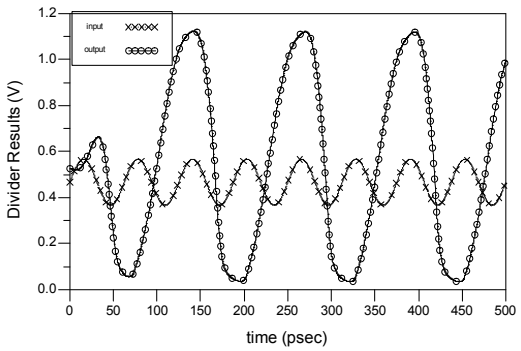

Fig. 8. Input and output waveforms of the divided-by-2 frequency divider with an input frequency of 16 GHz.

divides the input frequency by two precisely, but also amplifies the input signal at the output port (V_{out}). Therefore, the I/Q mixers operate in a LO power which is attractive for highly integrated ICs with low power consumption.

4. Balun

One of the most common problems in receiver frontend designs is that the LO source is single-ended and should be connected to the differential input mixer. One solution is to use passive balun implemented on board which is much bulkier than a silicon micro-strip line circuit, and the other solution is to utilize micro-strip lines for designing balance to unbalanced converter. To alleviate the foregoing drawbacks, an active narrow band balun which is shown in Fig. 9 is developed to convert the single-ended input to differential structure with a high gain precision for the entire band of 23.5 to 24.6 GHz. The proposed active balun consists of NMOS and PMOS

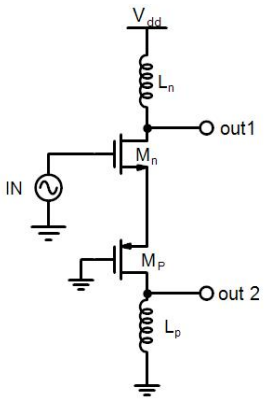

Fig. 9. Circuit schematic of single- to differential-ended balun.

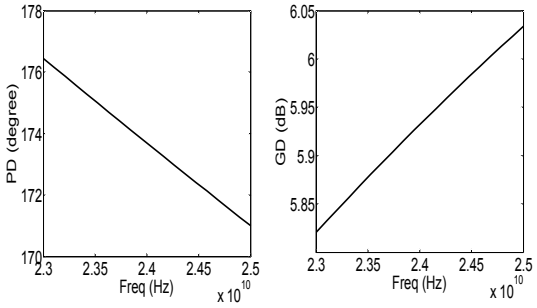

Fig. 10. Phase difference (PD) and gain difference (GD) between the output ports of S-D balun.

pair configuring in inverter type. As shown in this configuration, NMOS stacked on top of PMOS behave as common source and common gate, respectively. This topology reuses the dc current and leads to reduce power consumption. To reduce the deteriorative output parasitic capacitance influence of balun and parasitic capacitors of following mixers, inductors L_n and L_p are placed. These inductors with intrinsic capacitors of transistors form LC filter and resonant at 8 GHz frequency to increase the conversion gain and boost the voltage headroom by reducing the voltage drop across the transistor loads.

Fig. 10 shows the simulated gain difference (GD) as well as phase difference (PD) versus frequency. The proposed balun provides gain and phase imbalance within only 0.5 dB and 3° over the frequency band of 23.5 to 24.5 GHz, respectively.

The S-D balun has been directly utilized after the local oscillation generator for stimulation of the I mixers as well as utilized after frequency divider to convert single-ended balun to double structure for the Q mixers in the proposed receiver frontend architecture.

Finally, in order to enhance the integrity of the whole

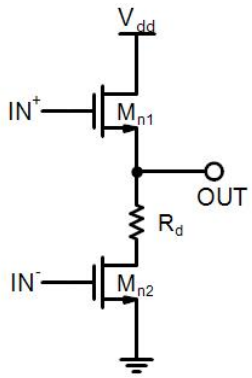

Fig. 11. Circuit schematic of the output differential- to single-ended balun.

Table 1. Circuit parameters of LNA and mixers

LNA	
M_n	72 μm/0.18 μm
M_p	24 μm/0.18 μm
L_g	0.3 nH
L_s	0.25 nH
L_x	0.85 nH
IF Mixer	
M_{P1}, M_{P2}	20 μm/0.18 μm
R_{LP}	5 kΩ
Baseband Mixer	
M_{n1}, M_{n2}, M_{n3}, M_{n4}	22 μm/0.18 μm
R_{Ln}	0.3 kΩ

circuit, an active balun is designed and used at the output ports of mixer stage. This balun converts the differential-ended mixer outputs to single-ended output (D-S) which can be connected to next stage without off-chip equipment. Fig. 11 illustrates the push-pull balun composed of both common-source and common-drain configurations with advantages of low power consumption and good isolation. Resistor, R_d is inserted to provide 50-Ω IF output impedance matching for down-conversion mixer. The signal gain of D-S balun is the sum of the two signal path gains [21]. Therefore, the D-S balun functions as a buffer and differential- to single-ended converter, simultaneously.

IV. RESULTS AND CONSIDERATIONS

The Proposed 24 GHz receiver frontend is designed and simulated in 130-nm TSMC CMOS process. The receiver frontend parameters are tabulated in Tables 1 and 2.

Table 2. Circuit parameters of divider and baluns

Divider	
M_{n1}	0.3μm/0.18 μm
M_{n2} , M_{n3}	3 μm/0.18 μm
M_{P1}	1.54 μm/0.18 μm
M_{P2}	2 μm/0.18 μm
M_{P3}	3.54 μm/0.18 μm
S-D Balun	
M_n	9 μm/0.18 μm
M_p	18 μm/0.18 μm
L_n	7 nH
L_p	8 nH
D-S Balun	
M_{n1}	20 μm/0.18 μm
M_{n2}	7 μm/0.18 μm
R_d	0.6 kΩ

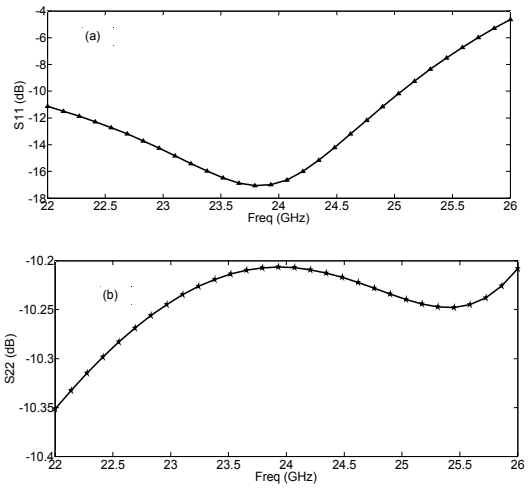

Fig. 12. Reflection coefficient of the proposed frontend versus RF frequency (a) Input return loss (S_{11}), (b) Output return loss (S_{22}).

The simulation is done at 1.5 V with dc current of 4.33 mA. The input and output reflection coefficients, S_{11} and S_{22}, are illustrated in Fig. 12 exhibiting a value better than -10 dB within the entire frequency range. The RF input port and the IF output port are well matched at their respective frequencies. For input impedance matching, the gate inductance (L_g), NMOS source inductance (L_s) and parasitic capacitance of NMOS and PMOS transistors form a multiselection LC ladder to achieve desired input return loss (e.g. S_{11}<-10 dB).

The second stage of the proposed frontend is mixer that realized in I/Q structure to convert RF frequency to baseband frequency. Firstly, high frequency is translated to IF frequency by utilizing single balanced mixer type. This single balanced switch adopts PMOS transistors to increase the linearity and voltage headroom, and hence to reduce power consumption. Furthermore, this switch mixer is realized in folded cascode topology and does not need independent biasing circuit. A double balanced Gilbert cell mixer is designed to translate IF frequency to baseband frequency. The whole transistors in mixer stage (second stage of the frontend receiver) are biased in subthreshold region to reduce the power consumption. Since transistors in mixer stage consume low power from the voltage supply, the voltage drop across the mixer loads are small and large resistors can be used in the output port of both mixers. Therefore, these large resistors lead increasing conversion gain of the receiver.

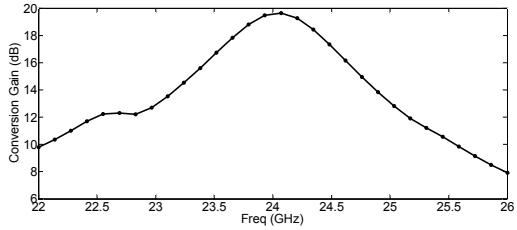

Fig. 13. Conversion gain versus RF frequency with 24-GHz LO signal.

A single- to differential-ended (S-D) balun is exploited at the output port of LO signal generator for the sake of stimulating mixer transistors. An active on-chip differential- to single-ended (D-S) balun is also adopted to simulate the conversion gain of the whole circuit that is shown in Fig. 13. The simulation exhibits that a 19.6-dB maximum power gain appears for a 24 GHz. The D-S balun also functions as a buffer which provides 50-Ω impedance for the output, and the matching result is shown in Fig. 12(b) (i.e. S_{22}<-10 dB). Both of the active baluns adopt cascode configuration to reduce the power consumption. Although, S-D balun exploits two inductors in the output ports, but it provides approximately identical and out-of-phase signals which are suitable for proposed receiver. Additionally, these active and on-chip baluns increase the integrity level of the receiver frontend.

Fig. 14 depicts that the proposed frontend features a low *NF* of 3 dB at the operation frequency of 24 GHz.

With the nature of cascading stages, the linearity of the receiver frontend mainly depends on the LNA and mixer. In this study, the complementary push-pull topology is adopted in the LNA stage for the improvement of gain compression and third-order intercept point (*IIP3*).

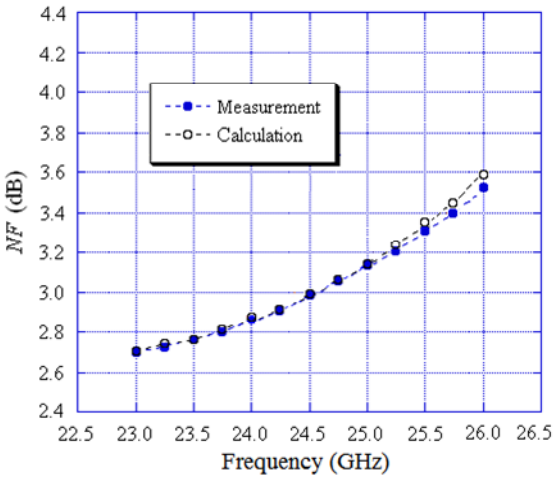

Fig. 14. Total noise figure (NF) of the proposed frontend versus RF frequency.

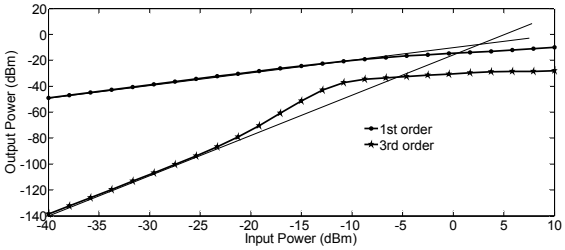

Fig. 15. IIP3 of the proposed frontend versus RF power.

Table 3. Comparison of the results of the proposed receiver frontend and other published works

Ref.	[5]	[6]	[16]	[22]	**This work**
Tech (nm)	180	180	130	SiGe HBT	130
Freq (GHz)	24	24	1.575	0	24
Conversion gain (CG) (dB)	28.4	27.5	42.5	21.7	19.6
NF (dB)	6	7.7	6.2	10.2	3
Power(mW)	54	43	0.586	595	6.5
IIP3 (dBm)	-13	-23[a]	-35	-35[a]	3

[a] P_{1dB}

Alternatively, the desirable circuit linearity is achieved by optimizing the device size and bias condition of this particular design. The IIP3 versus input RF power is illustrated in Fig. 15. The simulation illustrates *IIP3* of 3 dBm for the proposed frontend.

In the end, the performance summary of the proposed receiver frontend and comparison with other high-linear published works are shown in Table 3. As can be seen, the proposed receiver frontend performs very well in linearity and power consumption terms.

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V. CONCLUSIONS

A single-ended receiver frontend has been presented for 24-GHz automotive radar. By integrating the two-stage LNA and downconversion mixers, the frontend has been designed in 130-nm CMOS technology. The LNA stage was adopted complemenptary push-pull (CPP) topology to boost the gain and the linearity of whole circuit. Meanwhile, the LNA was realized in folded configuration to reduce power supply and to increase voltage headroom. The frontend was realized in IF-DCR architecture to increase integration level and alleviate the DCR problems. Two active baluns were also designed to increase the integrity of the frontend. Furthermore, the switch transistors were biased in subthreshold region to reduce the power consumption. The proposed receiver frontend showed conversion gain of 19.6 dB, *NF* of 3 dB, *IIP3* of 3 dBm and power dissipation of 6.5 mW.

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