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Seamless Transfer of Single-Phase Utility Interactive Inverters with a Synchronized Output Regulation Strategy

Ji Xiang†, Feifan Ji*, Heng Nian*, Junming Zhang*, and Hongqiao Deng*

†,*Department of System Science and Engineering, College of Electrical Engineering, Zhejiang University, Hangzhou, China

Abstract

This study presents a strategy using the synchronized output regulation method (SOR) for controlling inverters operating in stand-alone and grid-connected modes. From the view point of networked dynamic systems, SOR involves nodes with outputs that are synchronized but also display a desirable wave shape. Under the SOR strategy, the inverter and grid are treated as two nodes that comprise a simple network. These two nodes work independently under the stand-alone mode. An intermediate mode, here is named the synchronization mode, is emphasized because the transition from the stand-alone mode to the grid-connected mode can be dealt as a standard SOR problem. In the grid-connected mode, the inverter operates in an independent way, in which the voltage reference changes for generalized synchronization where its output current satisfies the required power injection. Such a relatively independent design leads to a seamless transfer between operation modes. The closed-loop system is analyzed in the state space on the basis of the output regulation theory, which improves the robustness of the design. Simulations and experiments are performed to verify the proposed control strategy.

Key words: Microgrid, Seamless transfer, Single-phase inverter, Synchronized output regulation

I. INTRODUCTION

Concerns for the environment and the scarcity of fossil fuel reserves have brought increasing attention to renewable energy sources. Distributed generation (DG), referring to generation plants connected to a distribution system, is a method for integrating renewable sources and distribution systems; this method also meets the need to produce energy that matches the demand and reduces the losses during energy delivery [1]. DG units, acting as renewable energy sources are often implemented using an inverter-based interface [2], which is connected to the grid to transfer energy in the grid-connected (GC) mode and to supply the local load when faults occur in the stand-alone (SA) mode. The control method for inverters should be changed according to the different working modes. A fast and smooth transition between the modes, which has emerged as an important issue in recent years, helps to prevent sudden voltage changes across critical local loads or any sudden current changes to the grid [3].

Under the GC mode, inverters control the current to provide the grid with a current that matches the required active and reactive powers. Generally, the current control for grid-connected three-phase inverters under a balanced grid situation is not difficult; and a method to achieve this was reported in [5]. In recent years, model predictive control for the current control of three-phase inverters [6]-[11] has received an increasing amount of attention. Current control for single-phase systems typically involves a proportional-resonant (PR) controller [12], [13] or a proportional-integral controller after a dq transformation [14]. In the SA mode, inverters control the voltage to energize the load. This conventional DC-AC inverter control emerges in the control of UPSs and driving AC motors. Generally, an outer voltage control loop provides the current command, for which an inner current control loop pursuing a fast response is made [15]. The harmonics are suppressed by the internal

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†Corresponding Author: jxiang@zju.edu.cn
Tel: +86-571-8795-2653, Zhejiang University
*Department of System Science and Engineering, College of Electrical Engineering, Zhejiang University, China

model control and the repetitive control methods [16], [17].

Another mode occurring in the transition from the SA to the GC is the synchronization mode. In this mode, the inverter aims to synchronize the output voltage of the point of common coupling (PCC) with the grid voltage. This synchronization is vital for connections to the utility. When the grid is under abnormal conditions, the inverter switches from the GC mode to the SA mode directly. Islanding detection is critical for determining the proper mode for an inverter [18], [19].

A seamless transfer is desirable in the transition between the 3 different operating modes. A seamless transfer algorithm can switch the inverter operations from the voltage control mode to the current control mode, and vice versa, with a minimum of interruption to the local load and grid [20]. In the cited study, the transfer steps between the GC and the SA modes are presented. However, the controller designs are not issued. During the transition from the GA to the SA mode, grid disconnection occurs at the instant of zero current and may last for half of a line frequency cycle. A method called intentional voltage control was proposed in [21] to hasten this disconnection process. In this case, the grid current reaches zero several milliseconds after the detection of a grid fault. A method for changing the reference voltage was proposed for the seamless transfer of a single-phase inverter [22] to ensure the controller output invariance during mode transfer. Indirect current control methods were presented in [23] and [24] for single-phase and three-phase inverters, respectively. The control strategy proposed in [25] reduces the over-voltage stress of renewable energy and critical loads under grid faults. The proposed controllers are composed of an outer current control loop and an inner voltage control loop. The outer current control loop stops in the SA mode and provides the voltage reference in the GC mode. In such a case, the inverter always works in the voltage control mode to ensure a seamless transfer. However, a direct analysis of the stability and performance, as well as a systematic synthesis method for the controllers, is still lacking because of factors such as the nonlinear calculations involved. These nonlinear factors were recently relaxed [26]. In [27], an improved indirect current control method was presented for three-phase inverters [27], and an inner capacitance current loop was introduced to widen the bandwidth of the voltage control loop. This work also conducted a comprehensive analysis of the steady and transient states in the frequency domain. A PLL-based seamless transfer method was presented for three-phase inverters [28]. The PLL was used for the synchronization mode and for holding the initial angle invariant at the beginning of the SA mode. A damping resistor was added in the capacitance branch of the LCL filter to enhance stability. Recently, uniform controllers for both the GC and SA modes based on robust μ-synthesis and model predictive control were presented in [29] and [30]. However, these works did not address the mode transfer.

A brief version of the current paper was presented at IEEE CDC 2015 [36]. For this study, numerous improvements have been made, including the following: a detailed design concept of a single-phase PLL is presented, the effects of an internal model controller on the inner loop are illustrated, and simulation results are presented on the MATLAB/Simulink platform, along with the results of a comparative experiment.

In this paper, a design method for the seamless transfer of single-phase inverters is presented, in which the viewpoint of SOR is applied. SOR is aimed at synchronizing the outputs of a network of agents and manifesting the target dynamics [31]. A whole single-phase plant can be treated as a network containing two nodes: the inverter and the grid. In the SA mode, the inverter operates on its own and outputs a sinusoid voltage to the load. In the GC mode, the inverter operates in the SOR case and outputs a voltage for the load, which is synchronized with the utility in a generalized sense so that the injecting current converges to an expected value.

The idea behind SOR is to adjust the output reference of the inverter (node) according to synchronization errors (such as current tracking errors) instead of directly changing the inverter controller. The same idea was adopted in [22] and [24]. However, the proposed SOR-based controller design offers three important advantages. 1) The model-based design provides a rigorous analysis of the stability and tracking performance. An internal model principle for output regulation, which ensures a high design robustness without requiring exact knowledge of the grid inductance parameters, was necessary in the decoupled current control in previous studies. 2) The inverter is relatively independent. This independence motivates stopping the PLL in the SA mode, which avoids the tracking phase of faulty grids. 3) The design method is scalable and is easily extended to networks with multiple inverters, such as microgrids. Moreover, the proposed controller is simple. It involves only two feedback scalar gains. However, a complex controller is permitted to improve the controller performance, involving more parameters.

The remainder of this paper is organized as follows. The system description is presented in Section II, along with the network perspective of the inverter plant and models of the three working modes. The designed seamless transfer controller based on SOR is described in Section III. Simulation results from the MATLAB/Simulink platform are illustrated in Section IV, followed by a scaled-down experiment in Section V. Conclusions are discussed in Section VI.

II. SYSTEM DESCRIPTIONS

The topology of a single-phase utility connected inverter is shown in Fig. 1. It shows a single-phase full-bridge voltage

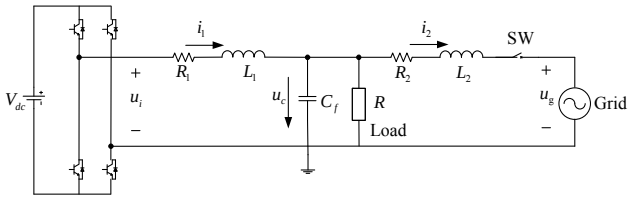

Fig. 1. Circuit diagram of a single-phase utility interactive inverter connected to a critical load and the grid [36].

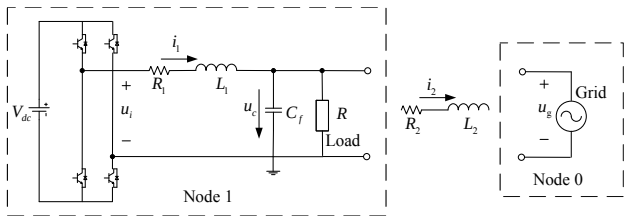

Fig. 2. Perspective from the viewpoint of a network [36].

source inverter (VSI) driven by a DC source, with an LC filter, connected to a load. It also connects to the utility via an extra inductance for harmonic suppression. A switch (SW) is located between the inductance and the grid. The inverter transmits power from the DC source into the utility power when the SW is activated in the GC mode. When the SW is deactivated, the inverter supplies the power of the DC source for critical loads in the SA mode.

A. Perspective for Two Nodes

The plant to be studied can be treated as a network system consisting of two nodes: the grid and the VSI with an LC filter. An inductance and a switch connect the nodes together, as shown in Fig. 2. The grid, designated as node 0, has an output of u_g, which is the grid voltage. The VSI, designated as node 1, has an output of u_c, which is the voltage of the filter capacitance. In any operating mode, the outputs of both nodes manifest the required sinusoids.

When the two nodes are connected, their outputs should be synchronized in advance to avoid overcurrent at the connecting moment. This SOR problem was studied in [31] and [32]. It requires the outputs of all of the nodes to be regulated and synchronized to track a given waveform (sinusoids in this case) and achieve a "cooperative output regulation." One way to solve the SOR problem is by using the output regulation method to track the reference signal and then synchronize the reference signals through the errors' feedback. The control of the currents or voltages of a VSI with an output regulation method was reported [16].

In the present work, the SOR strategy is applied to deal with the synchronization transition process before the connection moment of the VSI to the utility. It is also used to control the GC mode and the SA mode. This strategy provides the controller with a constant structure for the different modes to realize a seamless transfer of the plant as shown in Fig. 1.

Another merit of the SOR strategy is the treatment of the generation unit as a relatively independent node with a distributed controller. The result is scalable and can be extended to microgrids. This study considers three operating modes, which are described below.

B. Stand-Alone (SA) Mode

The switch is open in the SA mode. Node 1 simply supplies power to the local load. In this study, the VSI connects to the load through an LC filter, and the voltage is that of the filter capacitor. The dynamic model for node 1 is:

$$\frac{di_1}{dt} = -\frac{R_1}{L_1} i_1 + \frac{1}{L_1}(u_i - u_c) \tag{1a}$$

$$\frac{du_c}{dt} = -\frac{1}{RC_f} u_c + \frac{1}{C_f}(i_1 - i_2) \tag{1b}$$

where i_1 and i_2 are the inductances' currents, u_c is the capacitor's voltage, and u_i is the input of the LC filter which is treated as the equivalent output voltage of the inverter. In the SA mode, $i_2 = 0$. i_2 remains in the dynamic model to maintain consistency for the following GC mode. The reference u_r to be tracked by u_c is a sinusoid wave with a rated RMS equal to V_r and an angle frequency of w_n . u_r can be modeled by:

$$\dot{\eta}_u = \begin{bmatrix} 0 & w_n \\ -w_n & 0 \end{bmatrix} \eta_u, \quad u_r = \sqrt{2} V_r \begin{bmatrix} 1 & 0 \end{bmatrix} \eta_u, \tag{2}$$

where $\eta_u \in \Re^2$, and the initial condition is $\eta_u(0) \in \Omega \triangleq \{x \in \Re^2 : x^T x = 1\}$. In the output regulation theory, the above is an exosystem that produces reference signals. The controller for the SA mode aims to make $e_u = u_c - u_r \to 0$.

C. Synchronization Mode

When the SW is going to be turn on, the voltages on both sides of the switch should be synchronized in advance. In this mode, the dynamics of node 1 and those in the SA mode are the same. However, the goal is changed to make $e_g = u_c - u_g \to 0$, where u_g denotes the grid voltage and is defined as:

$$\dot{\eta}_g = \begin{bmatrix} 0 & w_n \\ -w_n & 0 \end{bmatrix} \eta_g, \quad \text{with} \quad \eta_g(0) = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$
$$u_g = \sqrt{2} U_g \begin{bmatrix} 1 & 0 \end{bmatrix} \eta_g \tag{3}$$

in which $\eta_g \in \Re^2$ and the voltage U_g denotes the RMS value of the voltage of the grid.

To hold the controller invariant with respect to the one in the SA mode, according to the solution of the SOR problem, $e_g \to 0$ is indirectly realized by adopting the dynamics of the exosystem η_u so that $u_r \to u_g$.

When synchronization is achieved, $\| u_c - u_g \| \le T_e$ for the threshold value T_e , SW is turned on, and node 1

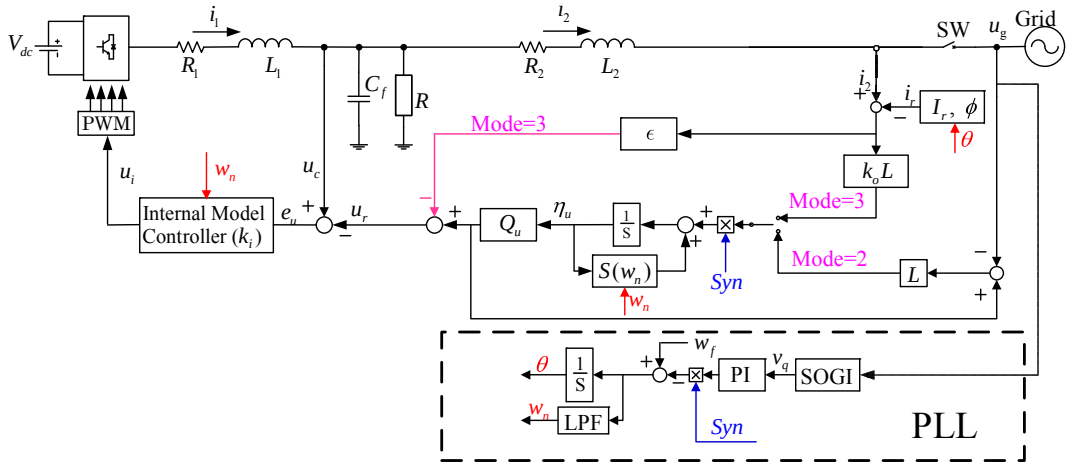

Fig. 3. Block diagram of the proposed controller, as well as the adopted PLL. The definitions of the selection signals Mode and Syn are detailed in Table I [36].

changes its mode to the GC. Note that the synchronization mode only occurs when the inverter going to change to the GC mode from the SA mode. In the reverse transient process that often occurs during grid faults, the SW needs to be deactivated as quickly as possible.

D. Grid-Connected (GC) Mode

In this mode, the SW is closed, and node 1 provides the grid with the desired current and it supplies power for the local load. The phase angle of the grid voltage is set to zero, that is, $\vec{u}_g = U_g \angle 0$. In addition, the reference current i_r, which is tracked by i_2, is given by $\vec{i}_r = I_r \angle \phi$, where I_r represents the RMS value and ϕ represents the phase angle. Similar to u_r, i_r is defined by:

$$\dot{\eta}_i = \begin{bmatrix} 0 & w_n \\ -w_n & 0 \end{bmatrix} \eta_i, \quad \text{with} \quad \eta_i(0) = \begin{bmatrix} \cos\phi \\ \sin\phi \end{bmatrix} \tag{4}$$
$$i_r = \sqrt{2} I_r \begin{bmatrix} 1 & 0 \end{bmatrix} \eta_i$$

where $\eta_i \in \Re^2$ is the state. The requirement of the phase angle is influenced by the initial conditions $\eta_i(0)$ and $\eta_g(0)$ in (3). Note that both η_g and η_i are only used for the theoretical analysis and are not needed for the controller design.

In this mode, the dynamic model of node 1 is invariant with augmented dynamics of i_2:

$$\frac{di_2}{dt} = -\frac{R_2}{L_2} i_2 + \frac{1}{L_2}(u_c - u_g). \tag{5}$$

The aim of the controller for the GC mode is to realize that $e_i = i_2 - i_r \to 0$. Similarly, the controller is held invariant by adjusting the exosystem η_u indirectly.

III. Controller Design

The controller structure is shown in Fig. 3, where the controller is divided into two parts. These parts are the inner voltage control loop and the outer current control loop. "Mode" denotes the three different modes of the study case (Table I). The outer loop is a simple integrated feedback, the gain k_0 of which is to be determined. This loop works for the GC mode (Mode=3) and the synchronization mode (Mode=2).

TABLE I
Values of Selection Signals and the Switch in the Various Operation Modes [36]

	Stand-alone	Synchronization	Grid-connected
Mode	1	2	3
Syn	0	1	1
SW	0	0	1

The outer loop operates under the current control mode when Mode = 3. The reference voltage η_u is regulated by the current tracking error e_i. The reference η_u is adjusted for asymptotically tracking the grid voltage u_g when Mode=2.

When the inverter works under Mode=1, only the inner voltage control loop is operating. When Syn=0, the output of the integrator is made constant, as is η_u, which is measured by scalar $\frac{V^*}{\| \eta_u \|}$ to ensure the voltage provide to the local loads. The peak value of the rated voltage is denoted by V^*. The zero Syn shuts down the PLL. w_0, i.e., the reference frequency is the nominal one, w_f. The reference voltage, at the instant of the transition from the GC to the SA mode, shows an invariant phase but rotates at a nominal speed. As a result, the transfer from the GC mode to the SA mode is smooth, and the minimization of the deterioration is achieved.

The proposed design solves the SOR problem by adjusting the reference voltage to allow the controller to adapt to

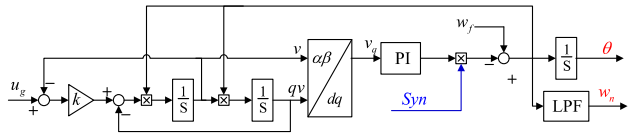

Fig. 4. Block structure of single-phase PLL.

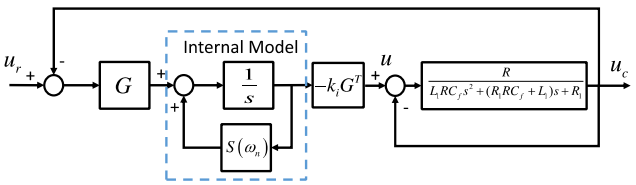

Fig. 5. Block diagram of the internal model controller for the inner loop.

different modes. This adjustment does not influence the design of the inner voltage control loop. Hence, different feedback gains do not need to be designed for the different modes.

Moreover, the controller shows a uniform structure for the different modes. The controller is concise, since only two parameters k_o and k_i need to be designed (Fig. 3) for the outer loop controller and the inner loop controller, respectively. The parameter ϵ is used to enhance the damping of the output loop, and it may be removed in the presence of R_2, as demonstrated in the following.

A. PLL

In practice, the frequency of the utility is not fixed but fluctuates around the rated frequency. Thus, the PLL circuits or algorithm should obtain the utility frequency and phase angle necessary for synchronization and the GC mode. A single-phase PLL that is based on a second-order generalized integrator (Fig. 4) is adopted.

The PLL has outputs θ and w_n. For the former, $u_g(t)=\sqrt{2}U_g\cos\theta(t)$, from which a desired current in the GC mode can be obtained by:

$$i_r=\sqrt{2}I_r\cos(\theta(t)+\phi)=\sqrt{2}I_r(\cos\theta(t)\cos\phi-\sin\theta(t)\sin\phi). \quad (6)$$

The angle frequency w_n used for the artificial exosystem of node 1 is used to build the internal model controller. A low pass filter is introduced to make ω_n vary slowly which allows ω_n to be approximated as a constant scalar in the theoretical analysis.

In the SA mode, a zero signal Syn ceases the PLL. Subsequently, node 1 works independently with $w_n=w_f$, which represents the rated line angle frequency.

B. Internal Model Controller for the Inner Loop

The inner loop controller, whose structure is illustrated in Fig. 5, is based on the internal model principle.

Note that i_2, which is treated as a disturbance to node 1, comes from the same dynamic mode as that for u_r, the reference voltage. The internal model to be embedded in the controller is the same as that in (2). The dynamic controller shows the form:

$$\dot{z}=S(w_n)z+Ge_u,\quad u_i=-k_iG^Tz \quad (7)$$

where $S(w_n)=\begin{bmatrix}0 & w_n\\ -w_n & 0\end{bmatrix}$. Since any nonzero G may be used for the controllability of pair (S,G), G can be selected as any vector. k_i is a positive scalar that acts as a tuning parameter. The utility of the dual G and G^T design is to provide passivity to the controller (7). With this controller, the closed loop system in the SA mode is described as:

$$\begin{cases}\dot{x}_i &= A_ux_i-k_iB_uG^Tz_i\\ \dot{z} &= S(w_n)z+G(C_ux_i-Q_u\eta_u)\\ \dot{\eta}_u &= S(w_n)\eta_u\end{cases} \quad (8)$$

where $x_i=[i_1,u_c]^T$ and:

$$A_u=\begin{bmatrix}-\frac{R_1}{L_1} & -\frac{1}{L_1}\\ \frac{1}{C_f} & -\frac{1}{C_fR}\end{bmatrix},\quad B_u=\begin{bmatrix}\frac{1}{L_1}\\ 0\end{bmatrix}$$

$$C_u=\begin{bmatrix}0 & 1\end{bmatrix},\quad Q_u=\begin{bmatrix}\sqrt{2}V_r & 0\end{bmatrix}$$

The following result is directly obtained from the output regulation theory [33].

Theorem 1: If the feedback scalar k_i is such that the following matrix:

$$A_{in}=\begin{bmatrix}A_u & -k_iB_uG^T\\ GC_u & S(w_n)\end{bmatrix} \quad (9)$$

is a Hurwitz, then the voltage tracking error e_u exponentially converges to zero under the controller (7).

Normally, the voltage of the VSI comprises harmonic components. According to the SOR theory, the harmonic components can be treated as disturbances. The disturbances can be rejected by designing $S(\omega_n)$ with the corresponding internal models.

C. Outer Loop Design

1) Synchronization mode: In the synchronization mode, the dynamics of node 1 are the same as those in the SA mode, except the dynamics of the exosystem η_u become:

$$\dot{\eta}_u=S(w_n)\eta_u+L(u_r-u_g). \quad (10)$$

where $L\in\Re^2$ is a vector to be determined. Evidently, the feedback term in the above system leads $u_r\to u_g$, which is ensured by the results as follows.

Lemma 1: Assume that $u_g=Q_g\eta_g$ for some row vector $Q_g\in\Re^2$. If L is such a vector that $S(w_n)+LQ_u$ is a

Hurwitz, then $u_r - u_g$ exponentially converges to zero for any Q_g.

Proof: There are two scalars b_1 and b_2 such that $Q_g = b_1 e^{S(w_n)b_2} Q_u$ for any Q_g. Define $\eta'_g = b_1 e^{S(w_n)b_2}\eta_g$. Then, $\dot{\eta}'_g = S(w_n)\eta'_g$ and $u_g = Q_u\eta'_g$. Noting that (10) is an observer of the system η'_g, $u_r - u_g \to 0$, with $S(w_n) + LQ_u$ being a Hurwitz.

The dynamics of η_u in (10) are independent of those of the inner loop. The closed loop system in the synchronization mode is a cascaded connection of two exponential systems. Hence, the following result can be obtained.

Theorem 2: If k_i and L are such that A_{in} and $S(w_n) + LQ_u$ are a Hurwitz, then u_c exponentially converges to zero under a controller consisting of (7) and (10).

The matrix L is the feedback gain of an observer, on the basis of which the optimal design can be applied. In this work, the gain is given by:

$$L = -XQ_u^T \tag{11}$$

where X is the solution of the ARE:

$$XS(w_f) + S(w_f)^T X - XQ_u^T Q_u X + I = 0 \tag{12}$$

The nominal model of the exosystem $S(w_f)$ is used instead of the real-time $S(w_n)$. As previously explained, the above solution achieves the largest robustness with respect to the uncertainties of $S(w_f)$ [34].

2) GC mode: In this mode, the dynamics of the exosystem η_u and the reference voltage u_r become:

$$\dot{\eta}_u = S(w_n)\eta_u + k_o L e_i, \quad u_r = Q_u\eta_u - \epsilon e_i. \tag{13}$$

where L is as same as the one in (11), with a scalar k_o as the regulating parameter to be designed, and a positive scalar ϵ can be treated as the virtual resistance of L_2 branch. The current error feedback changes the exosystem dynamics η_u until the reference voltage produced by the exosystem is such that $e_i = 0$. A damping term ϵe_i is added to regulate the convergence rate of the current control differently than the reference voltage in (2). In practice, this may be zero if a large R_2 exists.

In this case, the analysis of the closed loop system is more difficult than that of the other two modes since the dynamics of node 1 and the reference voltage η_u are coupled via the nonzero current i_2 and especially due to the fact that the proposed design is based on holding the inner loop invariant and not on redesigning a current controller. This is the essential idea of the SOR. The VSI is treated as a node with an inner structure that cannot be altered. It is only possible to revise the commands or the reference voltage.

In this mode, the closed loop system shows the following form:

$$\begin{cases} \dot{x}_i &= A_u x_i - k_i B_u G^T z_i \\ \dot{z} &= S(w_n)z + G(C_u x_i - Q_u\eta_u) + \epsilon G(i_2 - i_r) \\ \dot{i}_2 &= \dfrac{1}{L_2}C_u x_i - \dfrac{R_2}{L_2}i_2 - \dfrac{1}{L_2}u_g \\ \dot{\eta}_u &= S(w_n)\eta_u + k_o L(i_2 - i_r) \end{cases} \tag{14}$$

In this study the flowing are defined $x_o = [x_i^T, z, i_2]^T$ and $w_o = [\eta_g^T, \eta_i^T]^T$. The above system can be rewritten in a compact form as follows, which is a standard method in output regulation theory.

$$\begin{cases} \dot{x}_o = A_o x_o + B_o(-Q_u\eta_u) + P_o w_o \\ \dot{w}_o = S_o w_o \\ \dot{\eta}_u = S(w_n)\eta_u + k_o L(C_o x_o - Q_o w_o) \end{cases} \tag{15}$$

where:

$$A_o = \begin{bmatrix} A_u & -k_i B_u G^T & 0 \\ GC_u & S(w_n) & \epsilon G \\ \dfrac{1}{L_2}C_u & 0 & -\dfrac{R_2}{L_2} \end{bmatrix}, \quad B_o = \begin{bmatrix} 0 \\ G \\ 0 \end{bmatrix},$$

$$P_o = \begin{bmatrix} 0 & 0 \\ -\epsilon G\sqrt{2}I_r[1,0] & 0 \\ 0 & -\dfrac{1}{L_2}\sqrt{2}U_g[1,0] \\ 0 & 0 \end{bmatrix}$$

$$S_o = \begin{bmatrix} S(w_n) & 0 \\ 0 & S(w_n) \end{bmatrix},$$

$$C_o = \begin{bmatrix} 0_{1\times 4} & 1 \end{bmatrix}, \quad Q_o = \begin{bmatrix} \sqrt{2}I_r & 0_{1\times 3} \end{bmatrix}$$

Theorem 3: If k_o is such that $A_{ou} = \begin{bmatrix} A_o & -B_o Q_u \\ k_o LC_o & S(w_n) \end{bmatrix}$ is a Hurwitz, then the current tracking error e_i exponentially converges to zero under a controller consisting of (7) and (13).

D. Mode Transfer Sequence

The steps of the mode transfer process under the proposed controller (Fig. 3) are illustrated as follows.

Transfer from the grid-connected mode to the stand-alone mode

1) Detect a fault on the grid.
2) Set the signal Syn=0.
3) Provide a switch-off signal to the switch SW.
4) Set Mode=1 to switch the operating mode of the controller to the stand-alone mode.

This sequence shows that the controller gains and the

TABLE II
ELECTRICAL PARAMETERS OF THE STUDIED PLANT

R_1	L_1	R_2	L_2	C_f	R	V_r
0.5Ω	$1mH$	0.3Ω	$2mH$	$10\mu F$	10Ω	$220V$

controller commands are unchanged in the transfer process from the grid-connected to the stand-alone mode. In previous studies, the PLL locks on the phase of the capacitor voltage, which requires an extra step to gradually change the voltage reference. However, this is unnecessary in this paper.

If Syn=0, neither the PLL nor the outer loop will work, since the former indicates that the frame of the synchronization reference is rotating at the nominal speed, ω_f, while the latter indicates that the voltage reference η_u maintains its phase when Syn is changed from 1 to 0.

The reverse transfer process is complex and challenging since it should experience an intermediate synchronization mode.

Transfer from the stand-alone to the grid-connected mode

1) Detect the grid recovery.
2) Set Mode=2 and detect errors $u_c - u_g$ of the synchronization.
3) Set Syn=1 to unlock the PLL and the outer loop.
4) If $\| u_c - u_g \|$ is less than the threshold values set before the three periods, then turn on the switch SW.
5) Set Mode=3, and switch the operating mode of the controller to the GC mode.

In the transfer process with a transition, the controller gains have yet to be altered. Changes occur on the controller commands when Syn changes to 1 or when the Mode changes from 2 to 3. The switch of Syn does not cause a jump of the output angle θ of the PLL or a jump of the input u_i, since only integrators exist in the channel from the signal Syn to θ and u_i without any proportional gains.

E. Parameter Design

The proposed method only requires two designed scalar parameters, k_i and k_o. Their designs are decoupled, since k_o can be selected after k_i, which is independent of k_o. If k_i and k_o are zero, then A_{in} and A_{ou} are critically stable, and the solutions of k_i and k_o always make A_{in} and A_{ou} a Hurwitz, respectively. The root locus analysis method is preferred for the scalar feedback gain design.

The electrical parameters are given in Table II. The inner loop gain k_i is designed first. Fig. 6 shows the root locus of A_{in} with $G=[3,-1]^T$. The start point $k_i=0$ has two pair of complex eigenvalues from $S(w_n)$ located on the imaginary axis. As k_i increases, they tend to move to the left and then converge to negative infinity and the origin zero, respectively, after $k_i > 62$. The other pair eigenvalues from A_{in} tends to move to the right and then crosses the imaginary axis after $k_i > 1040$. In this study, $k_i = 500$ is selected.

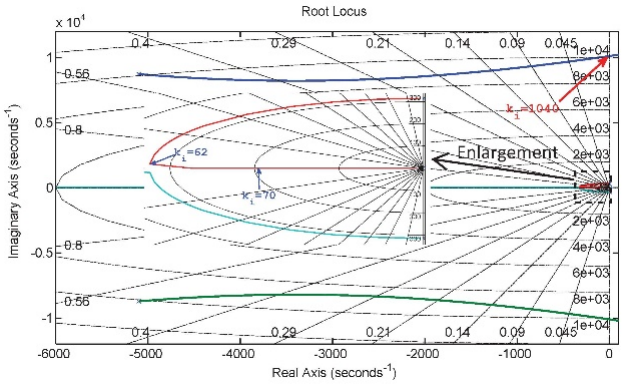

Fig. 6. Root locus of A_{in} as k_i varies.

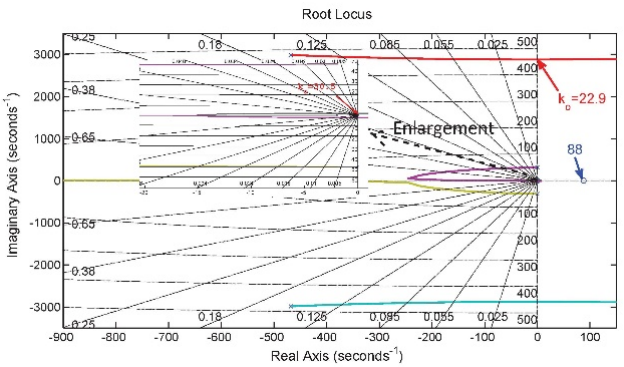

Fig. 7. Part root locus of A_{ou} as k_o varies.

For the design of k_o, $\epsilon = 1$ is selected and $L=[-1.36, 0.38]^T$ is calculated by (11). If $k_i = 500$, then the root locus of A_{ou} is shown in Fig. 7 with the rightmost pair complex eigenvalues $-4700 \pm 8000j$ −4700 ± 8000j omitted. These eigenvalues are almost fixed when k_o varies. Except for the origin zero, an extra zero is located at the right half real axis. The largest allowable value of k_o is 22.9. $k_o = 2.5$ is selected for the simulation.

F. Robustness Analysis

From the theoretical point of view of the control, the output regulation design, based on the internal model principle, offers robustness to the output tracking problem. The essence of the robustness here is that the no-bias output tracking problem is converted into a stabilization problem for an augmented linear system. When A_{ou} remains a Hurwitz under a certain perturbation of the parameters, the output performance is unchanged. The real stability radius of A_{ou},

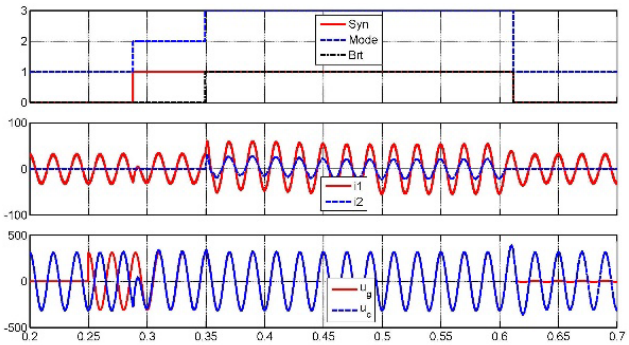

Fig. 8. Complete simulation process.

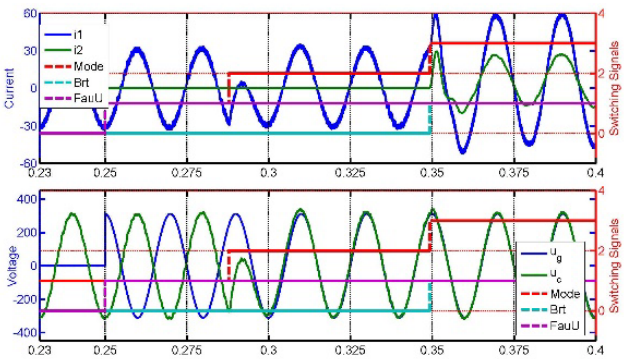

Fig. 9. Transition from stand-alone mode to grid-connected mode. Brt is the switch signal for the circuit break, and FauU is the switch signal for the utility fault.

denoted as r stab, is often used as the maximum size of the perturbation under which the system maintains stability [4]. Here, it is calculated as $ratab = 2.44$ and $\frac{1}{rstab} \approx 41\%$. Hence, A_{ou} remains stable for any electrical parameter perturbation with a size of 41% or less.

IV. Simulation Example

A simulation using the above parameters is performed in the MATLAB/Simulink environment to verify the developed controllers. In the simulation, the constant DC source is 400 V, the voltage of the single-phase utility grid is 220 V at 50 Hz, and the switching frequency of the inverter is 6 kHz. In the GC mode, the inverter energizes the local load and transfers energy to the utility. The desired current injected to the utility is $I_r = 15\angle\phi$ with $\phi = 10 * \pi / 180$. The local load has a resistance of 10Ω.

The simulation process is shown in Fig. 8. In the first phase, from 0 ms to 250 ms, the inverter operates in the SA mode and outputs the rated voltage to the local load. At 250 ms, the inverter detects the utility voltage. After two periods, the utility is confirmed to be normal, and the inverter enters the synchronization mode to close the circuit break at 287 ms. Once the synchronization error is less than a predefined threshold, the inverter switches to the GC mode at 350 ms. In

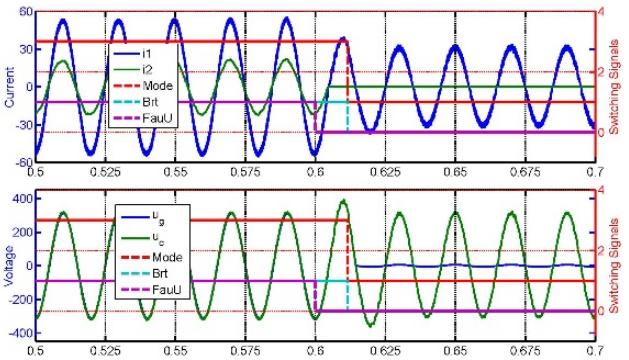

Fig. 10. Transition from grid-connected mode to stand-alone mode. Brt is the switch signal for the circuit break, and FauU is the switch signal for the utility fault.

the GC mode, the inverter injects the desired current to the utility. At 600 ms, the utility is broken. The inverter detects this unintentional islanding via phase-jump detection [35] and returns to the SA mode.

Fig. 9 shows an enlargement of the first mode transition from the SA mode to the GC mode. This transition is intentional and can be scheduled to be sufficiently smooth. However, a distortion of the load voltage arises at the beginning of the synchronization mode because of the required short synchronization process. As a result, the whole simulation can be finished in less than 1 s.

After two periods of synchronization, the inverter output is synchronized with the utility voltage, and the signal SW jumps to 1 to close the single-phase circuit break. Subsequently, the current i_2 injected to the utility rises, and the inverter enters the GC mode.

Fig. 10 is an enlargement of the mode transition from the GC mode to the SA mode. A utility fault occurs at 605 ms with a current of i_2=0. After the fault, u_c increases to a certain extent because of the detection time or the interval between fault occurrence and detection, during which the controller continues operating in the GC mode while $i_2 = 0$. As a result, the capacitance absorbs energy to be delivered to the utility so that its voltage rises. From this period, the true voltage is not the measured utility voltage u_g but the value of the capacitor voltage u_c. This characteristic is shown in Fig. 10, where u_g coincides with u_c until the single-phase circuit break deactivates. This coincidence is the main difficulty of islanding detection.

The controller detects the utility fault at 612 ms, after which the inverter switches to the SA mode. Fig. 10 shows that the load voltage u_c maintains a sinusoid waveform, except for an increasing magnitude in the short islanding detection phase. This seamless feature is caused by the phase of the reference voltage in the proposed controller being invariant during the switching time and the PLL not being used in the SA mode.

TABLE III
ELECTRICAL PARAMETERS OF THE HARDWARE [36]

R_1	L_1	R_2	L_2	C_f	R	V_r
0.5Ω	$0.8mH$	0.3Ω	$1mH$	$14.1\mu F$	60Ω	$30V$

TABLE IV
CONTROL PARAMETERS [36]

L	G	k_i	k_0
$[-1.4126,-0.0665]^T$	$[3,-1]^T$	48	1.3

V. EXPERIMENT

An experiment is designed to further verify the developed controller. Specifically, the experiment aims at verifying the seamless transition performance of the platform between different modes, whether from the SA mode to the synchronization mode, from the synchronization mode to the GC mode, or from the GC mode to the SA mode. The experimental hardware is shown in Fig. 13. The circuit topology of the hardware differs slightly from the simulated hardware. A tunable isolation transformer is added between the grid interface inductor and the grid in Fig. 1. Here, the ratio of the transformer is set to $30:220$ so that the inverter rated output voltage is AC 30 V. The voltage of the DC bus is 50 V. The parameters of the experimental hardware and the control algorithm are also different from those of the simulation, which are listed in Tables III and IV. As a result of practical limitations, some of the parameters of the real experimental platform are not the same as those of the simulation. The simulation accurately imitates high voltages and powers and can illustrate more information, as in the last section. The experiment highlights successful results in a real scaled platform.

A mechanical relay was selected as the grid connection switch. The switching frequency of the IGBTs is 20 kHz. In the SA mode, the switch is turned off, and the inverter converts DC 50 V to AC 30 V to provide energy for the local loads. When the switch is turned on under the GC mode, it supplies the local load and transfers 90 W active power to the utility via the transformer. The signal circuit is composed of a basic board and a control board. The signal circuit processes the sample signals from the voltage and current sensors in the power circuit and sends them to the controller. The control board contains a DSP28335 with peripheral circuits for the chip. The quality of the high-frequency switching signal is maintained by using fiber optic transmission between the signal circuit and the driving circuit of the inverter.

Fig. 12 illustrates the synchronization process that occurs during the transition from the SA mode to the synchronization mode. After the synchronization command (the falling edge of the purple waveform) is sent, the output voltage (the green waveform) reaches the grid voltage (the yellow waveform) within 80 ms. Once synchronization is achieved, the switch is deactivated, and the inverter operates in the GC mode with a mode change command (the falling edge of the purple waveform in Fig. 13). The current injected into the utility (the green waveform) reaches the reference in 100 ms. In Fig. 12, an apparent deviation exists between uc and ug after the synchronization. This deviation is not a deviation between the phases but is a result of poor grid quality.

Fig. 14 exhibits the transition from the GC mode to the SA mode during an open circuit fault. The current (the green line) quickly drops to zero, but the inverter continues in the GC mode immediately after the fault, since the latter has not been detected. This improper control mode causes the output

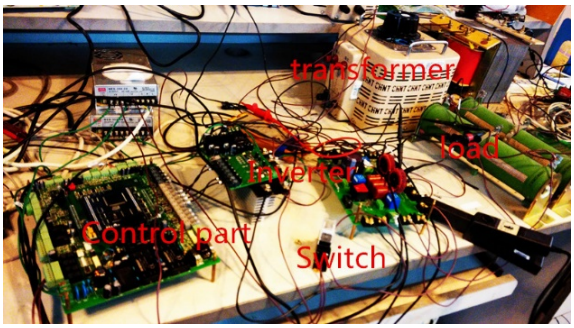

Fig. 11. Experimental platform [36].

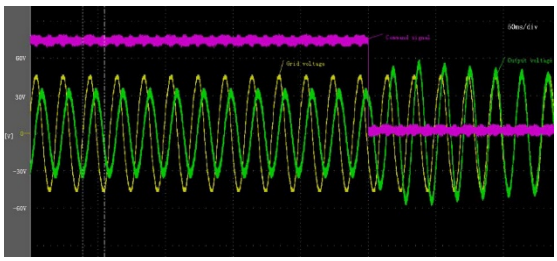

Fig. 12. Transition from stand-alone mode to synchronization mode [36].

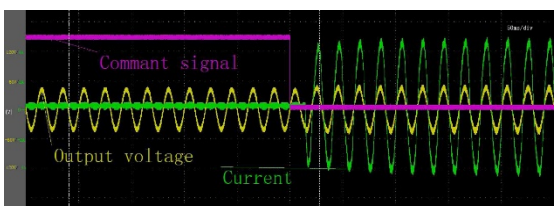

Fig. 13. Transfer process from synchronization mode to grid-connected mode [36].

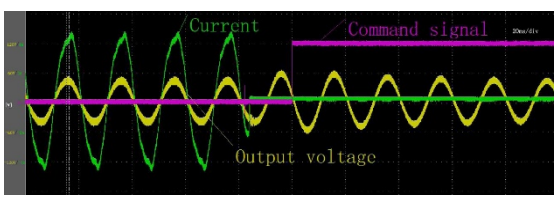

Fig. 14. Transition from grid-connected mode to stand-alone mode [36].

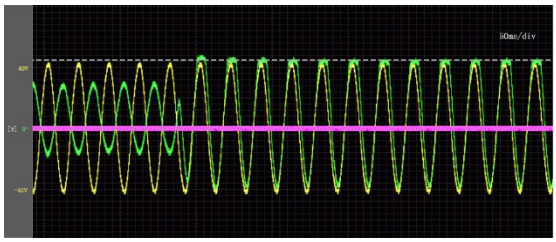

Fig. 15. Transition from stand-alone mode to synchronization mode with PR method.

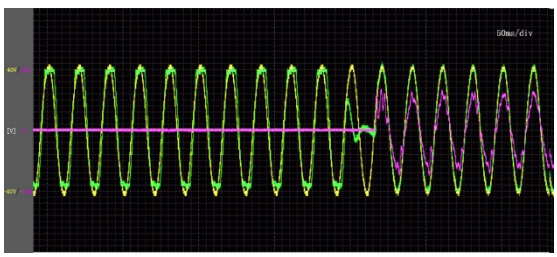

Fig. 16. Transition from synchronization mode to grid-connected mode with PR method.

voltage to rise. Once the fault is detected, the mode change command (the rising edge of the purple waveform) is sent, the inverter transitions from the GC mode to the SA mode, and the waveform of the output voltage restoration is stable in 60 ms. In Fig. 14, a distortion occurs in the current because of the aforementioned poor quality of the utility in the lab.

A comparative experiment using the PR controller under the same conditions is also performed. Figs. 15 and 16 show the transitions from the SA mode to the synchronization mode and from the synchronization mode to the GC mode. At 100 ms, a sharp distortion occurs in Fig. 15 during the transition, while a delay exists in Fig. 16. The same processes in Figs. 12 and 13 are smooth. The rough transitions cause interruptions to the local load and the grid. Since the method cannot achieve asymptotic tracking of the reference, errors persist between the grid and the output voltages.

VI. CONCLUSION

This paper presents an SOR strategy for the seamless transfer of inverter control. This strategy treats the inverter as a relatively independent node in the sense that the operation mode changes influence the reference voltage but do not change the inverter controller, which is always controlling the voltage. This condition offers a smooth transition between modes. An analysis of the closed loop system in the different modes is built in the state space model. This work validates the controller through simulation and experimental results. Future studies will focus on extensions of the proposed strategy to multiple parallel inverters.

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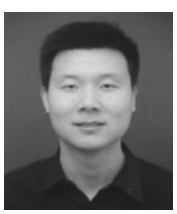
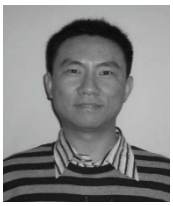


Ji Xiang received his Ph.D. degree in Control Science and Engineering from Zhejiang University, Hangzhou, China, in 2005. From 2005 to 2007, he worked as a Postdoctoral Researcher in Zhejiang University, Hangzhou, China, and he visited the City University of Hong Kong, Kowloon Tong, Hong Kong, China, for three months. Under the support of a Gleddens Senior Visiting Fellowship, he visited the University of Western Australia, Perth, Australia, in 2008. He is presently working as a Professor in the Department of System Science and Engineering at Zhejiang University. His current research interests include complex networks, multi-agent systems, and robotic manipulators.

Feifan Ji was born in Anhui, China, in 1991. He received his B.S. degree from the School of Mechanical, Electrical, and Information Engineering, Shandong University, Weihai, China, in 2012. He is presently working towards his Ph.D. degree in Electrical Engineering in the Department of Electrical Engineering, Zhejiang University, Hangzhou, China. His current research interests include multi-agent systems and the networking of power conversion systems.



Heng Nian received his B.S. and M.S. degrees in Electrical Engineering from the Hefei University of Technology, Hefei, China, in 1999 and 2002, respectively; and his Ph.D. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2005. From 2005 to 2007, he was a Postdoctoral Scholar in the College of Electrical Engineering, Zhejiang University, Hangzhou, China, where he has been an Associate Professor since 2007.

Junming Zhang was born in Zhejiang, China, in 1975. He received his M.S. and Ph.D. degrees in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2000 and 2004, respectively. In 2004, he became a Lecturer in the College of Electrical Engineering of Zhejiang University. In 2014, he was promoted to a full Professor in the College of Electrical Engineering of Zhejiang University. In 2010, he worked as a Visiting Scholar at Michigan State University in Professor Fangzheng Peng's PE lab. His current research interests include power management, power electronics system integrations, high efficiency conversion technology, renewable energy and its applications, etc. He has published more than 70 journal and conference papers. He is the holder of three Chinese and three US patents. He is also a reviewer of the IEEE Transactions on Industry Electronics/Power Electronics, the Transactions of China Electro Technical Society, and Journal of Power Supply. He received a second level Science and Technology Development Award from the China Education Commission in 2003, and his Ph.D. thesis was nominated as one of the "Hundred Excellent Theses" in China in 2006.

Hongqiao Deng was born in Zhejiang, China, in 1993. He is presently working towards his B.S. degree in the Department of Electrical Engineering, Zhejiang University, Hangzhou, China.