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Determination Method for Topology Configuration of Hybrid Cascaded H-Bridge Rectifiers

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Abstract

To reduce system complexity and implementation costs, fully-controlled H-bridge (FHB) modules and diode H-bridge PFC (DHB) modules are cascaded to form a hybrid cascaded H-bridge rectifier (HCHR). In this paper, the advantages of such a HCHR over other cascaded rectifiers are analyzed depending on the numbers of FHB modules and DHB modules. Therefore, to assign proper numbers to these two kinds of modules for the HCHR, a configuration determination method is investigated under balanced and imbalanced loads. Three principles are also presented to guide the configuration determination for the HCHR. In addition, the constraints for selecting the step-up ratio and filter inductance are derived based on a phasor diagram analysis. The proposed configuration determination method is validated by simulations under three different conditions in the PSIM environment. Finally, experiments are carried out on a scaled-down prototype where the configuration can be easily adjusted. The feasibility of the proposed theory is then verified by experimental results.

Key words: Hybrid cascaded H-bridge rectifier, Topology configuration, Unity power factor, Voltage balancing

I. INTRODUCTION

A cascaded H-bridge converter (CHBC) which replaces the line frequency transformer with a high frequency one has attracted significant research interest and is considered a promising candidate for medium/high voltage power conversion practices [1]-[8]. Fig. 1 shows the main topology of a typical CHBC. Several fully-controlled H-bridge (FHB) modules are cascaded to make up the rectifier stage of a CHBC. It is depicted that the output terminal of each H-bridge module in the rectifier stage is connected to the input terminal of a high frequency DC-DC converter. Although the CHBC enjoys advantages such as low switch voltage stress for high voltage applications, modularity, easy expansion capability and bi-directional power flow, it also possesses some undesirable properties. Two major drawbacks are its complicated control system and high implementation costs due to the large number of fully-controlled switches in its rectifier stage. In addition, when more H-bridge modules are cascaded, the number of fully-controlled switches is greatly increased, which requires more control, gate drive and protection circuits. This eventually reduces system reliability and increases implementation costs [9]-[11].

However, in nearly 70% of practical applications, including speed regulation for pumps and fans, only a unidirectional power flow is required. For such application, some fully-controlled switches can be eliminated or replaced. As shown in Fig. 2, [12] proposed a cascaded diode H-bridge rectifier (CDHR) to serve as the rectifier stage of a unitary directional cascaded converter. Several diode H-bridge PFC (DHB) modules are cascaded to make up the CDHR. Each DHB module consists of a diode rectifier and a boost PFC circuit connected in series. Compared to a traditional cascaded H-bridge rectifier (CHR), fewer fully-controlled switches are used. As a result, higher system efficiency and lower implementation costs are achieved. However, the filter inductor at the input side makes it impossible to realize unity power factor rectification. In order to achieve a sinusoidal input current, the CDHR can only operate with a lagging power factor. In addition, the lagging angle increases when the loads of the CDHR become heavier. This characteristic may limit the use of the CDHR in some applications where unity power factor is demanded.

This paper expands the family of cascaded H-bridge

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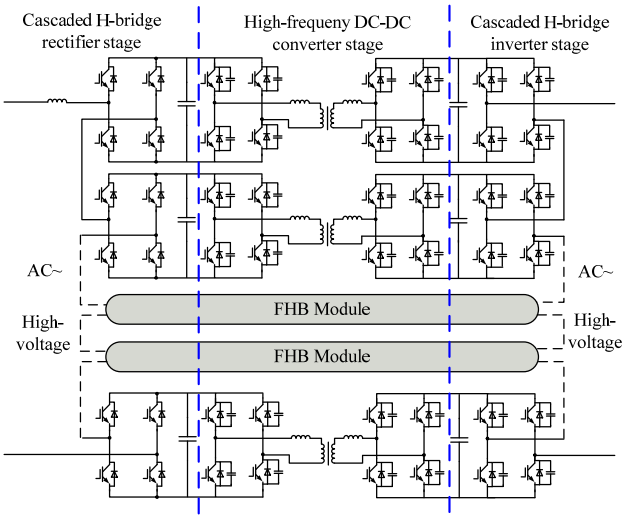

Fig. 1. Topology of cascaded H-bridge converter.

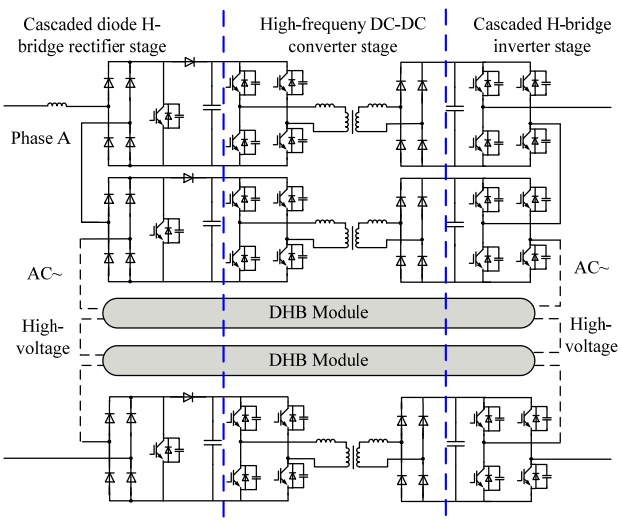

Fig. 2. Topology of cascaded diode H-bridge converter.

rectifiers by introducing the concept of a hybrid cascaded H-bridge rectifier (HCHR). In a HCHR, a part of the modules are FHB modules while the rest are DHB modules. When all of the cascaded modules are DHB modules, the HCHR is the same as the CDHR. Similarly, when all of the cascaded modules are FHB modules, the HCHR becomes a traditional CHR. Actually, the CDHR and CHR can be seen as two particular configurations of the HCHR.

It is clear that the HCHR topology configuration depends on the number of DHB and FHB modules. Therefore, determining a HCHR topology configuration means deciding the number of DHB and FHB modules. By assigning proper numbers to the FHB and DHB modules, the HCHR can enjoy combinatory advantages of both the CDHR and CHR. Reference [13] described a similar hybrid cascaded topology. However, it did not present the principles or control strategies of the rectifier. In addition, it did not demonstrate the validity of such a topology. No relevant researches on methods for determining

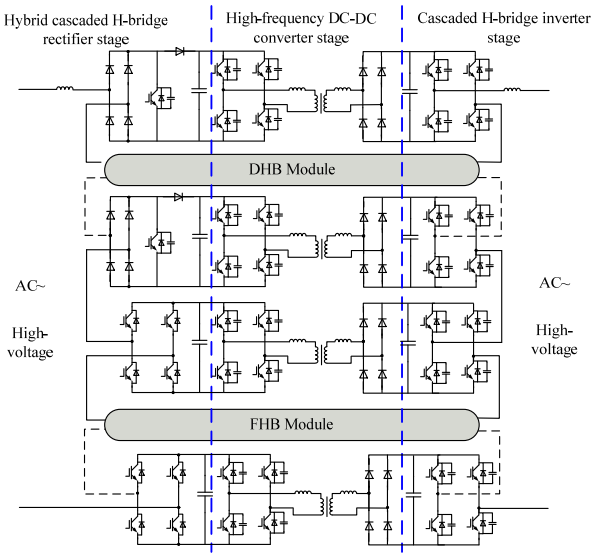

Fig. 3. Topology of the HCHR based cascaded converter.

the HCHR topology configuration have been reported. In an effort to minimize the number of fully-controlled devices and to achieve satisfactory rectification performance at the same time, this paper analyzes the basic principles of the HCHR and proposes a method for determining its topology configuration.

The rest of this paper is organized as follows. Section II presents the basic principles of the HCHR, including the topology configuration, the advantages of the HCHR and the steady-state mathematical model. Then, the determination method of the HCHR topology configuration under different load conditions is proposed by theoretical derivations using phasor diagrams in Section III. On this basis, Section IV derives the constraints for the step-up ratio and filter inductance. Simulation and experimental results are provided in Section V to verify the validity of the theoretical findings. Finally, conclusions are summarized in Section VI.

II. BASIC PRINCIPLES OF THE HCHR

A. Basic Configuration of the HCHR

Fig. 3 illustrates the topology configuration of a HCHR based multi-level converter which is suitable for high frequency unidirectional applications. This converter is composed of three power stages: a HCHR stage, a high frequency DC-DC converter stage with several independent DC-DC converters, and a cascaded H-bridge inverter stage. The HCHR input is connected to a medium/high voltage grid while its outputs are connected to high frequency DC-DC converters.

It should be noted that the three power stages operate with high switching frequencies. In the steady-state, the output voltages of the cascaded modules in the HCHR are regulated to be constant DC voltages. Meanwhile, the values of the input currents of the high frequency DC-DC converters can

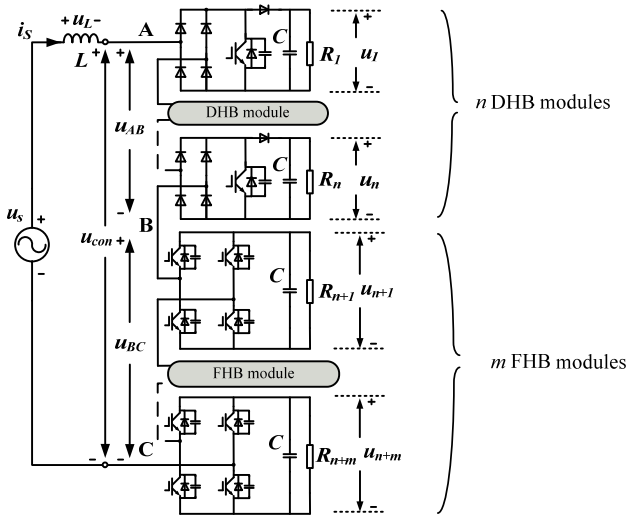

Fig. 4. Topology configuration of the HCHR.

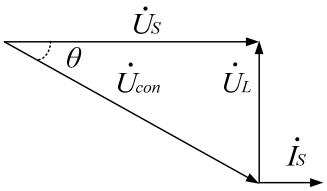

Fig. 5. AC side phasor diagram of a unity power factor rectifier.

also be seen as constant because of the high switching frequency and the coordinated control strategies employed for the HCHR and the DC-DC converters. Hence, the high frequency DC-DC converters can be regarded as resistive loads of the HCHR [14], [15]. Therefore, in the following sections, the loads of the HCHR modules are reasonably represented by resistors [16]-[18]. Then the configuration of the HCHR is shown in Fig. 4.

As can be seen, n DHB modules and m FHB modules are cascaded and then connected to the grid via a filter inductor L. A method for properly determining the values of n and m is the main task of this paper. It should be pointed out that when n=0, the HCHR is a traditional CHR. Similarly when m=0, the HCHR becomes a CDHR. Therefore, the concept of the cascaded H-bridge converter is extended by introducing the HCHR.

B. Steady-state Mathematical Model of the HCHR

A steady-state mathematical model of the system described in Fig.4 can be derived through KCL and KVL equations as:

$$\begin{cases} L\dfrac{di_S}{dt} = u_S - \sum\limits_{i=1}^{n} S_i^* \cdot u_i - \sum\limits_{j=n+1}^{n+m} (2S_j^* - 1)u_j \\ C\dfrac{du_i}{dt} = S_i^* \cdot i_S - \dfrac{u_i}{R_i} \\ C\dfrac{du_j}{dt} = \left(2S_j^* - 1\right) \cdot i_S - \dfrac{u_j}{R_j} \end{cases} \tag{1}$$

where:

u_s, i_s the input voltage and input current;
L the filter inductance at the AC side;
C the DC capacitance of each module;
R_i, u_i, S_i the load equivalent resistance, output voltage and switch state of Module i. S_i=0, 1;
R_j, u_j, S_j the load equivalent resistance, output voltage and switch state of Module j. S_j=0, 1;
$i=1,2,\ldots,n$;
$j=n+1,n+2,\ldots,n+m$;
S_i^*=1- S_i;
S_j^*=1- S_j.

Applying the volt-second balance and ampere-second balance principles to Equ. (1) and Equ. (2) can be yielded as:

$$\begin{cases} i_s = \dfrac{u_S}{\sum\limits_{i=1}^{n} R_i(1-d_i)^2 + \sum\limits_{j=n+1}^{m+n} R_j(1-2d_j)^2} \\ u_i = \dfrac{u_S \cdot R_i(1-d_i)}{\sum\limits_{i=1}^{n} R_i(1-d_i)^2 + \sum\limits_{j=n+1}^{m+n} (R_j(1-2d_j)^2} \\ u_j = \dfrac{u_S \cdot R_j(1-2d_j)}{\sum\limits_{i=1}^{n} R_i(1-d_i)^2 + \sum\limits_{j=n+1}^{m+n} R_j(1-2d_j)^2} \end{cases} \tag{2}$$

where:

d_i, d_j the duty cycle of *Module i* and d_j.

Equ. (2) indicates the input-output characteristics of the hybrid cascaded rectifier. By modifying the duty cycles d_1, $d_2 \ldots d_n$, d_{n+1}, $d_{n+2} \ldots d_{n+m}$, the output voltages of the cascaded modules and the input current of the rectifier can be adjusted.

C. Advantages of the HCHR

Fig. 5 shows a AC phasor diagram of a unity power factor rectifier. With unity power factor achieved, the input voltage $\dot{U}_S$ is in phase with the input current $\dot{I}_S$. The voltage across the filter inductor $\dot{U}_L$ is orthogonal to $\dot{I}_S$. In addition, $\dot{U}_{con}$ is the AC voltage of the rectifier.

Obviously, $\dot{U}_{con}$ lags $\dot{I}_S$ by θ, which means that during a certain period of time, the input current and AC voltage of the rectifier must be in opposite directions. However, due to the unidirectional conductivity of the diodes, the AC voltage and input current of a DHB cannot be in opposite directions. Therefore, if a CDHB composed of DHB modules is forced to operate with unity power factor, serious current distortions appear. However, if the CDHB is controlled to operate with a lagging power factor, the current distortions can be diminished. However, under these circumstances, unity power factor is impossible.

Fig. 6 shows a phasor diagram of the HCHR, in which *Module 1 ~ Module n* are DHB modules and *Module (n+1) ~ Module (n+m)* are FHB modules. $\dot{U}_i$ is the AC voltage of *Module i, i=1,2,3…n*. $\dot{U}_j$ is the AC voltage of *Module j, j=n+1,n+2…n+m*. Due to the unidirectional conductivity of

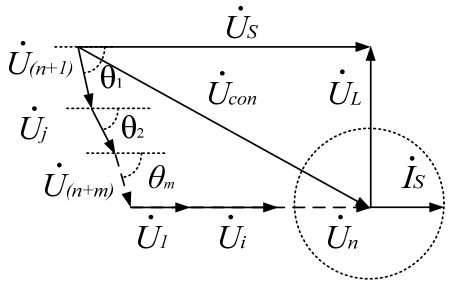

Fig. 6. Phasor diagram of the HCHR with unity power factor.

the diodes, $\dot{U}_i$ must be in phase with the input current $\dot{I}_S$ as stated above. However, $\dot{U}_j$ does not have to be in phase with $\dot{I}_S$ because the switches in the FHB modules are fully-controlled. Therefore, $\dot{U}_{con}=\sum\dot{U}_i+\sum\dot{U}_j$ and $\dot{U}_S=\dot{U}_{con}+\dot{U}_L$ can be satisfied. As a result, the HCHR is able to operate with unity power factor without severe input current distortions.

Compared with a CHR composed of FHB modules, the HCHR uses fewer fully-controlled switches. This results in benefits in terms of reducing the control, gate drive and protection circuits and increasing the system reliability. When more modules are cascaded, these advantages become even more outstanding.

III. Determination of the HCHR Topology Configuration

A. Principles for Determining the HCHR Configuration

(1) Unity power factor rectification and sinusoidal current should be guaranteed.

(2) The output voltages of the cascaded modules should be balanced. Otherwise, the imbalanced voltage caused by device loss mismatching and H-bridge module real power imbalance may result in capacitor overvoltage.

(3) The number of DHB modules should be maximized. Compared with a FHB module, a single DHB module uses three fewer fully-controlled switches. Therefore, with the first two principles satisfied, as many DHB modules should be used as possible.

B. Method of Topology Configuration Determination under Balanced Loads

Assume that the HCHR consists of N modules. *Module 1 ~ Module n* are DHB modules and *Module (n+1)~ Module (n+m)* are FHB modules, $n+m=N$. The equivalent loads are $R_1, R_2 \ldots R_N$, and the output voltages are $E_1, E_2 \ldots E_N$. To minimize the number of FHB modules, their AC voltages should be as low as possible. Therefore, the angles between the input current phasor and the AC voltage phasor of each FHB module should be equal, i.e. $\theta_{n+1}=\theta_{n+2}=\ldots=\theta_{n+m}=\theta$. As stated above, the AC voltage of each DHB module is in phase with the input current to avoid current distortion. Then the active component of the AC voltage of *Module x*, U_{Px} can be expressed as:

$$\begin{cases} U_{Px}=U_{conx}, x=1,2,\cdots,n \\ U_{Px}=U_{conx}\cos\theta, x=n+1,\cdots,n+m \end{cases} \tag{3}$$

where:

U_{conx} the AC voltage of *Module x*.

Then the active power transferred through *Module x* is:

$$U_{Px}I_S=E_xI_x, \quad x=1,2,\ldots,N \tag{4}$$

where:

I_x the output DC current of Module *x*.

In the steady-state the following equations are satisfied:

$$E_1=E_2=\cdots=E_n=\cdots=E_{n+m}=E \tag{5}$$

$$I_1=I_2=\cdots=I_n=\cdots=I_{n+m}=I \tag{6}$$

Substituting Equs. (3), (5) and (6) into Equ. (4) yields:

$$U_{P1}=U_{P2}=\cdots=U_{Pn}=\cdots=U_{P(m+n)} \tag{7}$$

Applying the geometrical relationship yields:

$$\sum_{x=1}^{m+n}U_{Px}=U_S \tag{8}$$

Substitute Equ. (7) into Equ. (8). Then the active component of the AC voltage of each module is expressed as:

$$U_P=U_{Px}=\frac{U_S}{m+n}=\frac{U_S}{N}, \quad x=1,2,\ldots,n+m \tag{9}$$

For each module, the maximum AC voltage $U_{\max}$ which can be obtained through modulation is:

$$\begin{cases} U_{\max}=\dfrac{4}{\sqrt{2}\pi}E, \quad x=1,2,\ldots,n+m \\ U_{Px}\le U_{\max} \end{cases} \tag{10}$$

Fig. 7 shows a phasor diagram of the HCHR for determining its configuration. It can be seen that the total AC voltage of the m FHB modules $\dot{U}_{BC}$ must be capable of composing the phasor triangle with its active component $m\dot{U}_P$ and inductor voltage $\dot{U}_L$. In addition, $U_{BC}\le mU_{\max}$ must be satisfied. Therefore, m is constrained by:

$$(mU_P)^2+U_L^2\le(mU_{\max})^2 \tag{11}$$

Substituting Equ. (9) into Equ. (11) yields:

$$(U_{\max}^2-\frac{U_S^2}{N^2})m^2-U_L^2>0 \tag{12}$$

Define step-up ratio k as:

$$U_{DC}=kU_S \tag{13}$$

where, U_{DC} is the total output voltage. Since the output voltages are balanced, $E=\dfrac{kU_S}{N}$.

Considering the input-output power balance:

$$U_SI_S=NEI \tag{14}$$

where, I_S is the input current of the rectifier. Therefore:

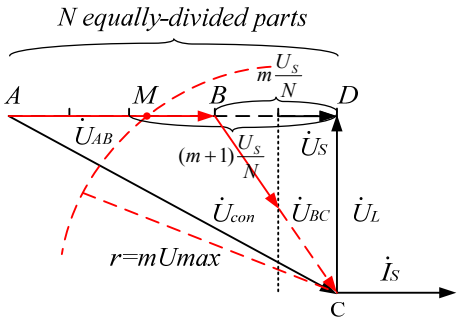

Fig. 7. Phaor diagram of the HCHR under balanced loads.

$$U_L = \omega L I_S \tag{15}$$

Substituting (10), (13), (14) and (15) into (12) yields:

$$m > \frac{\omega k N}{\sqrt{\frac{8}{\pi^2}k^2 - 1}} \frac{LI}{U_S} \tag{16}$$

Then the minimum integer value of m that satisfies Equ. (16) is chosen to be the number of FHB modules. Therefore, n=N-m is the number of DHB modules. Since $U_{\max} > U_P = \frac{U_S}{N}$ in (12), a larger m makes it easier to satisfy (11). In addition, it can be seen from Equ. (16) that m increases if the loads are heavier.

The proposed configuration determination method has its geometrical description. As shown in Fig. 7, U_S is divided equally into N parts. Each part is noted as $U_P = \frac{U_S}{N}$, which represents the active component of the AC voltage of each module. A circle centered at the start point of $\dot{U}_L$ (*Point C*) can be made with a radius of r=$mU_{\max}$. Then an intersection point of the circle and $\dot{U}_S$ can be obtained. Assume that d is the length between the intersection point and the terminal point of $\dot{U}_S$ (*Point D*). If $\frac{mU_S}{N} < d < \frac{(m+1)U_S}{N}$ is satisfied, then the intersection point is defined as *Point M*. The minimum integer value of m that makes the intersection point, *Point M*, is chosen as the number of FHB modules and n=N-m is the number of DHB modules. Then *Point B* can be located on $\dot{U}_S$, satisfying |AB|=$\frac{nU_S}{N}$. On this basis, the total AC voltage of n DHB modules $\dot{U}_{AB}$ and the total AC voltage of m FHB modules $\dot{U}_{BC}$ can be drawn. Since the active AC voltage of every module is guaranteed to be equal and $\dot{U}_{AB}$, $\dot{U}_{BC}$, $\dot{U}_{con}$ are able to compose the phasor triangle, the output voltages can be balanced and unity power factor can be realized.

C. Method of Topology Configuration Determination under Imbalanced Loads

When N loads are imbalanced, the output currents of the cascaded modules are sequenced and noted in ascending order, i.e. $I_1 \le I_2 \le \cdots \le I_n \le I_{n+1} \le \cdots \le I_N$. The active power transferred through each module is expressed as:

$$U_{Px} I_S = E I_x, \quad x=1,2,\ldots,n,n+1,\ldots,N \tag{17}$$

The active power transferred through each module is proportional to the load conductance. Define the load ratio as $n_x = \frac{I_x}{\sum_{i=1}^{N} I_i}$, x=1,2,…,n,n+1…N. The active component of the AC voltage of each module can be expressed as:

$$U_{Px} = n_x U_S \tag{18}$$

In this way, the active power transferred through each module is distributed according to its load conductance so that the output voltages can be balanced. Meanwhile, the total AC voltage of m FHB modules $\dot{U}_{BC}$ must be able to compose a phasor triangle with the sum of their active components $\sum_{i=1}^{m} U_{Pi}$ and inductor voltage $\dot{U}_L$. In addition, the following condition must be satisfied:

$$(\sum_{i=1}^{m} U_{Pi})^2 + U_L^2 \le (mU_{\max})^2 \tag{19}$$

Substituting (10), (13), (14) and (15) into (19) yields:

$$m > \frac{\sqrt{2}\pi N}{4k} \sqrt{\frac{\omega^2 L^2 (\sum_{i=1}^{N} I_i)^2}{{U_S}^4} + (\sum_{j=1}^{m} n_j)^2} \tag{20}$$

Then the minimum integer value of m that satisfies Equ. (20) is chosen to be the number of FHB modules and n=N-m is the number of DHB modules. It can also be seen from Equ. (20) that heavier loads lead to a larger m.

As can be derived from Equ. (19):

$$\begin{aligned}(mU_{\max})^2 - (\sum_{i=1}^{m} U_{Pi})^2 - U_L^2 &> (mU_{\max})^2 - (mU_{P\max})^2 - U_L^2 \\ &= (U_{\max}^2 - {U_{P\max}}^2)m^2 - U_L^2 > 0\end{aligned} \tag{21}$$

where U_{Pmax} is the maximum value of U_{Pi} and $U_{\max} > U_{Pmax}$. Therefore, a larger m makes it easier to satisfy Equ. (19). Similar to the balanced loads case, the determination method for the hybrid cascading mode under imbalanced loads has a corresponding geometrical description.

IV. Constraints for the Step-up Ratio and Filter Inductance

The step-up ratio and filter inductance are important for a HCHR to achieve a desired performance. This section derives the constraints for the step-up ratio and filter inductance. To avoid a loss of generality, the derivation is done under imbalanced loads. As indicated in Equ. (21), $U_{\max}$ is required to satisfy:

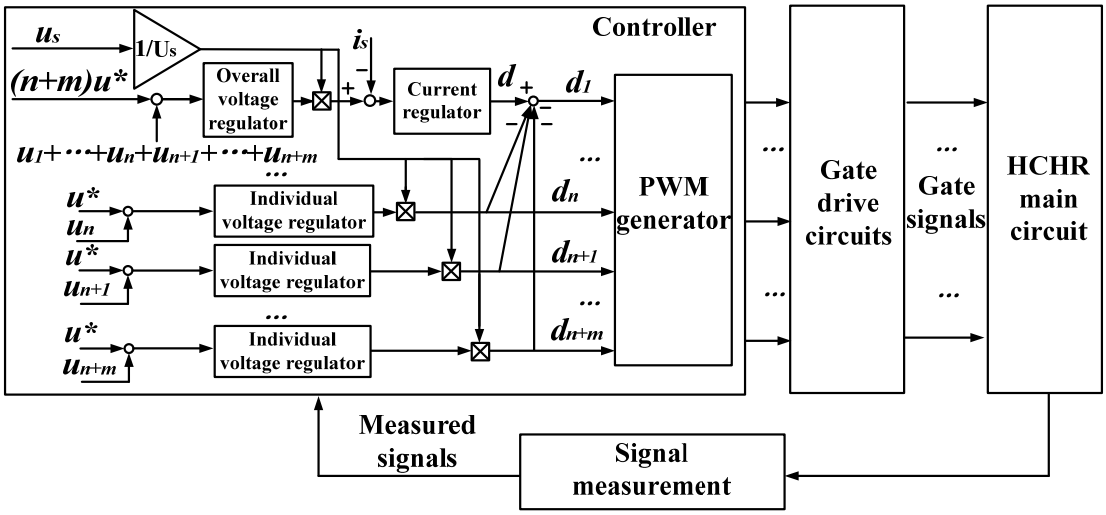

Fig. 8. Block diagram of the simulation model.

$$\begin{cases} U_{\max} = \dfrac{4}{\sqrt{2}\pi} E \\ U_{\max} > U_{P\max} = \dfrac{I_{\max}}{\sum_{i=1}^{N} I} U_S \end{cases} \tag{22}$$

Then the constraint for the step-up ratio can be obtained as:

$$k > \frac{\sqrt{2}\pi N}{4} \frac{I_{\max}}{\sum_{i=1}^{N} I_i} \tag{23}$$

Since the larger m is, the easier it is for Equ. (19) to be satisfied, the constraint for the filter inductance is derived based on the extreme condition that $m=N$. Therefore, Equ. (24) must be satisfied to guarantee the feasibility of the HCHR configuration.

$$(NU_{\max})^2 - (\sum_{i=1}^{N} U_{Pi})^2 - U_L^2 > 0 \tag{24}$$

Substituting Equs. (10) and (18) into Equ. (21) yields:

$$U_L^2 < (\frac{8}{\pi^2} k^2 - 1) U_S^2 \tag{25}$$

Substitute Equ. (15) into Equ. (25). The constraint for filter inductance is then expressed as:

$$L < \sqrt{\frac{(\frac{8}{k\pi^2} - \frac{1}{k^3}) N U_S}{\omega^2 \sum_{i=1}^{N} \frac{1}{I_i}}} \tag{26}$$

V. Simulation and Experimental Results

To verify the validity of the proposed theory, simulations have been carried out in the PSIM environment. A simulation model is built according to Fig. 4 and a block diagram is illustrated in Fig. 8. The dual-loop control strategy is employed in the controller. The overall voltage-loop is implemented to regulate the total output voltage. The current-loop that generates the total duty ratio d is responsible for realizing a unity power factor and sinusoidal current by forcing the input current to be in phase with the grid voltage. For *Module 2 ~ Module (n+m)*, a single individual voltage regulator is applied to make the output voltage equal to the reference voltage u^*. Through this individual voltage regulator, the duty cycles $d_2 \ldots d_n$, d_{n+1}, $d_{n+2} \ldots d_{n+m}$ are generated. Then the duty cycle of *Module 1* is obtained by $d_1 = d - d_2 - \ldots - d_{n+m}$. For the following simulations and experiments, the values of n and m are determined according to specific system parameters.

TABLE I
Parameters for the Simulation Model

Parameters	Values
Input voltage *us/V*	220
Switching frequency *fs/kHz*	10
Load of Module 1 R_1/Ω	20
Load of Module 2 R_2/Ω	20
Filter inductance *L/mH*	0.2
Capacitance of each module *C/mF*	0.2
Reference output voltage u_{ref}/V	250

Table I lists the initial parameters for the simulation model. In this case, two modules are used to make up the rectifier. Firstly, the topology configuration is determined while only considering using minimum fully-controlled devices. Then both of the modules are implemented using DHB modules. Fig. 9 shows the input current and output voltages. The two output voltages are almost maintained at the reference value. However, it is clearly seen that serious current distortions occur.

Therefore, the topology configuration should be redesigned. According to calculations based on the proposed theory in Section III, Module 1 adopts the FHB module and Module 2 adopts the DHB module. As can be seen from Fig. 10, a

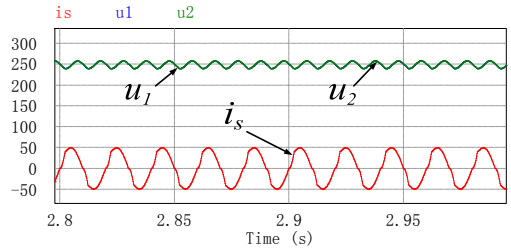

Fig. 9. Input current and output voltages of the HCHR based on 2 DHB modules.

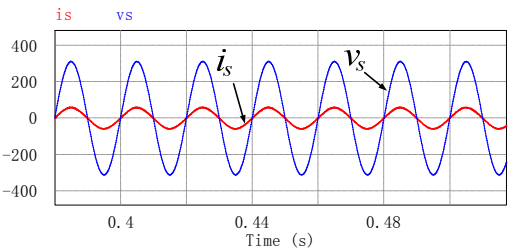

Fig. 10. Input current and voltage of the HCHR based on 1 DHB and 1 FHB module.

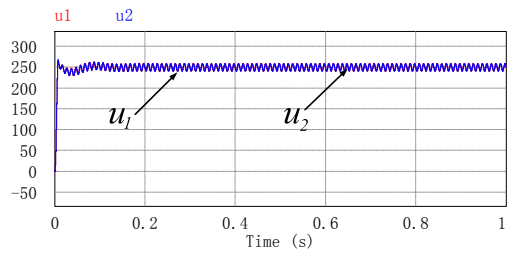

Fig. 11. Input current and voltage of the HCHR based on 1 DHB and 1 FHB module.

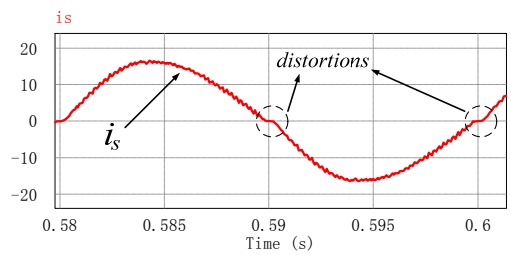

Fig. 12. Input current of the rectifier based on 1 DHB and 1 FHB with modified loads and reference output voltage.

sinusoidal input current and unity power factor rectification are achieved. Fig. 11 shows that the output voltages are kept equal to the reference value. The feasibility and performance of the HCHR under balanced loads are validated.

To verify the feasibility of the proposed determination method under imbalanced loads, the load of *Module 1* is changed from 20Ω to 15Ω. In addition, the reference output voltage is modified to be 150V, which leads to a change in the step-up ratio *k*. If *Module 1* is still a FHB and *Module 2* is still a DHB, input current distortions appear at the zero-crossings as shown in Fig. 12. Therefore, the configuration needs to be redesigned. As a result, both of the modules adopt FHB modules. Fig. 13 and Fig. 14 show that satisfactory rectification and output DC voltage balancing are achieved.

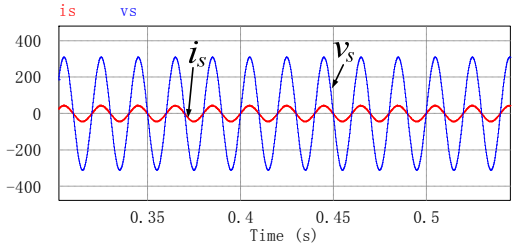

Fig. 13. Input voltage and current of the rectifier based on 2 FHB with modified loads and reference output voltage.

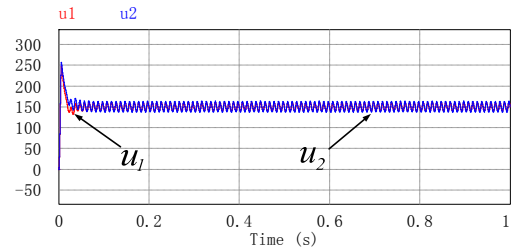

Fig. 14. Output voltages of the rectifier based on 2 FHB modules with modified loads and reference output voltage.

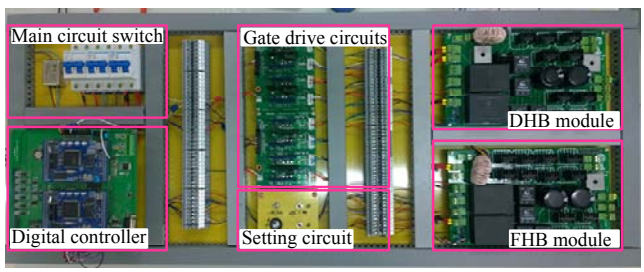

Fig. 15. Scaled-down experimental prototype.

TABLE II
PARAMETERS FOR THE EXPERIMENTAL PROTOTYPE

Parameters	Values
Input voltage *us/V*	220
Switching frequency *fs/kHz*	10
Load of Module 1 R_1/Ω	20
Load of Module 2 R_2/Ω	20
Filter inductance *L/mH*	0.2
Capacitance of each module *C/mF*	0.2
Reference output voltage u_{ref}/V	250

To further verify the performance of the HCHR and the proposed configuration determination method, a scaled-down experimental prototype is implemented in the lab. The prototype is shown in Fig. 15. A DSP TMS320F28335 serves as the core controller. The parameters are provided in Table II. The two modules can be implemented as FHB or DHB depending on the configuration determination.

First, without determining the configuration using the proposed method, Module 1 and 2 are implemented as DHB modules to minimize the number of fully-controlled devices. However, as shown in Fig. 16, a severe input current distortion appears and a slight output DC voltage imbalance exists.

Obviously, the configuration needs to be redesigned. By taking the three principles presented in Section III into

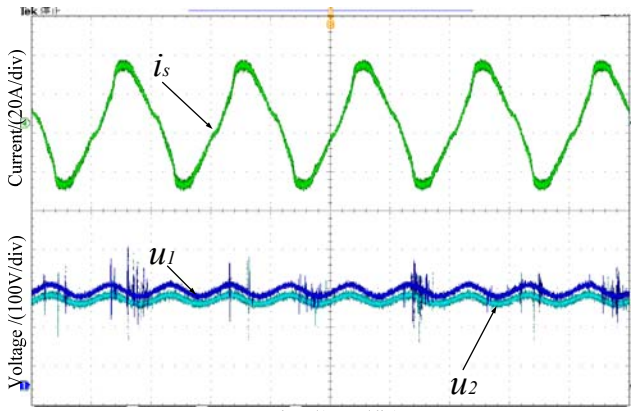

Fig. 16. Input current and output voltages of the HCHR based on 2 DHB modules.

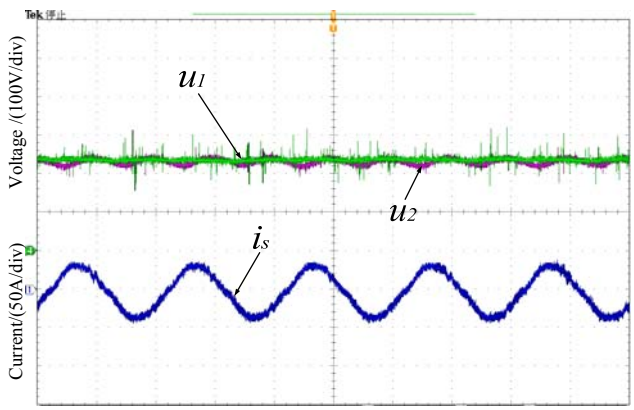

Fig. 17. Input current and output voltages of the HCHR based on 1 DHB and 1 FHB module.

considerations, it is easy to determine that one module should be a FHB module and the other one should be a DHB module. Therefore, a FHB is adopted for *Module 1* while a DHB is adopted for *Module 2*.

Fig. 17 shows the input current and output voltages of the HCHR based on one DHB and one FHB module. The output voltages of the two modules are maintained at the reference value and the input current is sinusoidal. As shown in Fig. 18, input current is in phase with the input voltage, which indicates a unity power factor. Therefore, a HCHR composed of one DHB and one FHB can realize satisfactory rectification and output DC voltage balancing.

Compared to a rectifier composed of two FHB modules, the three fully-controlled switches are reduced, resulting in less complicated control, gate drive, and protection circuits, which helps cut down the implementation costs in practical applications. Meanwhile, system reliability is also increased due to simpler control circuits. This demonstrates the advantages of the HCHR over the traditional CHR.

To verify the feasibility of the proposed determination method under imbalanced loads, the load of Module 1 is changed from 20Ω to 15Ω. In addition, the reference output voltage is modified to 150V, which leads to a change of the

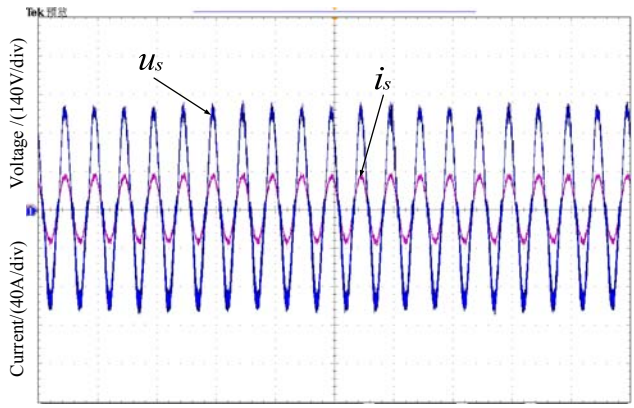

Fig. 18. Input current and voltage of the HCHR based on 1 DHB and 1 FHB module.

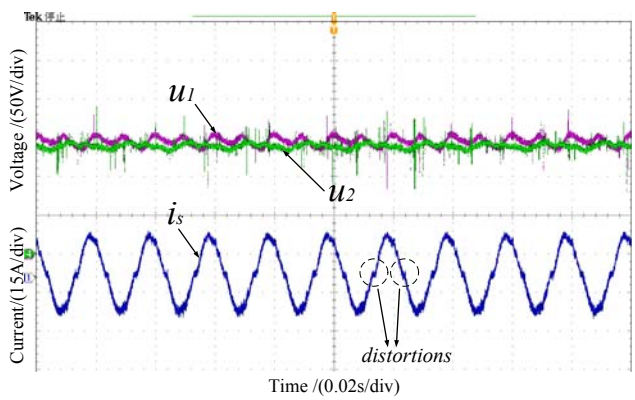

Fig. 19. Input current and output voltages of HCHR composed of 1 DHB and 1 FHB with modified loads and reference voltage.

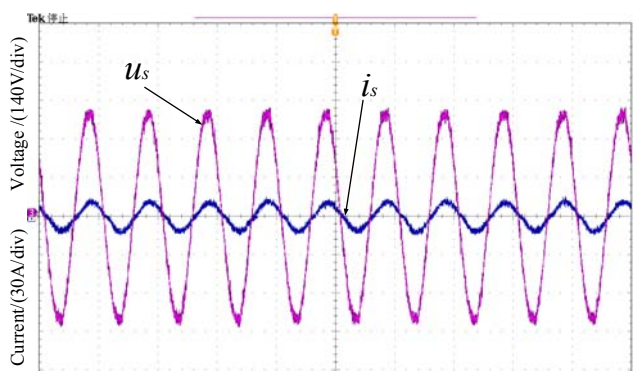

Fig. 20. Input current and voltage of the rectifier composed of 2 FHB modules with modified loads and reference output voltage.

step-up ratio k. If Module 1 is still a FHB and Module 2 is still a DHB, the input current and output voltages become undesirable as shown in Fig. 19. Input current distortions exist at the zero-crossings and a slight difference appears between the output voltages.

Therefore, the configuration should be redesigned. According to Equation (20) in Section III and Equation (23), (26) in Section IV, the number of FHB modules should be two so that unity power factor rectification and output voltage balancing can be realized, while the constraints for filter

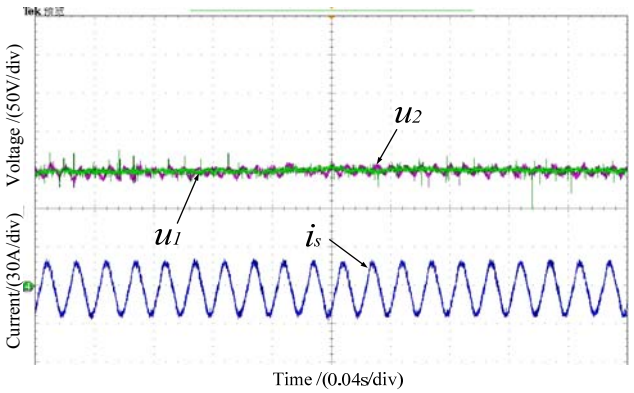

Fig. 21. Input current and output voltages of the rectifier composed of 2 FHB modules with modified loads and reference output voltage.

inductance and step-up ratio can also be satisfied. Therefore, both of the modules are implemented using FHB modules. Fig. 20 shows the input voltage and rectifier using two FHB modules. As depicted in the figure, the input current is sinusoidal and in phase with the grid voltage. Fig. 21 shows the output voltages and input current. It can be seen that the output voltages of the two FHB modules are well balanced.

Simulation and experimental results agree with the theoretical analysis in validating the satisfactory rectification and voltage balancing performance of the presented HCHR when its configuration is properly determined using the proposed method.

VI. CONCLUSIONS

This paper investigates a detailed configuration determination method for the presented HCHR topology. Three basic principles are proposed to achieve unity power factor rectification, output DC voltage balancing and a reduced number of fully-controlled devices. On this basis, a configuration determination method under balanced and imbalanced load conditions is derived. In addition, a corresponding geometrical description of the configuration determination method is presented in the form of a phasor diagram. Additionally, constraints for the step-up ratio and filter inductance are derived. Simulation and experiment results validate the theoretical analysis.

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REFERENCES

[1] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 4, pp. 1737-1746, Jul. 2009.

[2] Z. Li, P. Wang, and Z. Chu, "An improved pulse width modulation method for chopper cell based modular multilevel converters," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3472-3481, Aug. 2012.

[3] H. Iman-Eini, S. Farhangi, M. Khakbazan-Fard, and J.-L. Schanen, "Analysis and control of a modular MV-to-LV rectifier based on a cascaded multilevel converter," *Journal of Power Electronics*, Vol. 9, No. 2, pp. 133-145, Mar. 2009.

[4] S. M. Park and S.-Y. Park, "Versatile control of unidirectional AC–DC boost converters for power quality mitigation," *IEEE Trans. Power Electron.*, Vol. 30, No. 9, pp. 4738-4749, Sep. 2015.

[5] X.Wang, J. Liu, S. Ouyang, T. Xu, F. Meng, and S. Song, "Control and experiment of an H-bridge-based three-phase three-stage modular power electronic transformer," *IEEE Trans. Power Electron.*, Vol. 31, No. 3, pp. 2002-2011, Mar. 2016.

[6] Y.-M. Park, H.-S. Ryu, H.-W. Lee, M.-G. Jung, and S.-H. Lee, "Design of a cascaded H-bridge multilevel inverter based on power electronics building blocks and control for high performance," *Journal of Power Electronics*, Vol. 10, No. 3, pp. 262-269, May 2010.

[7] R. Nagarajan and M. Saravanan, "Performance analysis of a novel reduced switch cascaded multilevel inverter," *Journal of Power Electronics*, Vol. 14, No. 1, pp. 48-60, Jan. 2014.

[8] M. Saradarzadeh, S. Farhangi, J.-L. Schanen, D. Frey, and P.-O. Jeannin, " A novel DC bus voltage balancing of cascaded H-bridge converters in D-SSSC application, " *Journal of Power Electronics*, Vol. 12, No. 4, pp. 567-577, Jul. 2012.

[9] F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies," *IEEE Trans. Smart Grid*, Vol. 3, No. , pp. 413-421, Mar. 2012.

[10] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, Vol. 29, No. 10, pp. 5579-5591, Oct. 2014.

[11] H. Zhang and Z. Shiwu, "Drive circuit of three-level IGBT module based on 2SC0108T Chip," *High Power Converter Technology*, Vol. 2, pp. 5-9, Mar./Apr. 2014. (in Chinese)

[12] W. Cong, W. Chang, J. Jian, and C. Hong, "New cascade diode H-bridge multi-level rectifier," *Transactions of China Electrotechnical Society*, Vol. S1, pp. 273-281, Dec. 2014. (in Chinese)

[13] W. Chang, "Novel high-power cascaded H-bridge multi-level converter," Ph.D. Dissertation, China University of Mining & Technology, Beijing, China, 2015. (in Chinese)

[14] A. Moeini, H. Iman-Eini, and A. Marzoughi, "DC link voltage balancing approach for cascaded H-bridge active rectifier based on selective harmonic elimination-pulse width modulation," *IET Power Electron*., Vol. 8, No. 4, pp. 583-590, Aug. 2015.

[15] P. Karamanakos, K. Pavlou, and S. Manias, "An enumeration-based model predictive control strategy for the cascaded H-bridge multilevel rectifier," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 7, pp. 3480-3489, Jul. 2014.

[16] J. Venkat, A. Shukla, and S. V. Kulkarni, "Operation of a three phase solid state-transformer under unbalanced load

conditions," in *Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference on*, pp. 1-6, 2014.
[17] J. Shi, W. Gou, H. Yuan, T. Zhao, and A. Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," *IEEE Trans. Power Electron.*, Vol. 26, No. 4, pp. 1154-1166, Apr. 2011.
[18] X. She, A. Q. Huang, and G. Wang, "3-D space modulation with voltage balancing capability for a cascaded seven-level converter in a solid-state transformer," *IEEE Trans. Power Electron.*, Vol. 26, No. 12, pp. 3778-3789, Dec. 2011.

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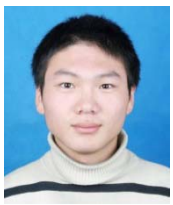

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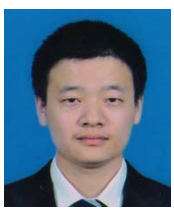

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