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Capacitance Estimation of the Submodule Capacitors in Modular Multilevel Converters for HVDC Applications

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Abstract

To achieve higher reliability in the modular multilevel converters (MMC) for HVDC transmission systems, the internal condition of the DC capacitors of the submodules (SM) needs to be monitored regularly. For an online estimation of the SM capacitance, a controlled AC current with double the fundamental frequency is injected into the circulating current loop of the MMC, which results in current and voltage ripples in the SM capacitors. The capacitor currents are calculated from the arm currents and their switching states. By processing these AC voltage and current components with digital filters, their capacitances are estimated by a recursive least square (RLS) algorithm. The validity of the proposed scheme has been verified by simulation results for a 300-MW, 300-kV HVDC system. In addition, its feasibility has been verified by experimental results obtained with a reduced-scale prototype. It has been shown that the estimation errors for both the simulation and experimental tests are 1.32% at maximum.

Key words: Capacitance estimation, Circulating current, Condition monitoring, Modular multilevel converter, Submodule capacitor

I. INTRODUCTION

Recently, modular multilevel converters have drawn a significant amount of attention not only for high-voltage high-power applications such as high-voltage direct-current (HVDC) transmission systems, but also for medium voltage applications such as motor drives, active power filters, static synchronous compensators, etc. [1], [2]. When compared with conventional multilevel converters such as the neutral-point clamped (NPC) type, the flying-capacitor type, and the cascaded H-bridge type, the attractive features of the MMC are its low switching frequency, high efficiency, modularity, scalability, and flexible design [3]-[7]. In addition, due to modular structures with cascaded submodules, a series connection of multiple semiconductor devices in one converter arm and especially high DC-voltage capacitors can be avoided, which significantly reduces the voltage stresses on the devices. A large number of levels enables a remarkable decrease in the average switching frequency without any distortion of the output voltage or current waveforms. An MMC-based HVDC transmission system is shown in Fig. 1 [8].

It has been reported that MMC-based HVDC transmission systems have been commercialized by Siemens, and that the product model is the HVDC PLUS [9]. For instance, a 400-MW HVDC PLUS consisting of 216 power modules in each arm of the MMC was commissioned in 2010 for the Trans Bay Cable Project [9], [10]. Another product from Siemens that utilizes MMC technology for the applications of high-voltage STATCOMs, is the SVC PLUS. The power rating of this system ranges from 25 to 250 MVAR, in which each converter branch of the MMC is typically composed of 12 to 48 submodules [11].

In multilevel converters with a large number of converter modules, the fault diagnosis of IGBTs and DC capacitors is

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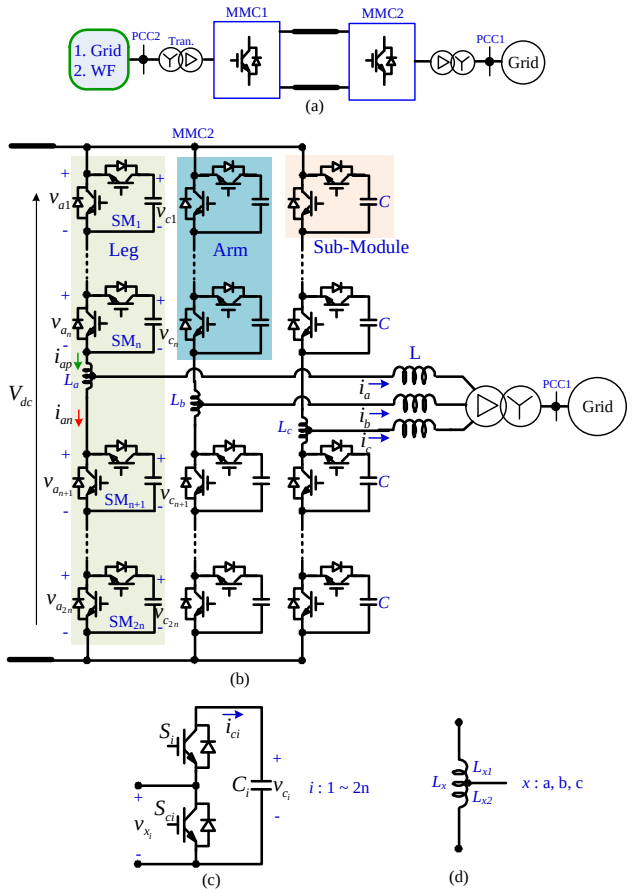

Fig. 1. HVDC transmission system. (a) Circuit diagram. (b) Grid-connected MMC. (c) Submodule. (d) Arm inductors.

an important issue. So far, there have been several studies which focus mainly on the fault detection of the IGBT open circuits for MMCs and cascaded H-bridge multilevel converters [12]-[14].

On the other hand, the fault diagnosis of SM capacitors in MMCs has not been deeply investigated in previous publications. It is known that the capacitor is one of the weakest components in power electronic converters, since capacitors are gradually deteriorated due to chemical processes [15], [16]. The aging effects of a capacitor result in a decrease of the capacitance or an increase of the equivalent series resistance (ESR) [17].

Therefore, to increase the reliability of the whole system, condition monitoring of electrolytic capacitors is essential. This usually relies on capacitance estimation. Several studies have been conducted on fault diagnosis techniques for the DC-link capacitors in two-level AC/DC PWM converters [18] and in AC drive inverters [15], [19], [20]. A method with current injection in the converter input or the inverter output to produce AC current and voltage components in capacitors was proposed in [18], [19], which gives a high estimation accuracy. However, fault diagnosis of the SM capacitors of the MMCs in HVDC transmission systems has been rarely reported.

In this paper, a scheme for capacitance estimation of the SM capacitors in MMC-based HVDC transmission systems is proposed for condition monitoring, which is extended from [21] and [22]. In this work, the grid-connected application of MMCs is investigated rather than simple inverter systems. More importantly, the AC current injection technique in the circulating current loops is analyzed in detail. For the proposed scheme, the capacitance of every SM can be estimated during normal operation, where the current and voltage ripple components in the capacitors are utilized. At first, a regulated AC current is injected into the circulating current loop of the converter-phase leg. Then, AC voltage and current ripples in the submodule capacitors are induced, where the capacitor currents are calculated by the arm currents and switching states of the SM. The capacitances of each SM are estimated by an RLS method. The effectiveness of the proposed estimation method is verified by PSIM simulation and experimental tests, where a 300-MW 300-kV 7-level MMC is used for the simulation, and a down-scaled prototype of a 3-level MMC in the laboratory was tested. The results show that the maximum estimation error for both the simulation and experiment is about 1.32%.

II. Modeling of Modular Multilevel Converters in HVDC Transmission Systems

A. Structure of the System

An overall HVDC transmission system based on an MMC is used to deliver power between two grids or from a wind farm to a grid, which is shown in Fig. 1(a). Fig. 1(b) shows a three-phase MMC consisting of six arms, where each arm of the converters is composed of *n* series-connected SMs and one inductor [3], [4], [23]. The SM is composed of a half bridge with a complementary switch pair and a DC capacitor as shown in Fig. 1(c). The coupled inductors in the converter arms are shown in Fig. 1(d), which can be used to control the circulating currents and to limit the fault currents. The output voltage of the SM, v_{x_i}, depends on the switching states of the SM, which are equal to the capacitor voltage, $v_{c_i}\,(i=1\sim 2n)$, when the upper switch, S_i, is turned on and the lower switch, S_{ci}, is turned off. On the other hand, the output voltage is zero when the lower switch is turned on and the upper switch is turned off. In this case, the capacitor is of unchanged states, which are isolated from the arm current.

B. Equivalent Model of a Three-Phase MMC

Fig. 2 shows an equivalent circuit of an MMC. The output voltage of the arm is the sum of the output voltages for all of the SMs in the arm [4]. Since the capacitor voltages fluctuate and are unbalanced among the different SMs, the output voltages of the upper and lower arms also contain ripple components, which can be expressed as [24]:

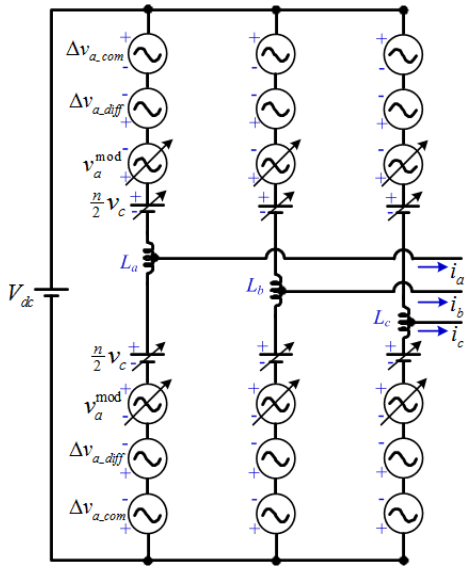

Fig. 2. Equivalent circuit of three-phase MMC.

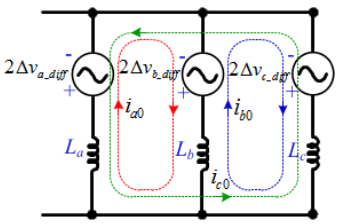

Fig. 3. Circulating currents in three-phase MMC.

$$v_{arm\_p}^{a} = \frac{n}{2}v_c - v_a^{\text{mod}} - \Delta v_{a\_diff} + \Delta v_{a\_com} \quad (1)$$

$$v_{arm\_n}^{a} = \frac{n}{2}v_c + v_a^{\text{mod}} - \Delta v_{a\_diff} - \Delta v_{a\_com} \quad (2)$$

where $v_{arm\_p}^{a}$ and $v_{arm\_n}^{a}$ are the output voltages of the upper and lower arms, respectively, v_a^{mod} is the desired output AC voltage generated from the pulse modulation, and Δv_{a_diff} and Δv_{a_com} represent undesired ripple voltages, which are the differential and common mode ripple voltages, respectively, caused by the capacitor ripple voltage. Then, the output voltage in the leg is expressed as:

$$v_{arm\_p}^{a} + v_{arm\_n}^{a} = nv_c - 2\Delta v_{a\_diff} = V_{dc} - 2\Delta v_{a\_diff} \quad (3)$$

where V_{dc} is the HVDC-link voltage.

C. Analysis of the Circulating Currents

The second term on the right-hand side of (3) is the voltage difference of the phase leg voltage and the HVDC-link voltage, which is also the voltage drop in the arm inductor L_x. The voltage ripples in different phase legs of the MMC are different from each other, which cause the circulating current flowing among the three phase legs. Fig. 3 shows the circulating current paths in the three-phase MMC. The voltage equation for the loop around the DC link and converter leg-A is expressed as:

$$V_{dc} = \sum_{i=1}^{2n} v_{a_i} + L_a \frac{d}{dt}(i_{ap} + i_{an}) \quad (4)$$

where i_{ap} and i_{an} are the upper and lower arm currents, respectively.

The circulating current, i_{a0}, flowing through converter leg-A is defined as [3], [4]:

$$i_{a0} = i_{ap} - \frac{i_a}{2} = i_{an} + \frac{i_a}{2} = \frac{1}{2}(i_{ap} + i_{an}) \quad (5)$$

where i_a is the phase-A current.

From (3) to (5), the voltage equation can be rewritten as:

$$\begin{aligned} V_{dc} &= v_{arm\_p}^{a} + v_{arm\_n}^{a} + 2\Delta v_{a\_diff} \\ &= v_{arm\_p}^{a} + v_{arm\_n}^{a} + 2L_a \frac{di_{a0}}{dt}. \end{aligned} \quad (6)$$

It can be seen from (3) and (6) that the output voltages of the SMs can be used to regulate the circulating current. Consequently, the circulating current can be utilized to control the arm voltages as well as the SM capacitor voltages.

D. Current and Voltage Ripples in SM Capacitors

As shown in Fig. 1, the current of the SM capacitors, i_{ci}, is determined by the switching function of the SM and the corresponding arm current, which is expressed as [24], [25]:

$$i_{ci} = F_{sw}^{SMi} i_{arm} \quad (7)$$

where i_{arm} is the current of the corresponding arm and F_{sw}^{SMi} is the switching function of the SM, which is defined as:

$$F_{sw}^{SMi} = \begin{cases} 1 \text{ when } S_i \text{ is turned on} \\ 0 \text{ when } S_{ci} \text{ is turned on} \end{cases}. \quad (8)$$

The switching function of the SMs consists of DC and fundamental components with the switching harmonics neglected [23]. In addition, it is known that the arm currents mainly contain DC and fundamental components [4]. Then, it can be seen in (7) and (8) that the capacitor current contains DC, fundamental and double fundamental frequency components, which depend on the load conditions. This current ripple causes voltages ripple in the SM capacitors.

III. Control of Modular Multilevel Converters

In MMCs, circulating current reduction and capacitor voltage balancing in the phase leg of the converter are important issues. Thus, average control for the converter leg voltages and voltage balancing control for each of the SM capacitors are necessary [3].

A. Average Control for Converter Leg Voltages

A cascaded control structure is employed for average control of the converter leg voltage. The outer loop controls

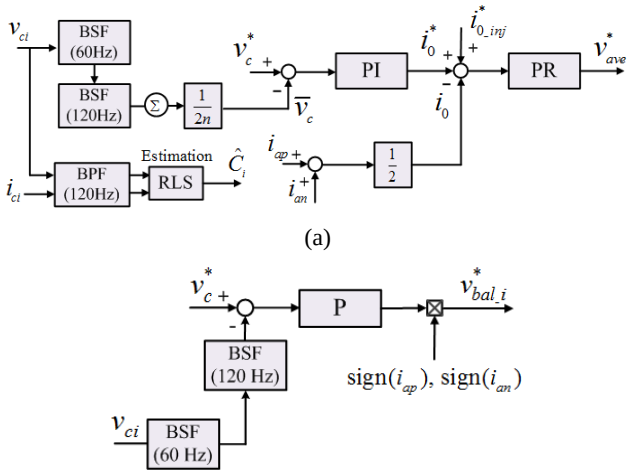

Fig. 4. Control block diagram of SMs. (a) Average control. (b) Balancing control.

TABLE I
SWITCHING STATES OF SM

S_{ci}	S_i	v_{xi}	Current direction	Capacitor state
off	on	$\frac{1}{6}V_{dc}$	$i_{ci}>0$	charging
off	on	$\frac{1}{6}V_{dc}$	$i_{ci}<0$	discharging
on	off	0	$i_{ci}>0$	unchanged
on	off	0	$i_{ci}<0$	unchanged

the average voltage for all of the SM capacitors in order to follow its command, where controller output is the circulating current reference. Then, the inner current control loop regulates the circulating currents flowing in the converter legs.

To obtain the voltage and current ripples of the SM capacitors sufficiently high for estimation under any operating conditions, the regulated AC current component is injected into the circulating current loop during the estimation process. The injected current reference, $i^*_{0\_inj}$, is chosen as:

$$i^*_{0\_inj} = I_{inj} \cdot \sin(2\pi f_{inj} t + \varphi_{inj}) \tag{9}$$

where I_{inj} and f_{inj} are the magnitude and frequency of the injected current, respectively, and φ_{inj} is the initial phase angle of the injected current. The magnitude should be chosen so that the arm currents and the ripple component of the capacitor currents are kept within allowable ranges. It is known that second-order harmonic in the arm currents may exist, which charges or discharges the SM capacitors. In this paper, the injected frequency is chosen as double the fundamental frequency, which causes a sufficient voltage ripple for the capacitance estimation. The initial phase angle of the injected current is selected as [24], [26]:

$$\varphi_{inj} = \varphi + \pi \tag{10}$$

where φ is the phase shift between the grid voltage and current.

A block diagram of the average voltage control is shown in Fig. 4(a), where PI (proportional and integral) controllers are used for the outer voltage control loop. The average voltage, $\overline{v}_c$, which is the feedback signal for the average voltage control loop, is calculated as:

$$\overline{v}_c = \frac{1}{2n}\sum_{i=1}^{2n} BSFs(v_{ci}) \tag{11}$$

where v_{ci} is the i^{th}-SM capacitor voltage. Band-stop filters (BSF) with 60-Hz and 120-Hz cut-off frequencies are applied to the SM capacitor voltages, since the capacitor voltages may contain ripple components with fundamental and second-order harmonics due to the injected AC current and arm current.

Due to the presence of the injected AC current component in the circulating current, PR (proportional and resonant) regulators are employed for the inner current control loop, where the circulating current, calculated from the upper and lower arm currents in (5), is a feedback term. It is worth noting that the regulated AC current is periodically injected only during the short time of the estimation process, which does not harm the whole system operation as well as the converter control performance. Under normal conditions, the circulating current is suppressed by the average control.

B. Balancing Control for Submodule Capacitor Voltages

The SM capacitor voltages are controlled to be constant by selecting appropriate switching states for the corresponding SMs, where the capacitors can be either charged or discharged depending on the arm currents. Fig. 4(b) shows a block diagram of the balancing control for each SM, where a proportional controller is used. The capacitor voltage reference, v^*_c, is set as $\frac{1}{n}V_{dc}$, which is the same as the reference of the average capacitor voltage. The polarity of the voltage command for the balancing control depends on that of the arm currents as shown in Fig. 4(b). BSFs with 60-Hz and 120-Hz cutoff frequencies are also used to eliminate the ripples of the capacitor voltages.

C. Carrier-Phase-Shift PWM

For a simple analysis, a 7-level MMC is taken into account in this paper. Table I summarizes the switching states of an SM and the resultant output voltages, where the SM capacitor voltage is one sixth of the DC-link voltage for the 7-level MMC. The output voltage of the SM can be either 0 or $\frac{1}{6}V_{dc}$, depending on the switching states.

In this paper, carrier-phase-shift pulse-width modulation (CPS-PWM) is applied to a 7-level MMC, where the modulation scheme for the SM switches is shown in Fig. 5 [27], [28]. Six triangular carrier waves (y_{c1}, ..., y_{c6}), with a frequency of f_s, are required for the six SMs in each arm, and the carrier phase angles in the same arm are consecutively shifted by an angle of 60^0. The reference signals for the SMs

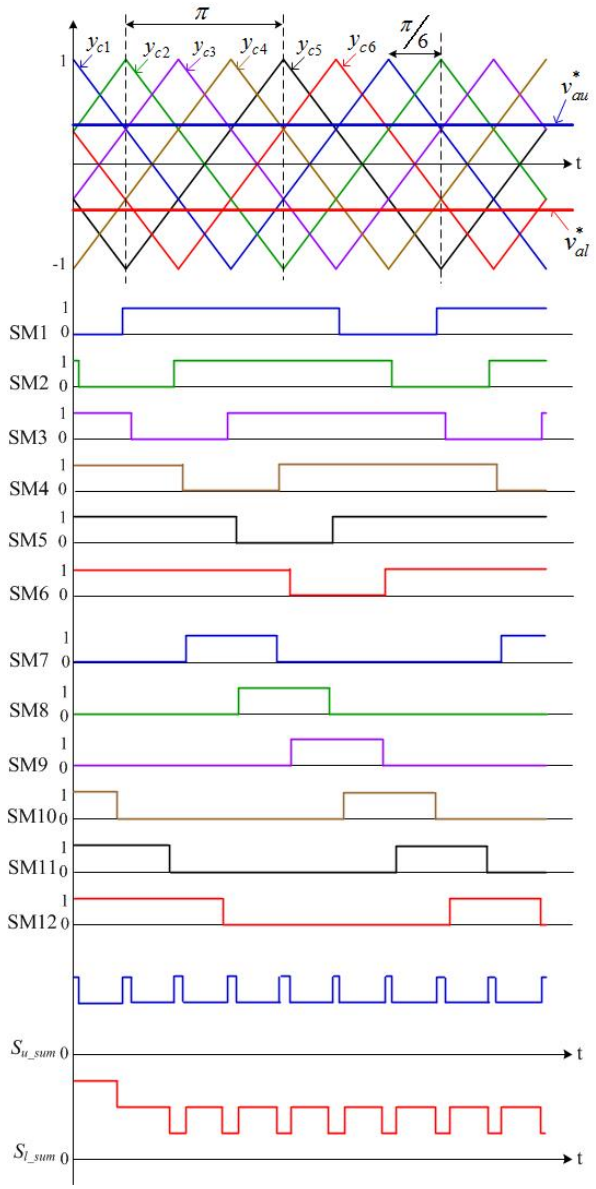

Fig. 5. Scheme of carrier-phase-shift PWM for phase A.

in the upper and lower arms are $v^*_{ai\_u}$ and $v^*_{ai\_l}$, respectively. The gating signals of the switches for the SMs in the converter legs are generated by comparing the reference signals with the corresponding carrier waves. The two waveforms from the bottom of Fig. 5 illustrate the upper and lower arm voltages.

D. Overall Control of the MMC

An MMC-based onshore converter of the HVDC transmission is used to control the HVDC-link voltage to be constant and to regulate the grid voltage through reactive power control. Fig. 6 shows a control block diagram of the MMC, where two cascaded controllers for the HVDC-link voltage and the grid reactive power are used. The main control loops are DC voltage and reactive power controllers, which produce the *dq*-axes current references for the inner

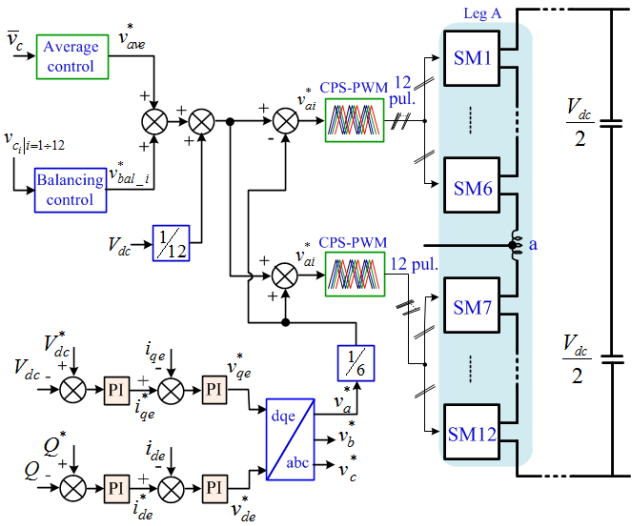

Fig. 6. Overall control block diagram for the MMC.

current control loops in the synchronous reference frame. The outputs of the current controllers are the voltage references for the MMC.

The voltage references, v^*_{ai}, for each SM are expressed in (11) for the upper SM and in (12) for the lower SM in leg-A as:

$$v^*_{ai} = v^*_{ave} + v^*_{bal\_i} - \frac{v^*_a}{6} + \frac{V_{dc}}{12} \quad (i:1\sim 6) \tag{11}$$

$$v^*_{ai} = v^*_{ave} + v^*_{bal\_i} + \frac{v^*_a}{6} + \frac{V_{dc}}{12} \quad (i:7\sim 12) \tag{12}$$

where $v^*_{a\_ave}$ and $v^*_{a\_bal}$ are the voltage commands of the averaging and balancing controls, respectively, as shown in Fig. 4, and v^*_a is the voltage reference for phase A, which is transformed from the *dq*-axes voltage reference produced from the current controllers. An overall control block diagram for one phase of the MMC is shown in Fig. 6, where the CPS-PWM is applied.

IV. Capacitance Estimation of the Submodule Capacitors

A. Reconstruction of the Capacitor Currents

The capacitor current can be estimated from the arm current and the switching states of the submodules, which is expressed as:

$$i_{ci} = S_i \cdot i_{ap} \tag{13}$$

where i_{ci} is the instantaneous current of the i^{th}-SM capacitor, and S_i is "1" or "0" when the upper switch of the i^{th}-SM turns on or off, respectively. Then, the capacitor current can be expressed with the gating time as:

$$i_{ci} = \frac{T_{on\_i}}{T_s} i_{ap} \tag{14}$$

TABLE II
PARAMETERS OF MMC IN HVDC SYSTEM

Parameters	Values
Rated power	300 MW
AC grid voltage	33 kV / 60 Hz
Transformer (Y/Δ)	33/160 kV
DC-link voltage	300 kV
Number of SMs per arm	6
DC voltage of SMs	50 kV
Capacitance o SMs	200 μF
Arm inductance	10 mH
Input filter	0.5 Ω / 60 mH

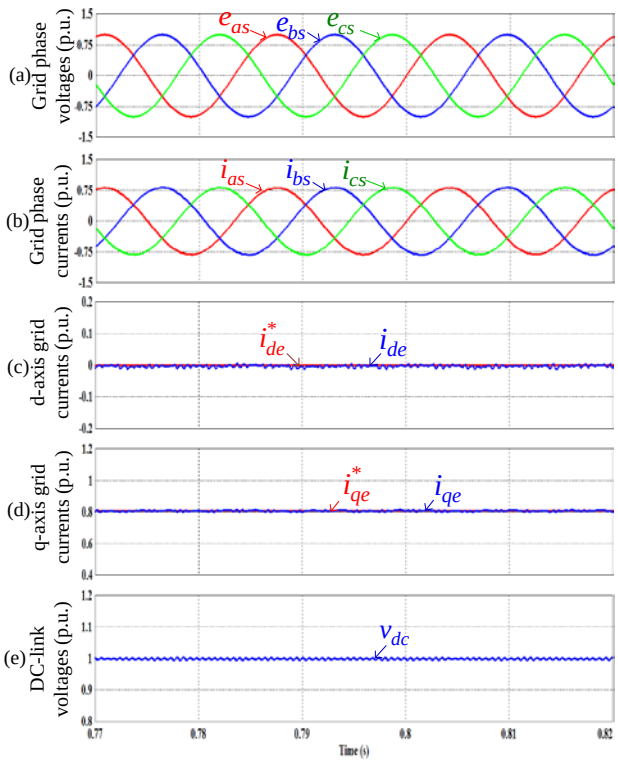

Fig. 7. Performance of grid-connected MMC under the current injection. (a) Grid voltages. (b) Grid phase currents. (c) *d*-axis grid currents. (d) *q*-axis grid currents. (e) HVDC-link voltage.

where T_{on_i} is the turn-on time of the upper switch, and T_s is a switching period of the SM.

B. Estimation of the Capacitance

When regulated AC current is injected into the circulating current loop, the current and voltage in all of the SM capacitors contain ripple components. The relationship between the voltage and current in the capacitor is expressed as:

$$i_{ci} = C_i \frac{dv_{ci}}{dt} = C_i (v_{ci})' \tag{15}$$

where C_i is the capacitance of the i^{th}-SM capacitor.

Then, applying BPFs (band-pass filters) with a 120-Hz cutoff frequency to the measured voltage and the reconstructed current of the SM capacitor, the capacitance,

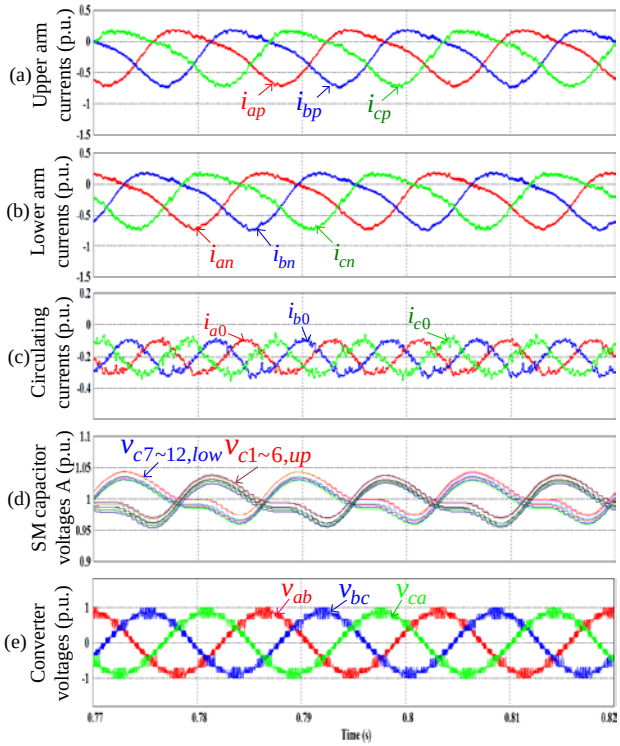

Fig. 8. Operation of MMC under the current injection. (a) Upper-arm currents. (b) Lower-arm currents. (c) Circulating currents. (d) Submodule capacitor voltages in leg A. (e) Line-to-line voltages of MMC.

$\hat{C}_i$, can be obtained by the RLS algorithm as [19]:

$$\begin{aligned}\hat{C}_i(n+1) = \hat{C}_i(n) + \mu(n) BPF[(v_{ci})'(n)] \cdot \\ \left\{ BPF[i_{ci}(n)] - \hat{C}_i(n) BPF[(v_{ci})'(n)] \right\}\end{aligned} \tag{16}$$

where $\mu(n)$ is an adjustment gain, which is chosen as (3×10^{-9}) in this paper by a trial and error method.

For the capacitance estimation, the voltage and current information of the SM capacitor is needed. Therefore, they are sensed and processed by digital filters, as shown in Fig. 4(a). From the estimated capacitance, the deterioration condition of the capacitors is judged. If it is decreased by more than 20% from its initial value, the capacitor needs to be replaced [29]. In this paper, the temperature dependency on the capacitance of the capacitor has not been discussed. However, its effect can be considered easily by measuring the capacitor temperature as described in [19].

V. SIMULATION RESULTS

To verify the effectiveness of the proposed estimation scheme, simulations for a 300-MW 300-kV HVDC transmission system have been carried out. The studied HVDC system, consisting of a 7-level MMC, is integrated to the grid as shown in Fig. 1(b), while the other end of the HVDC system is modeled by a current source representing

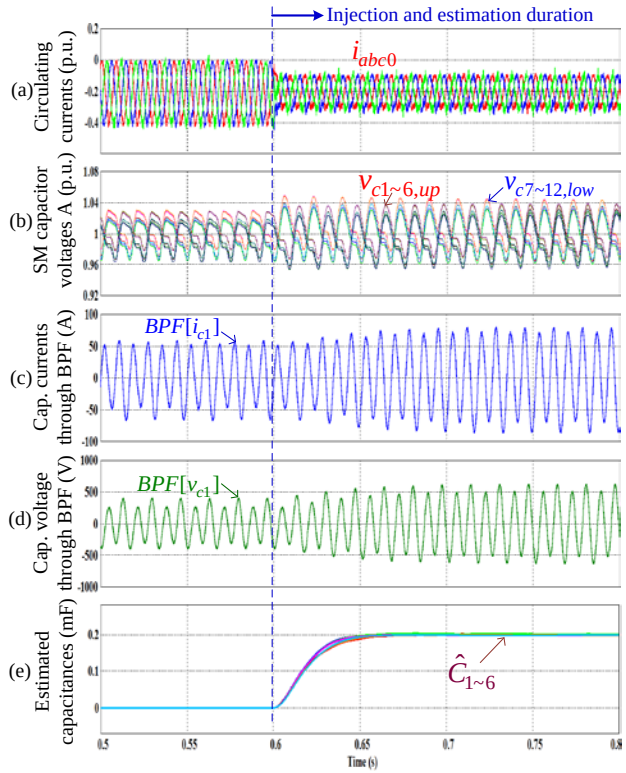

Fig. 9. Capacitance estimation performance. (a) Circulating currents. (b) Submodule capacitor voltages. (c) Capacitor current through BPF at 120 Hz. (d) Capacitor voltage through BPF at 120 Hz. (e) Estimated capacitances.

TABLE III
ERRORS OF ESTIMATED CAPACITANCES IN SIMULATION

Actual values	Estimated values	Error
200 μF	201.9 μF	0.95 %
	200.9 μF	0.45 %
	202.6 μF	1.3 %
	200.2 μF	0.1 %
	200.6 μF	0.3 %
	200.4 μF	0.2 %

wind farm generation. The parameters of the system are listed in Table II, where the DC voltages of the SM capacitors are controlled at 50 kV, and the SM capacitance is selected as 200 μF [30]. The carrier frequency of each SM is 1.25 kHz. In this paper, the frequency and magnitude of the injected currents are chosen as $f_{inj} = 120\,Hz$ and $I_{inj} = 300\,A$, which is about 0.2 p.u. when compared with the current rating at 1,530 A.

Fig. 7 shows the control performance of the grid-connected MMC during current injection at the steady state. The three-phase grid voltages are shown in Fig. 7(a), and the three-phase grid currents are purely sinusoidal and balanced as shown in Fig. 7(b). Fig. 7(c) shows the *d*-axis grid current, which is well controlled at zero for unity power factor operation. The *q*-axis grid current is satisfactorily regulated to control the real power to the grid, which is about 0.8 p.u. as

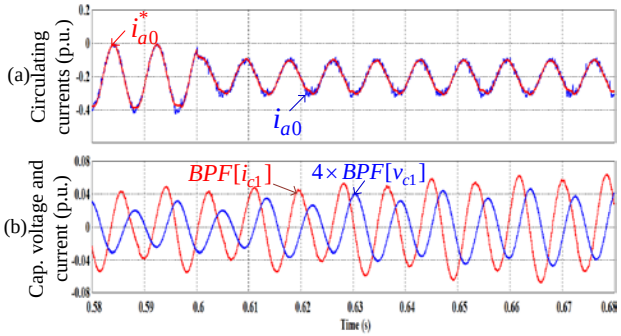

Fig. 10. Circulating current control. (a) Circulating currents in leg A. (b) Capacitor current and voltage through BPF at 120 Hz.

shown in Fig. 7(d). The HVDC-link voltage is shown in Fig. 7(e), which is mostly kept at a nominal value of 300 kV.

The operation of the MMC during current injection is investigated and illustrated in Fig. 8. Fig. 8(a) and (b) show the upper-arm and low-arm currents, which contain the DC, the fundamental, and the injected 120-Hz components. The circulating currents of the three legs of the MMC are shown in Fig. 8(c). They contain dominant 120-Hz components when compared to others. It can be seen in Fig. 8(d) that the submodule capacitor voltages in the upper and lower arms are acceptably balanced with a ripple of less than 5% when compared with the nominal value of 50 kV. It is noted that the ripples of the submodule capacitor voltages are intentionally increased during the capacitance estimation process. The line-to-line voltages of an MMC with 13 levels are shown in Fig. 8(e).

The estimation performance of the SM capacitances is shown in Fig. 9. Fig. 9(a) shows the three-leg circulating currents before and during the current injection, where the circulating currents are reduced by the injected currents when compared with those without injection. However, due to this injection, the voltages of the SM capacitors are increased when compared with those from before the injection, which improves the capacitance estimation accuracy. Fig. 9(c) and (d) shows the signal processing for the capacitor current and voltages, respectively, through the BPFs at a cut-off frequency of 120 Hz. It is obvious that the components of the capacitor current and voltage at 120 Hz during the estimation process are higher than those under normal operation. From the capacitor current and voltage components at 120 Hz, the capacitances of the six upper-arm SM capacitors are calculated in (16) as shown in Fig. 9(e). The estimation errors of the capacitances are listed in Table III, where the maximum is about 1.3%. The control performance of the circulating current is shown in Fig. 10(a), where the actual value tracks the reference value satisfactorily before and during the estimation process. The capacitor current and voltage waveforms through the BPF are shown together in Fig. 10(b).

Fig. 11 shows the performance of the MMC and the

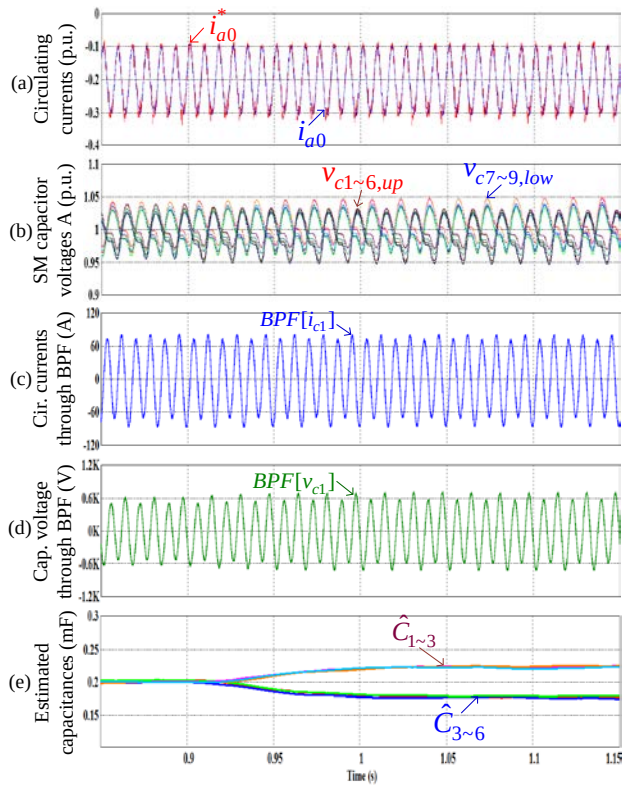

Fig. 11. Capacitance estimation performance in an abrupt variation of capacitors in leg A. (a) Circulating currents. (b) Submodule capacitor voltages. (c) Capacitor current through BPF at 120 Hz. (d) Capacitor voltage through BPF at 120 Hz. (e) Estimated capacitances.

estimation of the SM capacitances in the case of an abrupt variation in the capacitors, where the capacitors $C_1 \sim C_3$ are changed from a nominal value of 200 µF to 225 µF and the capacitors $C_4 \sim C_6$ are changed to 175 µF. The other capacitors are unchanged. Fig. 11(a) shows the circulating currents in leg A, which is still well controlled. Fig. 11(b) shows the SM capacitor voltages, which are slightly changed due to variations of the capacitances. The 120-Hz components of the capacitor current and voltage are shown in Fig. 11(c) and (d), respectively, from which the capacitances are calculated as shown in Fig. 11(e). Under an abrupt variation of the capacitance, the estimation errors are still less than 1.32%.

VI. Experimental Results

Experimental tests were also conducted for a 3-level grid-connected MMC to validate the feasibility of the proposed method. Fig. 12 shows the experimental setup. A TMS320F28335 DSP chip was used to control the IGBT converter including 24 PWM gating signals, which were implemented by a Xilinx FPGA device (XC3S400-PQG208EGQ1321). The carrier frequency of the phase-shift PWM for the SM is 2.5 kHz. The parameters of the MMC are listed in Table IV. The DC-link voltage is controlled at 200 V,

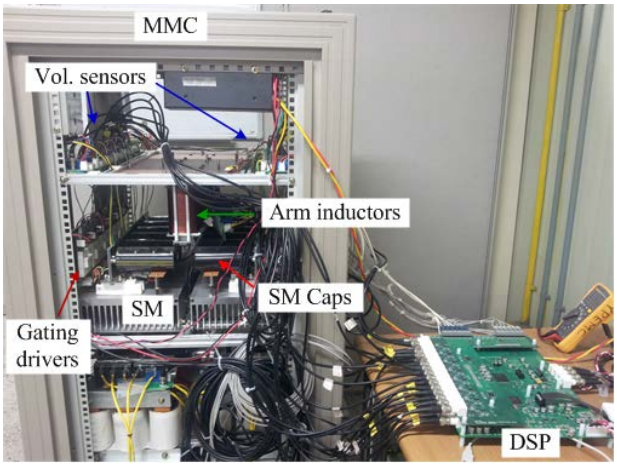

Fig. 12. Experimental setup.

TABLE IV
Parameters of MMC (Experiments)

Parameters	Values
AC grid voltage	120 V / 60 Hz
Number of SMs per arm	2
SM capacitor voltage	100 V
SM capacitance	2,200 µF
Arm inductance	1 mH
Input filter inductance	1 mH
Carrier frequency	2.5 kHz

where the SM capacitor voltages are balanced at 100 V. For the sake of simplicity, only the MMC at one HVDC station is operated and a resistive load is connected to the DC bus.

The control performance of the MMC connected to the grid with currents injected into the circulating current loops is shown in Fig. 13. Fig. 13(a) shows the three-phase grid voltages. The three-phase grid currents are shown in Fig. 13(b), which are mostly sinusoidal and balanced. It can be seen in Fig. 13(c) and (d) that the controllers of the *dq*-axes grid currents work successfully, where the actual currents follow their references. Fig. 13(e) shows the DC-link voltage, which is controlled at 200 V with a ripple of less than 1 V.

Fig. 14 shows the operation of the MMC, where the upper-arm and lower-arm currents are shown in Fig. 14(a) and (b), respectively. It can be seen that harmonics appear in the arm currents due to the injection of AC currents in the circulating current loops. The circulating currents are calculated from the upper-arm and lower arm currents, which are shown in Fig. 14(c). There exists a difference between the waveforms of the arm and circulating currents here and those of Fig. 8 for the simulation test. The reason for this difference is that parameters such as the SM capacitances and arm inductances in the laboratory prototype are not identical, unlike the simulation system. In addition, the performance of the average and balancing controls in the MMC with 3 levels is a lot more degraded than in the 7-level MMC for the simulation test. The SM capacitor voltages are balanced at the nominal value of 100 V as shown in Fig. 14(d). Fig. 14(e) shows the

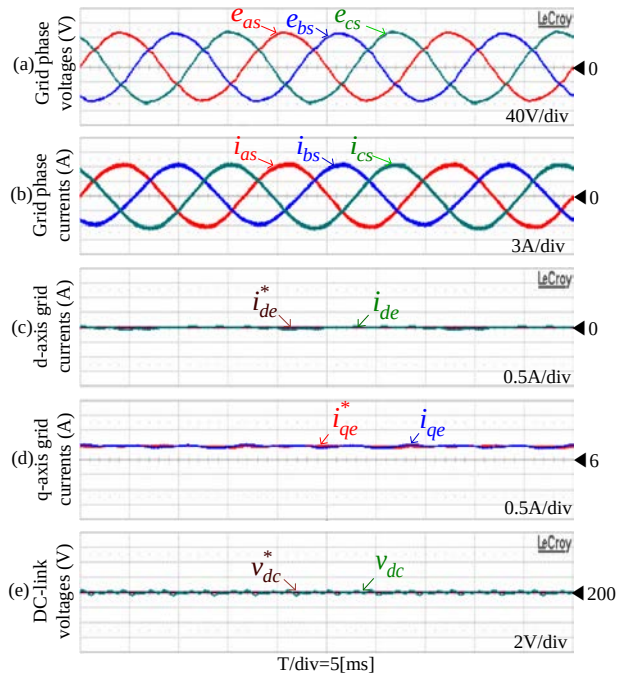

Fig. 13. Performance of grid-connected MMC under the current injection (experiment). (a) Grid voltages. (b) Grid currents. (c) *d*-axis grid currents. (d) *q*-axis grid currents. (e) DC-link voltage.

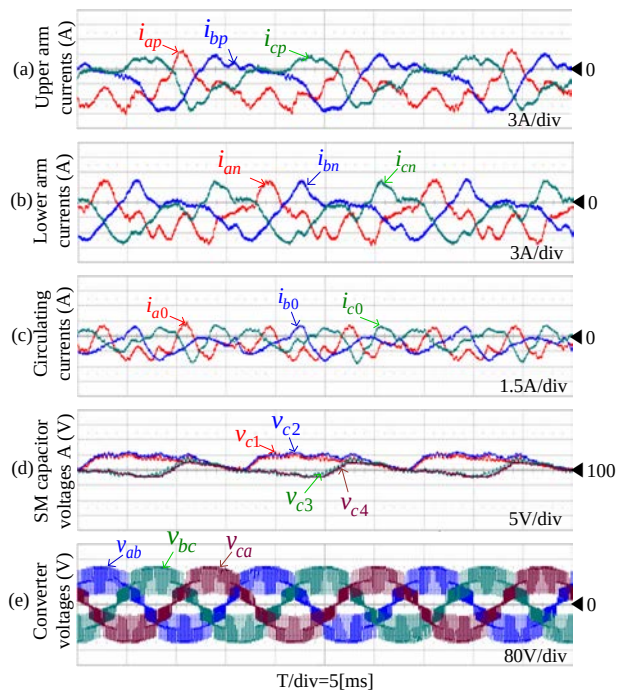

Fig. 14. Operation of MMC under the current injection (experiment). (a) Upper-arm currents. (b) Lower-arm currents. (c) Circulating currents. (d) Submodule capacitor voltages in leg A. (e) Line-to-line voltages of MMC.

line-to-line voltages of the MMC.

Fig. 15 shows the estimation performance of the SM capacitances in a 3-level MMC. Fig. 15(a) shows the three-leg circulating currents before and during the current

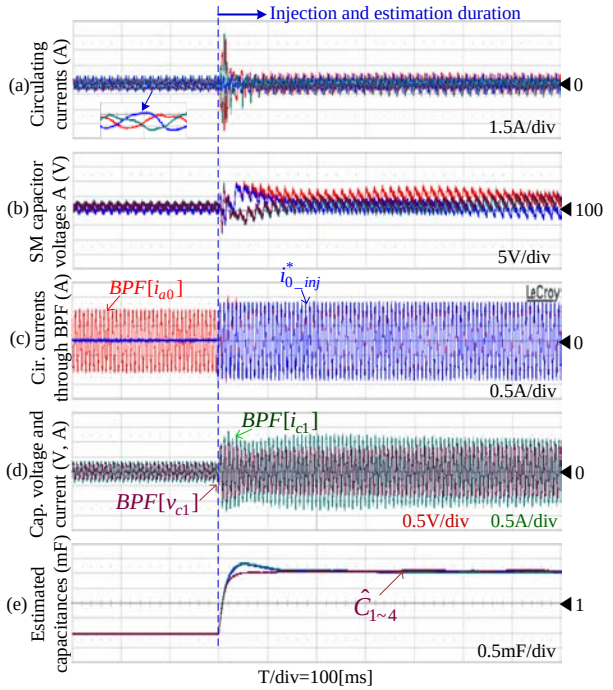

Fig. 15. Capacitance estimation performance (experiment). (a) Circulating currents. (b) Capacitor voltages. (c) Injected current reference and BPF-based circulating current. (d) BPF-based voltage and current of capacitor. (e) Estimated capacitances.

injection, where the ripples of the SM capacitor voltages are increased as shown in Fig. 15(b). It can be seen that the ripple of the capacitor voltages is still in the allowable range, which is balanced around 100 V. Under the transient state, the circulating currents are not well tracked with a high transient value, and an unbalance of the SM capacitor voltages exists during current injection. The reason for the above phenomena is the limited number of SMs of the MMC in the experimental tests, where the performance of the average and balancing controls cannot be simultaneously satisfied perfectly. Fig. 15(c) shows the injected current reference and the leg-A circulating current through the BPF at a cut-off frequency of 120 Hz. In this experiment, the frequency and magnitude of the injected currents are chosen as $f_{inj}=120\,Hz$ and $I_{inj}=1.25\,A$, respectively. It is obvious in Fig. 15(d) that the SM capacitor voltage and current through the 120-Hz BPF during the AC current injection are almost doubled when compared with those without the injection. This considerably improves the capacitance estimation accuracy. The estimated capacitances for the four upper-arm and lower-arm capacitors in leg A are shown in Fig. 15(e). The estimation errors are listed in Table V, which also lists the rated, measured, and estimated capacitances of the four SM capacitors. The maximum estimation error in the experimental tests is about 1.32%.

In Fig. 16, the circulating currents along with the SM capacitor voltage and current passing through the 120-Hz BPFs are shown near the instant of current injection. It can be

TABLE V
ERRORS OF ESTIMATED CAPACITANCES IN EXPERIMENT

Rating C	Measured C	Estimated C	Error
2,200 μF	2,035 μF	2,051 μF	+0.79 %
	2,045 μF	2,018 μF	-1,32 %
	2,043 μF	2,030 μF	-0.63 %
	2,053 μF	2,080 μF	+1.31 %

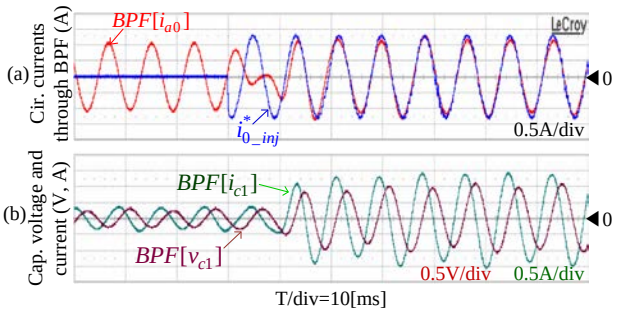

Fig. 16. Circulating current control. (a) Circulating currents in leg A. (b) Capacitor current and voltage through BPF at 120 Hz.

seen in Fig. 16(a) that the control of the circulating current works satisfactorily, where the band-pass-filtered quantity tracks the injected current reference in less than two cycles. According to the injected AC current, the band-pass-filtered voltage and current of the SM capacitors are large enough to obtain a high estimation accuracy, as shown in Fig. 16(b).

It should be noted that the circulating currents depend on the leg voltages of the MMC. Since the output of the average control contains second-order harmonic components, which is the reference for the circulating current PR controllers, the circulating current has a 2nd-order harmonic component even before the injection, as shown in Fig. 15(c) and Fig. 16(a).

VII. CONCLUSIONS

In this paper, an online capacitance estimation scheme for the SM capacitors in the MMCs used for HVDC transmission systems has been presented. This scheme is based on the relationship between the capacitor voltage and current. At first, the regulated AC current is injected into the circulating current loops, which induces voltage and current ripples in the SM capacitors. Then, the capacitor voltages are acquired by sensors, whereas the capacitor currents are reconstructed from the switching states and arm currents without using sensors. Finally, from the voltage and current ripple components, the capacitances are estimated with an RLS algorithm. The proposed method requires no additional hardware, and can be simply implemented by software. From simulation and experimental results, it is shown that the capacitance estimation error is 1.32% at its maximum. Therefore, the condition of the SM capacitors in the MMC can be monitored reliably from the estimated capacitance. The proposed scheme can be also applied to diagnose the fault condition of SM film capacitors in the MMC with a high estimation accuracy.

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