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Novel Voltage Source Converter for 10 kV Class Motor Drives

Mehdi Narimani*, Bin Wu**, and Navid Reza Zargari†

*Department of Electrical and Computer Engineering, McMaster University, Hamilton, Ontario, Canada
**Department of Electrical and Computer Engineering, Ryerson University, Toronto, Ontario, Canada
†Medium-Voltage R&D, Rockwell Automation Canada, Cambridge, Ontario, Canada

Abstract

This paper presents a novel seven-level (7L) voltage source converter for high-power medium-voltage applications. The proposed topology is an H-bridge connection of two nested neutral-point clamped (NNPC) converters and is referred to as an HNNPC converter. This converter exhibits advantageous features, such as operating over a wide range of output voltages, particularly for 10–15 kV applications, without the need to connect power semiconductors in series; high-quality output voltage; and fewer components relative to other classic seven-level topologies. A novel sinusoidal pulse width modulation technique is also developed for the proposed 7L-HNNPC converter to control flying capacitor voltages. One of the main features of the control strategy is the independent application of control to each arm of the converter to significantly reduce the complexity of the controller. The performance of the proposed converter is studied under different operating conditions via MATLAB/Simulink simulation, and its feasibility is evaluated experimentally on a scaled-down prototype converter.

Key words: DC–AC power conversion, Multilevel converter, Sinusoidal pulse width modulation

I. INTRODUCTION

Multilevel converters are attractive for high-power medium-voltage (MV) applications to achieve the desired voltage level and performance [1], [2]. A multilevel converter topology produces a staircase output voltage, which improves output waveforms by decreasing harmonic distortion, thereby improving output filter size. Multilevel topologies also reduce switching losses and *dv*/*dt* across switches, and they can minimize or even eliminate interface transformers [3]. These properties make multilevel converters suitable for a wide range of applications, such as MV motor drives [4], [5], FACTS controllers [6], HVDC transmission systems [7], and grid-connected photovoltaic systems [8].

The three major multilevel voltage source converters (VSCs) are neutral-point clamped (NPC) converters, flying capacitor (FC) converters, and cascaded H-bridge (CHB) converters which called "classic multilevel converters" [2]. Although these converters have significant advantages over conventional two-level VSCs, certain drawbacks limit their applications. For instance, the number of passive components in NPC and FC converters increases significantly with the number of levels. The voltage balancing of capacitors is also a significant problem for high-level converters [2].

The numbers of variants and new multilevel converters have been proposed in the literature [4]-[18]. However, most of these converters are variations of the three classic multilevel topologies or are hybrids of them, which are referred to as "advanced multilevel topologies."

Some of the recent advanced topologies, such as the three-level active NPC (3L-ANPC) and five-level active NPC (5L-ANPC), are considered practical for MV drive applications. They are also commercialized by manufacturers.

The 3L-ANPC is an improved three-level NPC where the clamping diodes are replaced with clamping switches to control loss distribution among the switches of the converter [9], [10]. This topology has the same number of output voltage levels and the same voltage rate of power semiconductor devices compared with three-level NPC. The 5L-ANPC converter is a combined 3L-ANPC and a 3L-FC; it increases the number of output voltage levels [11]-[14]. In

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†Corresponding Author: narimanm@mcmaster.ca
Tel: +1-905-966-1356, McMaster University
*Dept. of Electrical and Computer Eng., Ryerson University, Canada
**Rockwell Automation, Canada

this converter, the voltage rate of power semiconductors is different. Some switches are subjected to half the DC-link voltage, whereas others are subjected to one-fourth the DC-link voltage. This characteristic indicates that the maximum voltage ratings of the power semiconductors in a 3L-ANPC and a 5L-ANPC are the same as that in a 3L-NPC converter and that rates are half of the DC-link voltage. Based on this voltage limitation and the existing power IGBTs in the market, which are limited to 6,500 V, the output AC voltage of these power converters can reach up to 6.6 kV [19], [20].

A new topology called the nested NPC (NNPC) converter is a four-level converter that was recently proposed in [15]. In this topology, all power semiconductors have the same voltage rate, which is one-third the DC-link voltage. This voltage rate helps the converter operate in an increased output voltage of up to 7.2 kV.

For MV drive applications, most installed MV drives operate within 3.3 kV to 7.2 kV because of the aforementioned drawbacks of multilevel topologies, which limit the voltage rating of existing power semiconductors. However, the demands for a high voltage range have increased in the market because a high-voltage power converter can improve the efficiency of an MV drive for high-power applications. Therefore, the next generation of MV drives, called 10 kV class MV drives, is expected to operate within 10 kV to 15 kV.

A solution for the aforementioned drawbacks is the H-bridge connection of two classic 3L-NPCs, which yields a five-level converter called 5L-HNPC [16]-[18]. The output voltage of this structure can be twice as high as that of a conventional NPC converter while maintaining the same voltage rating for power semiconductors. Although the output voltage of a 5L-HNPC can reach up to 10 kV with the existing power semiconductors in the market, the output voltage remains limited to 10 kV, and it cannot reach 10–15 kV.

CHB converters and modular multilevel converters (MMCs) are two practical solutions for 10 kV class drives (10–15 kV range), which employ existing power semiconductors. These solutions allow 10 kV class drives to meet the requirements of high-voltage applications without the need for connecting power semiconductors in series.

The main issue with 10 kV class CHB drives is the number of components, particularly the diode rectifiers, and the number of secondary windings in the phase-shifting transformer. The excessive diode rectifiers can reduce the reliability of the system, and the complex phase-shifting transformer can increase size and weight. These two issues can also increase the cost of the overall power converter and drive system [21]-[23].

A 10 kV class drive with an MMC converter has two main issues: a) circulating current and b) low-frequency operation of the drive [24]-[30]. The circulating current affects the power losses in power semiconductors, which in turn affect the efficiency of the drive system. The MMC converter cannot operate in low-frequency conditions because of the extremely high voltage fluctuations of FCs. The third harmonic [27]-[30] should be injected into the system that generates the common-mode voltage issue on the motor side to improve the performance of an MMC drive.

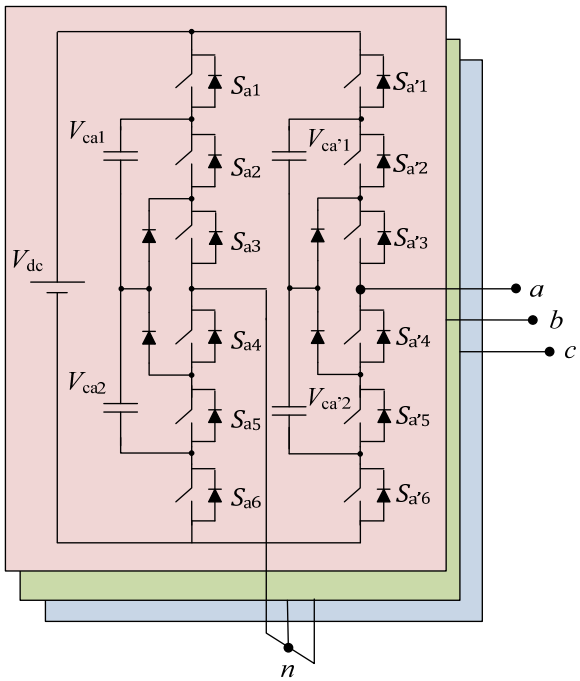


Fig. 1. Proposed HNNPC converter.

The present study proposes a new seven-level topology for 10 kV class (10–15 kV) applications. The proposed topology is an H-bridge connection of two 4L-NNPC converters in each arm. This proposed seven-level H-bridge NNPC (7L-HNNPC) is shown in Fig. 1. The proposed topology has the following features:

- It can operate for a wide range of MV drives, that is, 2.3–15 kV, without the need for power semiconductors connected in series.
- It has fewer power diode rectifiers and a simpler phase-shifting transformer than a CHB converter with the same power rate and output voltage level.
- Unlike an MMC converter, the proposed topology does not suffer from circulating current and low-frequency operation.

Table I compares conventional CHB, MMC, and the proposed HNNPC topology for a 15 kV converter that employs 6.5 kV IGBT.

A novel and simple SPWM technique is developed to control the FC voltages in the 7L-HNNPC converter. This practical technique is not as complex as other techniques.

The operation of the HNNPC converter is explained in Section II. A simple SPWM technique to control and balance

TABLE I
NUMBER OF POWER SWITCHES IN DIFFERENT TOPOLOGIES AND PROPOSED TOPOLOGY IN EACH PHASE

Topology	Number of Switches per phase	Output Voltage Levels	Transformer	
			Secondary Winding	Secondary Cables
CHB [1]	12	7	9	27
MMC [27]	24	13	-	
HNNPC (Proposed)	12	7	6	18

the voltage of FCs is developed in Section III. The simulation studies and experimental results are presented in Sections IV and V, respectively.

II. 7-LEVEL HNNPC CONVERTER

A. Operation of 7-level HNNPC Converter

Fig. 1 shows the structure of the proposed HNNPC converter. In this topology, each phase of the converter consists of two NNPC arms. The first arm is connected to the output terminal, whereas the second arm is connected to the second arms of the other phases. Each phase is supplied with isolated DC sources. In practice, DC sources are often composed of multipulse diode rectifiers.

The NNPC topology [15] is a combination of an FC topology and an NPC topology called an NNPC converter, which provides a four-level output voltage. The capacitors Cx_1 and Cx_2, $x=a, b, c$, in each arm are charged to one-third of the total DC-link voltage to ensure equally spaced steps in the output voltages. A 4L-NNPC topology comprises fewer passive components, such as power diodes and FCs, in comparison with classic four-level topologies [15]. The 4L-NNPC topology is composed of 6 diodes instead of 18 diodes, which are required in a four-level NPC. However, the proposed topology requires six capacitors and is thus different from an FC converter, which comprises nine capacitors.

Each arm in an HNNPC converter can generate four voltage levels from six distinct switching combinations (Table I). Table I shows that two redundant switching states can generate an output voltage of $1/6V_{dc}$ and $-1/6V_{dc}$. Each redundant state provides a specific charging and discharging current path for each FC. This specific feature of redundant switching states helps balance the voltage of the capacitors of each arm.

Table II shows that each NNPC arm can generate four different output voltages (i.e., $V_{dc}/2$, $V_{dc}/6$, $-V_{dc}/6$, and $-V_{dc}/2$). The appropriate combination of the four levels of each arm can result in seven different output voltage levels:
(V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$)
The HNNPC topology exhibits the following features:

- Its output voltage is twice that of a four-level NNPC topology, thus helping to operate the converter in the voltage range of 10–15 kV.
- 7L-HNNPC and 4L-NNPC converters have the same voltage rate of power semiconductors, i.e., $1/3\ V_{dc}$.
- A seven-level output voltage is achieved. Thus, the output voltage quality can be improved.

An HNNPC topology has fewer components than a CHB converter.

III. SPWM TECHNIQUE FOR 7L-HNNPC CONVERTER

In this section, a simple SPWM technique is developed to control the 7L-HNNPC converter and the voltage of FCs.

The proposed approach is a single-phase single-arm modulator based on a sinusoidal pulse width modulation scheme. Three level-shifted triangular carriers are employed on each arm in each phase, and all carriers have the same frequency, amplitude, and phase (in-phase disposition scheme), as in Fig. 2.

Each phase has two modulating signals, which show a 180°

TABLE II
SWITCHING STATES OF A FOUR-LEVEL NNPC TOPOLOGY AND CONTRIBUTION OF THE AC-SIDE CURRENTS TO FC VOLTAGES

State	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{Cx1}	V_{Cx2}	Output Voltage	Output Level
D	1	1	1	0	0	0	No Impact	No Impact	$\frac{V_{dc}}{2}$	3
C2	1	0	1	1	0	0	Charging ($i_x > 0$) Discharging ($i_x < 0$)	No Impact	$\frac{V_{dc}}{6}$	2
C1	0	1	1	0	0	1	Discharging ($i_x > 0$) Charging ($i_x < 0$)	Discharging ($i_x > 0$) Charging ($i_x < 0$)		
B2	1	0	0	1	1	0	Charging ($i_x > 0$) Discharging ($i_x < 0$)	Charging ($i_x > 0$) Discharging ($i_x < 0$)	$-\frac{V_{dc}}{6}$	1
B1	0	0	1	1	0	1	No Impact	Discharging ($i_x > 0$) Charging ($i_x < 0$)		
A	0	0	0	1	1	1	No Impact	No Impact	$-\frac{V_{dc}}{2}$	0

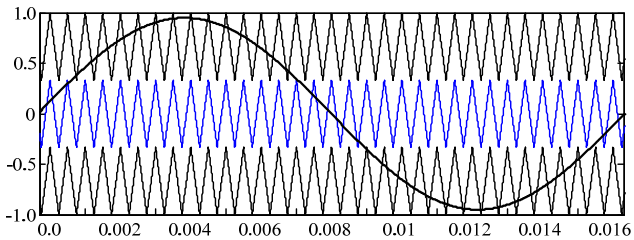


Fig. 2. Level-shifted multicarrier modulation for a 4L-NNPC inverter.

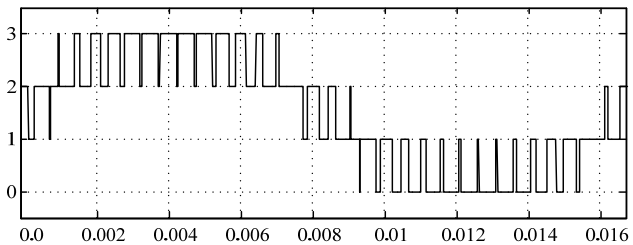


Fig. 3. Desired output levels based on modulating signal.

phase shift with respect to each other. The modulating signals for different phases have a ±120° phase shift with respect to each other. The modulating signal and three carriers are compared to generate the gating signals for each arm and thereby obtain the desired output levels (Fig. 3). The corresponding switching state can be chosen from Table II on the basis of the desired output level at each sampling time. It can then be applied to the power switches.

Table II indicates that two redundant switching states can be applied for output levels 1 and 2. The redundant switching states can be selected to charge or discharge the FCs and thereby minimize the difference between the nominal and measured voltage values.

Table III shows how the appropriate switching state can be selected for output levels 1 and 2. First, the direction of the output current of each arm is measured. The deviations of the capacitor voltages are then determined as follows:

$$\Delta V_{CXi} = V_{CXi} - V_{dc} / 3, \quad (1)$$
$$x = a, a', b, b', c, c'; \quad i = 1, 2;$$

where V_{CXi} is the measured capacitor voltage, $V_{dc}/3$ is the nominal value, and ΔV_{CXi} denotes the deviations of the capacitor voltages. The deviation ΔV_{CXi} should be close to zero to achieve capacitor voltage balance.

On the basis of the output current direction and FC voltage deviation from their nominal values, the appropriate switching states can be selected and applied to the HNNPC converter. For example, if the desired output level is 1 and the arm current is positive, $\Delta V_{CX1} < 0$ and $\Delta V_{CX2} < 0$ are assumed. This scenario indicates that both capacitors must be charged. According to Table II, State B2 [1 0 0 1 1 0] should be selected and applied to the power switches. With this strategy, the proposed balancing method can be used (Table III).

According to Tables II and III, the following procedure should be followed to control FC voltages:

1- The desired output level should be determined by comparing the carriers and modulation signal (Fig. 3).
2- Phase current direction and FC voltages should be measured to determine the capacitor voltage deviation based on (1).
3- Finally, the appropriate switching state can be selected from Table II, and the corresponding gating signals can be applied to the power semiconductors.

TABLE III
PROPOSED VOLTAGE BALANCING METHOD

Output Level	i_x	ΔV_{CX1}	ΔV_{CX2}	Condition	State
1	≥ 0	≥ 0	≥ 0	-	B1
			< 0	-	B2
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	B1
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	B2
			< 0	-	B2
	< 0	≥ 0	≥ 0	-	B2
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	B1
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	B2
		< 0	≥ 0	-	B2
			< 0	-	B1
2	≥ 0	≥ 0	≥ 0	-	C1
			< 0	-	C1
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	C1
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	C2
			< 0	-	C2
	< 0	≥ 0	≥ 0	-	C2
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	C1
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	C2
		< 0	≥ 0	-	C1
			< 0	-	C1

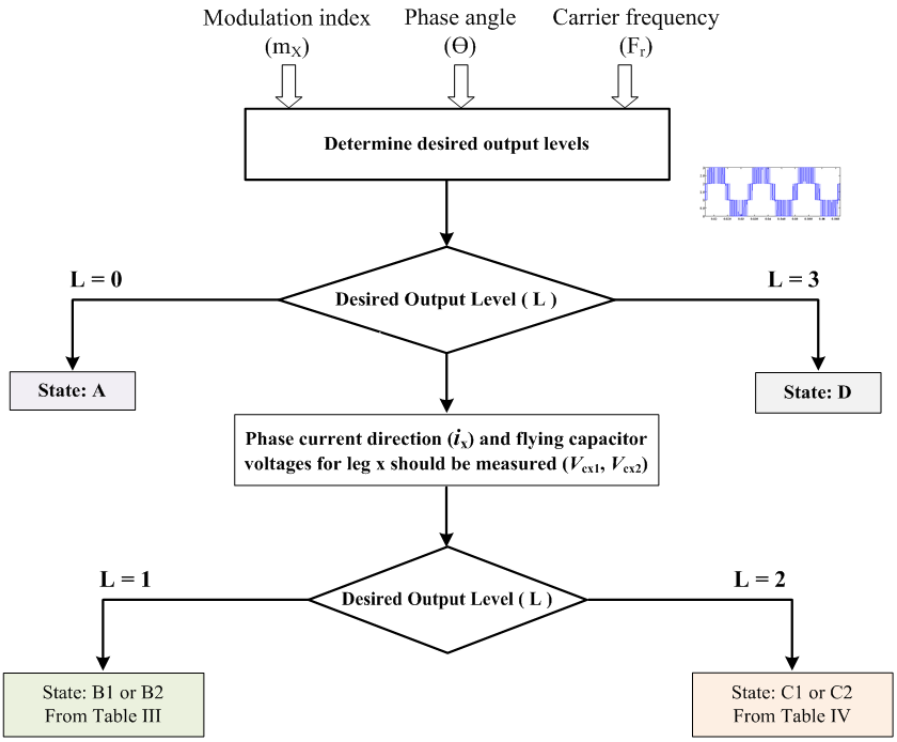


Fig. 4. Block diagram of the proposed SPWM approach for leg *x* (*x* = *a*, *a'*, *b*, *b'*, *c*, *c'*).

The flowchart shown in Fig. 4 illustrates the procedure for controlling the voltage of FCs in each leg. First, the modulating signal for phase x (x=*a*, *a'*, *b*, *b'*, *c*, *c'*) is compared with that for the carriers (four carriers). The desired output levels are then determined. If the desired output level (L) is 0 or 3, then the corresponding switching state is State A or D (Table II), respectively. Otherwise, the capacitor voltages V_{CX1} and V_{CX2} and phase current i_X should be measured. The appropriate switching state should then be selected from Table III on the basis of the output level (L).

This procedure can be implemented for each arm of each phase, with the difference being the phase shifting among the modulation signals. Table II shows that the implementation of the proposed technique in controlling FC voltages is relatively simple in practical applications.

The proposed 7L-HNNPC converter shows redundancy in switch combinations to produce output levels (Table II). Two redundant switching states are applied to generate voltage levels of 1/6 V_{dc} and −1/6 V_{dc} for each leg. Each redundant state provides a specific charging and discharging current path for each floating capacitor that helps achieve capacitor voltage balance based on Table III. Therefore, many redundant switching states exist, and balancing the FC voltages in all operating conditions is possible at different load power factors and modulation indexes.

IV. Simulation Results

Simulation studies are conducted in MATLAB/Simulink to demonstrate the performance of the proposed 7L-HNNPC converter and SPWM approach. The simulations also demonstrate the effectiveness of the developed SPWM in generating output voltages and regulating FC voltages. A 10 MVA, 15 kV power converter is considered.

The parameters used in the simulation studies are presented in Table IV. The performance of the proposed SPWM controller is studied for steady-state and transient-state conditions.

A. Steady-state Analysis

Figs. 5 and 6 show the performance of the 7L-HNNPC converter via the SPWM technique with different modulation indexes. Fig. 5 shows the inverter output voltage, output currents, and FC voltages; here, the modulation index *m* is 0.95, and the output voltage has a THD of 17.15%, and the current THD is 2.5%.

Fig. 6 also shows the inverter output voltage, output currents, and FC voltages; here, the modulation index *m* is 0.5, the output voltage has a THD of 29.8%, and the current

TABLE IV
Parameters of the Simulation Study

Converter Parameters	Values	Values (p.u)
Converter Rating	10 MVA	1.0
Output Voltage	15 kV	1.0
Flying Capacitors	1000 µF	10
Input DC Voltage	11.8 kV	-
Output Frequency	60 Hz	1.0

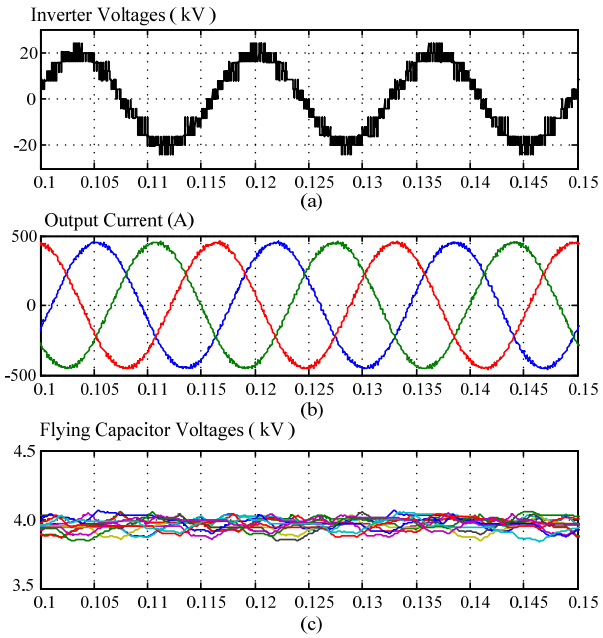


Fig. 5. Simulation waveforms: (a) inverter output voltage, (b) output currents, (c) FC voltages (m = 0.95, PF = 0.9).

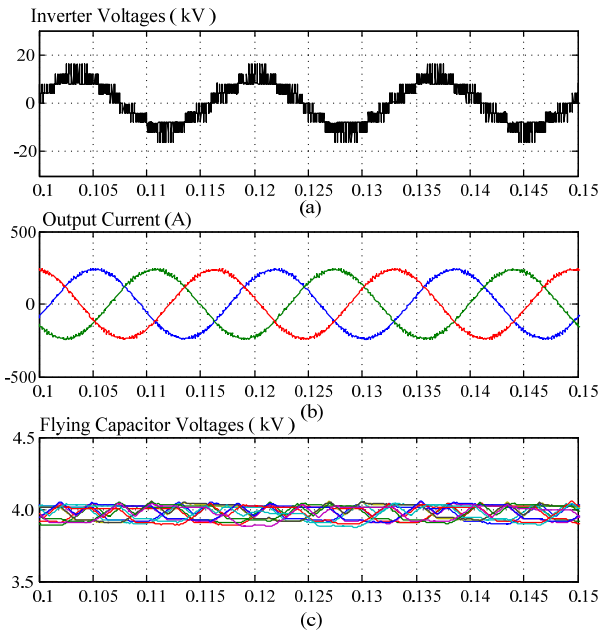


Fig. 6. Simulation waveforms: (a) inverter output voltage, (b) output currents, (c) voltage of FCs (m = 0.5, PF = 0.9).

THD is 3.5%.

The AC output voltage is 15 kV, the DC-link voltage is 12 kV, and the voltage stress across the power semiconductors is 1/3 V_{dc} = 4 kV. In a real converter used in practice, the power semiconductors have a 35%–45% margin in terms of voltage rate. Therefore, considering even a 45% margin, 6.5 kV IGBT can be applied to a 15 kV motor drive [31], [32].

B. Transient-state Analysis

A load step change is studied to evaluate the performance of the proposed SPWM controller. In this case, a step change from half load to full load, where m = 0.95, is applied to the converter. Fig. 7 shows the performance of the controller that can maintain FC voltages at nominal values.

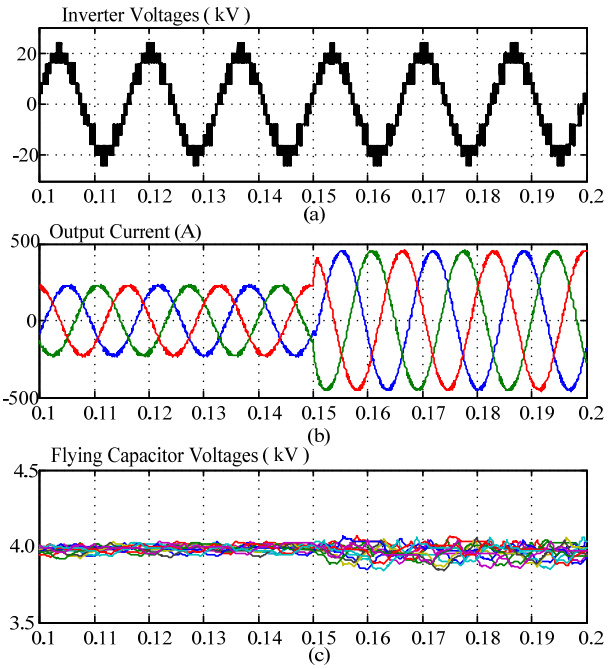


Fig. 7. Simulation waveforms: (a) inverter output voltage, (b) output currents, (c) FC voltages (step change from half load to full load, m = 0.95, PF = 0.9).

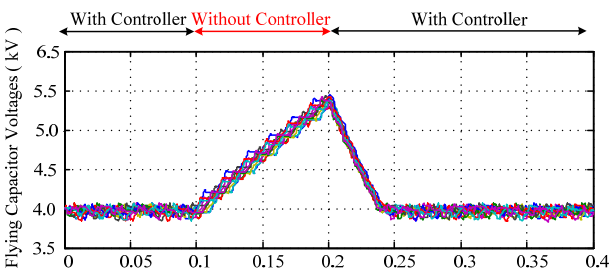


Fig. 8. Voltage of FCs with and without controller.

C. Evaluation of the Controller

In this case, the HNNPC converter presumably operates under normal operating conditions, and the controller is suddenly deactivated at t = 0.1 s, which means that the flowchart (Fig. 4) is not applied and that conventional SPWM is employed.

The controller reactivates at t = 0.15 s. Fig. 8 shows that the capacitor voltages increase when the controller is deactivated and that the capacitor voltages start to be controlled at nominal values when the controller reactivates. This study shows the performance of the controller scheme described in Table II.

V. EXPERIMENTAL RESULTS

The feasibility of the proposed 7L-HNNPC converter and

TABLE V
PARAMETERS OF THE STUDY (EXPERIMENTS)

Converter Parameters	Values	Values (p.u)
Converter Rating	5 kVA	1.0
Output Voltage	208 V	1.0
Flying Capacitors	2000 µF	10
Input DC Voltage	120 V	-
Output Frequency	60 Hz	1.0

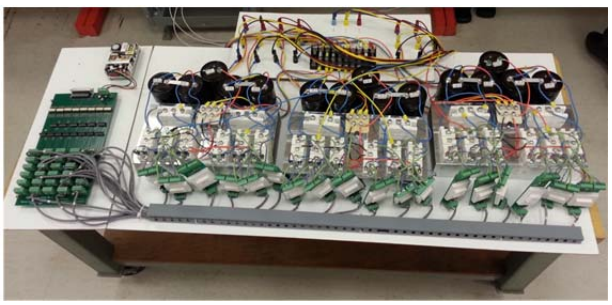


Fig. 9. Experimental setup for the proposed HNNPC Converter.

SPWM approach is evaluated experimentally. The parameters in Table V are used to obtain the experimental results from a scaled-down prototype. The experimental setup for the converter is shown in Fig. 9.

A phase shifting transformer is employed on the grid side to implement the three isolated DC sources. The phase shifting transformer is a 10 kVA/208 V transformer with three secondary windings and phase shifting of 0°, −20°, and −40°).

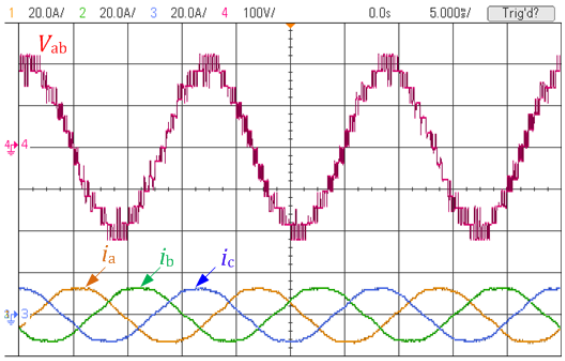
The converter switches, clamping diodes, and gate drivers are developed by Semikron SKM75GB123D, SKKD75F12, and SKHI22B, respectively. SPWM technique is implemented with a dSpace DS1103 rapid prototyping board, and the gating signals are sent to the converters through an interface board consisting of MC14504BCP and TLP521-4. MC14504BCP is a level shifter that shifts a TTL signal to CMOS logic levels. TLP521-4 is an optocoupler used to isolate the signals from the power circuit.

Figs. 10 and 11 show the performance of the proposed converter under different operating conditions. Fig. 10 shows the inverter output voltage, output currents, and FC voltages; here, the modulation index m is 0.95, the output voltage has a THD of 17.8%, and the current THD is 2.8%.

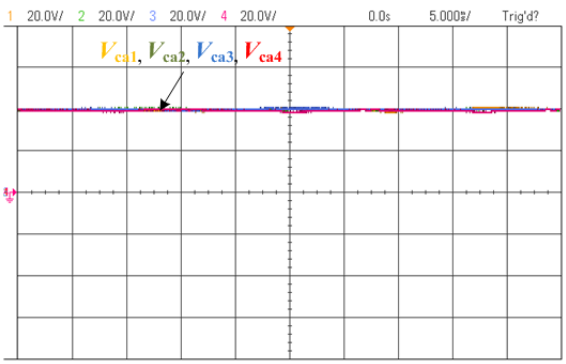
Fig. 11 also shows the inverter output voltage, output currents, and FC voltages; here, the modulation index m is 0.5, the output voltage has a THD of 30.9%, and the current THD is 3.75%.

Fig. 12 shows the performance of the proposed converter under transient conditions when the load changes from half load to full load. Figs. 10 to 12 show that the capacitor voltages are balanced in all cases.

Fig. 13 shows the controller performance. The capacitors start charging if no control exists on the capacitor voltages,

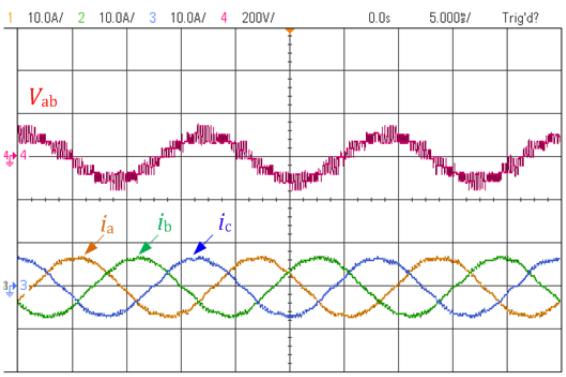


(a) Inverter voltage and output currents.

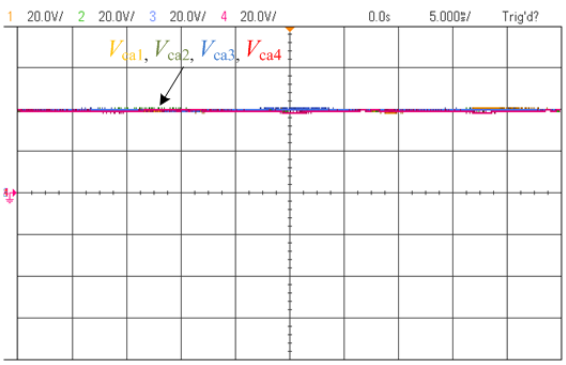


(b) FC voltages.

Fig. 10. Experimental waveforms for HNNPC converter at steady-state condition, m = 0.95, and PF = 0.9.

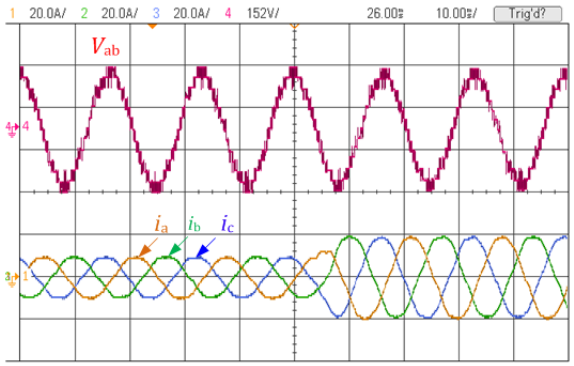


(a) Inverter voltage and output currents.

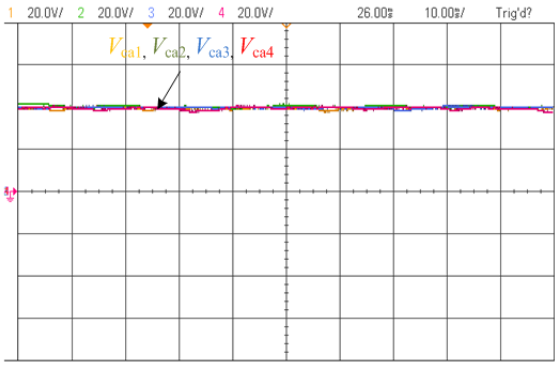


(b) FC voltages.

Fig. 11. Experimental waveforms for HNNPC converter at steady-state condition, m = 0.5, and PF = 0.9.



(a) Inverter voltage and output currents



(b) FC voltages

Fig. 12. Experimental waveforms for HNNPC converter at transient-state condition when the load changes from half load to full load (m = 0.95 and PF = 0.9).

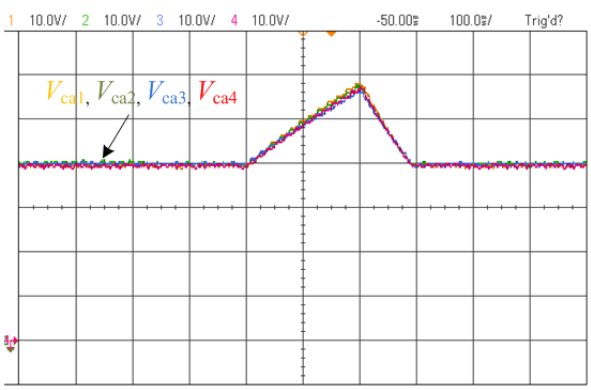


Fig. 13. Experimental waveforms for HNNPC converter with and without a controller (m = 0.95).

and their voltages increase. The capacitor voltages return to the nominal values when the controller is reactivated.

The experimental results match the simulation results well.

VI. Conclusions

This paper presents a new seven-level VSC for high-power MV applications. The proposed HNNPC topology is an H-Bridge connection of two NNPC converters. The main feature of the converter is that it can operate over a wide range of voltages (2.3–15 kV) using available power semiconductors without the need for power semiconductors connected in series. The number of components in the proposed topology is fewer than that in the classic multilevel topology with the same voltage rate. The line-to-line output voltage has 13 levels. The output filter can also be minimized or eliminated entirely in some applications because of the high-quality line-to-line waveform.

A novel SPWM technique is developed for the proposed converter to control FC voltages. This controller can be applied independently to each converter arm, thereby reducing complexity. The proposed converter is tested under different operating conditions in a MATLAB/Simulink environment, and its feasibility is evaluated experimentally on a scaled-down prototype.

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Mehdi Narimani received his Ph.D. degree in Electrical Engineering from the University of Western Ontario, Canada, in 2012. He is currently an Assistant Professor at the Department of Electrical and Computer Engineering at McMaster University, Hamilton, Canada. He is the author of more than 55 journal and conference proceeding papers and four patents (issued/pending review). His current research interests include high power converters, control of power electronics, and renewable energy systems.

Bin Wu received his Ph.D. degree in Electrical and Computer Engineering from the University of Toronto, Canada, in 1993. After working at Rockwell Automation Canada, he joined Ryerson University, Toronto, Canada, where he is currently a Professor and NSERC/Rockwell Industrial Research Chair in Power Electronics and Electric Drives. Dr. Wu received the Gold Medal of the Governor General of Canada, the Premier's Research Excellence Award, Ryerson Distinguished Scholar Award, and the NSERC Synergy Award for Innovation. He is a fellow of Engineering Institute of Canada (EIC) and Canadian Academy of Engineering (CAE).

Navid Reza Zargari received his Ph.D. degree from Concordia University, Montreal, Canada, in 1995. He has been with Rockwell Automation Canada since November 1994 as a Manager of the Medium Voltage R&D department. Dr. Zargari is a Senior member of IEEE. He has co-authored more than 80 research papers and holds 20 US patents. His research interests include power converter topologies and their control aspects, power semiconductors, and renewable energy sources. He received the Premier's Innovation Award in 2009 from the Province of Ontario. In 2011 he co-authored a book on Power Conversion and Control of Wind Energy Systems.