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Topologies of Active-Switched Quasi-Z-source Inverters with High-Boost Capability

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Abstract

This paper proposes both an active-switched quasi-Z-source inverter (AS-qZSI) and an extended active-switched qZSI (EAS-qZSI), which are based on the classic qZSI. The proposed AS-qZSI adds only one active switch and one diode to the classic qZSI for increasing the voltage boost capability. Compared with other topologies based on the switched-inductor/capacitor qZSI, the proposed AS-qZSI requires fewer passive components in the impedance network under the same boost capability. Additionally, the proposed EAS-qZSI is designed by adding one inductor and three diodes to the AS-qZSI, which offers enhanced boost capability and lower voltage stress across the switches. The performances of the two proposed topologies are verified by simulation and experimental results obtained from a prototype with a 32-bit DSP built in a laboratory.

Keywords: Active switch, Quasi-Z-source inverters, Switched inductor, Voltage boost capability

I. INTRODUCTION

A conventional voltage source inverter can achieve voltage step-down operations because its peak ac output voltage is lower than the dc input voltage. Therefore, an extra dc boost converter is connected between the dc input voltage and the inverter to increase the dc-link voltage across the inverter bridge. To overcome the constraints of a conventional inverter, a quasi-Z-source inverter (qZSI) was presented in [1]. The qZSI can boost the dc-link voltage by controlling the shoot-through state of the inverter leg and can draw continuous input current without an additional capacitor for filtering. The qZSI is suited to renewable power generations and fuel-cell vehicles due to its voltage boost capability with a single-power stage [2]-[5]. However, the usable boost factor of the qZSI is generally limited due to a narrow shoot-through state range. This condition brings difficulties to further qZSI applications, which require a power converter with a high voltage gain.

Recently, several dc-dc conversion schemes based on the quasi-Z-source impedance network have been introduced in order to enhance the boosting capability. In [6]-[10], the switched-inductor (SL) / switched-capacitor (SC) structures are developed by adding extra inductors / capacitors and diodes in the quasi-Z-source impedance network, and a hybrid SL/SC topology is proposed. To further improve the boost capability, additional cells are serially connected at the qZSI [11], [12]. However, more inductors and/or capacitors at the impedance network are needed to further boost the voltage, and this condition will increase the volume and cost of the power converter. The ZSI-based topology is presented for reducing capacitor voltage stress and suppressing a high start-up current [13]. The topology to add one switching device and one diode to a classic qZSI is proposed in [14]. The number of passive components in the impedance network can be reduced. However, the boost factor may not be enough for renewable power generation.

In this paper, two types of topologies, namely, an active-switched qZSI (AS-qZSI) and an extended active-switched qZSI (EAS-qZSI) are proposed. The proposed topologies offer high boost capability and low voltage stress across the switches. The operating principles and a comparison with other topologies based on the switched inductor/capacitor qZSI declare the performances of the proposed topologies. Such performances are verified by the simulation and experimental results.

II. REVIEW OF CLASSIC QZSI AND MODIFIED TOPOLOGIES

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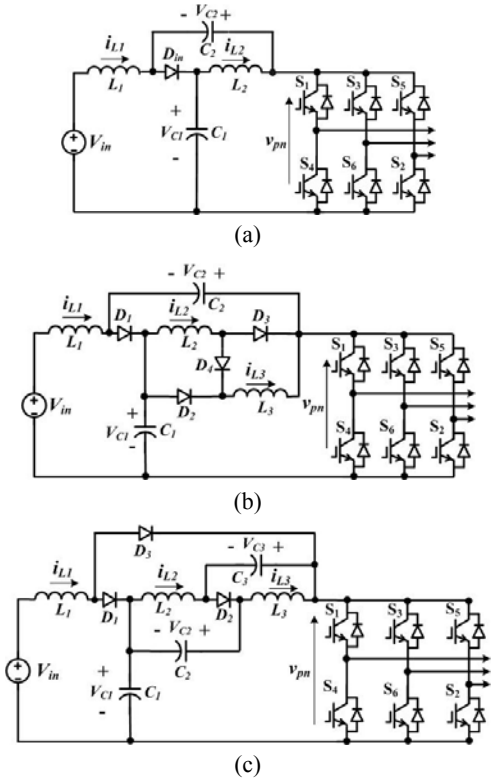


Fig. 1. Classic qZSI and modified topologies. (a) Classic qZSI. (b) Switched-inductor qZSI (SL-qZSI). (c) Continuous- current diode-assisted extended boost qZSI (DA-qZSI).

Both the classic qZSI and modified topologies based on the classic qZSI structure are shown in Fig. 1. Fig. 1(a) shows the classic qZSI, which has a continuous input current and a lower capacitor voltage stress [1]. The boost factor, defined as the ratio of the peak dc-link voltage across the inverter leg $\hat{v}_{pn}$ to the dc input voltage V_{in}, is given by

$$B = \frac{\hat{v}_{pn}}{V_{in}} = \frac{1}{1-2(T_{sh}/T_s)} = \frac{1}{1-2D} \tag{1}$$

where T_{sh} is the shoot-through time during a switching period T_s, and $D = T_{sh}/T_s$ is the shoot-through duty ratio.

Fig. 1(b) shows a modified topology based on a qZSI structure called a switched-inductor quasi-ZSI (SL-qZSI). This topology was proposed in [8]. In a SL-qZSI, the three diodes and one inductor are added to the impedance network of the classic qZSI. The SL-qZSI has a SL structure for raising the boost factor and reducing the in-rush current, and its boost factor is given by

$$B = \frac{1+D}{1-2D-D^2}. \tag{2}$$

Fig. 1(c) shows a continuous-current diode-assisted extended-boost qZSI (DA-qZSI). This topology was proposed in [6]. It can be extended to have a higher boost ability by connecting more cells in serial. The boost factor of the DA-qZSI is given by

$$B = \frac{1}{1-3D+2D^2}. \tag{3}$$

III. Operation Principles of the Proposed Topologies

The operation principles for the two types of proposed topologies, AS-qZSI and EAS-qZSI, will be described, respectively.

A. Operation of the AS-qZSI

Fig. 2 shows the proposed AS-qZSI, where one active switch (S_7) and one diode (D_0) are inserted in the impedance network of the classic qZSI. The proposed AS-qZSI has an extra shoot-through state in addition to the non-shoot-through state, which are the same operating states of the classic qZSI. Therefore, similar to the classic qZSI, the AS-qZSI has two operating states. Fig. 3 shows equivalent circuits of the AS-qZSI in the shoot-through state and the non-shoot-through state.

Shoot-through state: In the shoot-through state for an interval of DT_s, the dc-link across the inverter leg is shorted by turning on the upper and lower switches for any of the phase legs, and the switching device S_7 is switched on. The diodes D_o and D_1 are off. The energies stored at two capacitors C_1 and C_2 are supplied to the two inductors L_1 and L_2 during this state. From Fig. 3(a), the two inductor voltages v_{L1} and v_{L2}, and the dc-link voltage v_{pn} can be written as follows, respectively:

$$v_{L1} = V_{c2} + V_{in} \tag{4}$$

$$v_{L2} = V_{c1} \tag{5}$$

$$v_{pn} = 0 \tag{6}$$

Non-shoot-through state: In the non-shoot-through state for an interval of $(1\text{-}D)T_s$, the circuit operates like a conventional inverter, and the switching device S_7 is switched off. The diodes D_o and D_1 are in the conduction state. The energy stored at the two inductors is delivered to the two capacitors and the dc-link side. Thus, the two inductors are discharged and the two capacitors are charged during this state. From Fig. 3(b), the two inductor voltages v_{L1} and v_{L2}, and the dc-link voltage v_{pn} can be written as follows, respectively:

$$v_{L1} = V_{c2} - V_{c1} + V_{in} \tag{7}$$

$$v_{L2} = -V_{c2} \tag{8}$$

$$v_{pn} = V_{c1} \tag{9}$$

Applying the volt-second balance principle to each inductor L_1 and L_2 from (4), (5), (7), and (8), the two capacitor voltages V_{c1} and V_{c2} can be obtained as a function of D as follows, respectively:

$$V_{c1} = \frac{1-D}{1-3D+D^2} V_{in} \tag{10}$$

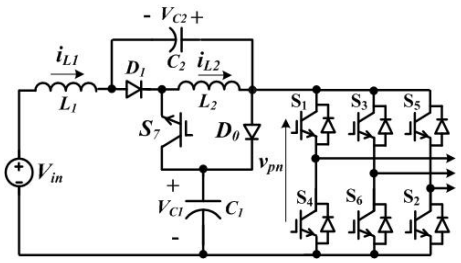
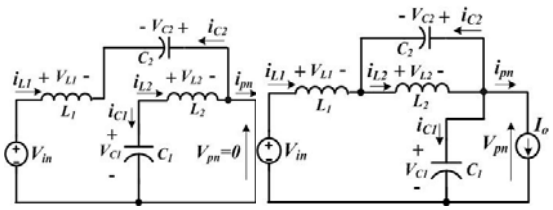


Fig. 2. Schematic circuit of the proposed AS-qZSI.



(a) (b)

Fig. 3. Equivalent circuits of the proposed AS-qZSI. (a) Shoot-through state. (b) Non-shoot-through state.

$$V_{c2} = \frac{D}{1-3D+D^2} V_{in} \tag{11}$$

Considering that the peak dc-link voltage $\hat{v}_{pn}$ is identical with the capacitor voltage V_{c1}, the boost factor of the AS-qZSI can be expressed as

$$B = \frac{\hat{v}_{pn}}{V_{in}} = \frac{V_{c1}}{V_{in}} = \frac{1-D}{1-3D+D^2}. \tag{12}$$

B. Operation of the EAS-qZSI

Fig. 4 shows the proposed EAS-qZSI, in which one inductor (L_3) and three diodes (D_2, D_3, D_4) are added to the AS-qZSI to further enhance the boost capability. Similar with the AS-qZSI, the EAS-qZSI has two operation modes: the shoot-through state and the non-shoot-through state. Fig. 5 shows equivalent circuits of the EAS-qZSI in the shoot-through state and non-shoot-through state.

1) Shoot-Through State: In the shoot-through state for an interval of DT_s, the dc-link across the inverter leg is shorted by turning on the upper and lower switches for any of the phase legs, and the switching device S_7 is switched on, just like the AS-qZSI. The diodes D_2 and D_3 are in the conduction state, whereas diodes D_o, D_1, and D_4 are in the blocking state. The two inductors L_2 and L_3 are connected in parallel, and they store energy from capacitor C_1. The inductor L_1 stores the energy from both capacitor C_2 and the dc input voltage V_{in}. Therefore, the two capacitors C_1 and C_2 are discharged, and the three inductors L_1, L_2, and L_3 are charged during this state. From Fig. 5(a), the three inductor voltages v_{L1}, v_{L2}, and v_{L3}, the dc-link voltage v_{pn}, and the capacitor current i_{c1} can be written as follows, respectively:

$$v_{L1} = V_{c2} + V_{in} \tag{13}$$

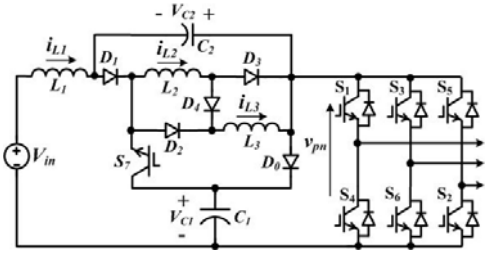
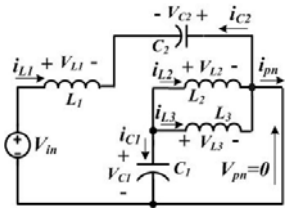
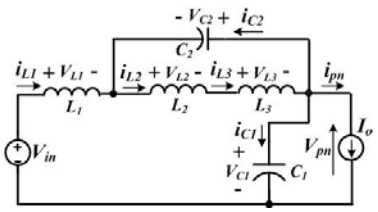


Fig. 4. Schematic circuit of the proposed EAS-qZSI.



(a)



(b)

Fig. 5. Equivalent circuits of the proposed EAS-qZSI. (a) Shoot-through state. (b) Non-shoot-through state.

$$v_{L2} = v_{L3} = V_{c1} \tag{14}$$

$$v_{pn} = 0 \tag{15}$$

$$i_{c1} = -(i_{L2} + i_{L3}) \tag{16}$$

2) Non-Shoot-Through State: In the non-shoot-through state for an interval of $(1\text{-}D)T_s$, the circuit operates just like a conventional voltage source inverter, and the switching device S_7 is switched off. The diodes D_o, D_1, and D_4 are in the conduction state, whereas the diodes D_2 and D_3 are in the blocking state. The two inductors L_2 and L_3 are serially connected, and the energy stored at the three inductors is supplied to the two capacitors and the dc-link side. Thus, the three inductors are discharged and the two capacitors are charged. From Fig. 5(b), the three inductor voltages, the dc-link voltage, and the capacitor current can be written as follows, respectively:

$$v_{L1} = V_{c2} - V_{c1} + V_{in} \tag{17}$$

$$v_{L2} = V_{c2} - v_{L3} \tag{18}$$

$$v_{pn} = V_{c1} \tag{19}$$

$$i_{c1} = i_{L1} - I_o \tag{20}$$

Assuming that $L_2 = L_3$, it follows that $v_{L2} = v_{L3}$ and $i_{L2} = i_{L3}$. Applying the volt-second balance principle to each inductor L_1 and L_2 from (13), (14), (17), and (18), the two capacitor

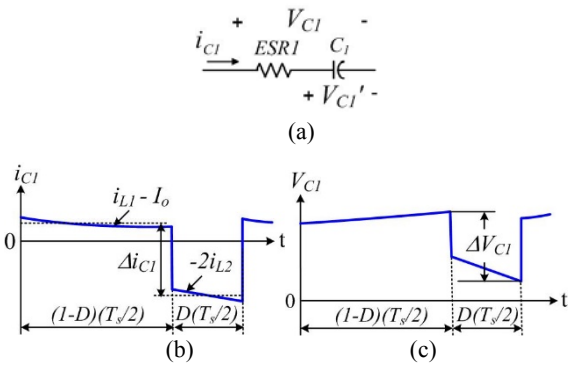


Fig. 6. Effects of capacitor voltage. (a) Equivalent circuit of capacitor C_1. (b) Capacitor current. (c) Capacitor voltage ripple.

voltages V_{c1} and V_{c2} can be obtained as a function of D through the following equations respectively.

$$V_{c1} = \frac{1-D}{1-4D+D^2} V_{in} \tag{21}$$

$$V_{c2} = \frac{2D}{1-D} V_{in} = \frac{2D}{1-4D+D^2} V_{in} \tag{22}$$

Similarly, applying the ampere-second balance principle to capacitor C_1 from (16) and (20), the average of the two inductor currents can be obtained as

$$\bar{i}_{L1} = \frac{(1-D)^2}{1-4D+D^2} I_o \tag{23}$$

$$\bar{i}_{L2} = \bar{i}_{L3} = \frac{1-D}{1-4D+D^2} I_o . \tag{24}$$

Considering that the peak dc-link voltage $\hat{v}_{pn}$ is identical to the capacitor voltage V_{c1}, the boost factor of the EAS-qZSI can be expressed as

$$B = \frac{\hat{v}_{pn}}{V_{in}} = \frac{V_{c1}}{V_{in}} = \frac{1-D}{1-4D+D^2} . \tag{25}$$

The peak phase voltage of inverter $\hat{v}_{ph}$ is expressed as

$$\hat{v}_{ph} = M \cdot \frac{\hat{v}_{pn}}{2} = M \cdot B \cdot \frac{V_{in}}{2} \tag{26}$$

where M is the modulation index.

From (26), the ac voltage gain G can be expressed as

$$G = \frac{\hat{v}_{ph}}{V_{in}/2} = M \cdot B . \tag{27}$$

3) Effects of the Capacitor Voltage Due to Current Ripples: The effects of capacitor voltage V_{c1} for capacitor current variations are analyzed. Fig. 6 shows an equivalent circuit of capacitor C_1 considering the equivalent series resistance (ESR), and the capacitor voltage ripple generated by the capacitor current variations during half of a switching period [17].

From (23) and (24), the capacitor voltage ripple can be expressed by (28). The capacitor voltage ripple is dependent on the shoot-through duty ratio, the switching period, the load current, the capacitance, and the ESR in the capacitor.

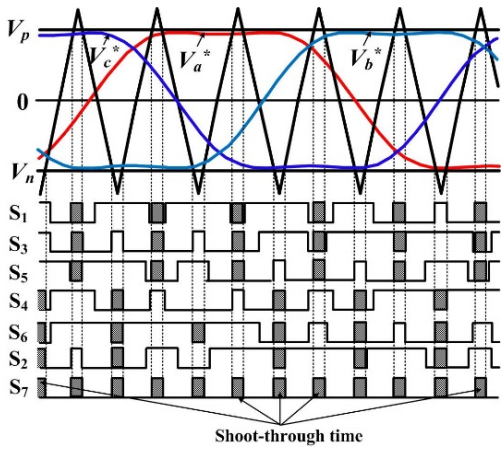


Fig. 7. Modulation under constant boost control method.

$$\Delta V_{c1} = ESR1 \cdot \Delta i_{c1} + \Delta V_{c1}^{'} = ESR1 \cdot \Delta i_{c1} + \frac{DT_s}{2C_1} \bar{i}_{c1} \tag{28}$$

where $\Delta i_{c1} = (\bar{i}_{L1} - I_o) + 2\bar{i}_{L2} = \frac{2}{1-4D+D^2} I_o$,

$$\bar{i}_{c1} = 2\bar{i}_{L2} = \frac{2(1-D)}{1-4D+D^2} I_o .$$

C. PWM Techniques

Some PWM control techniques for effectively adjusting the shoot-through state within a zero state are introduced to boost the dc-link voltage. The relationship between M and B (or D) from (27) is dependent on the PWM control techniques. Three PWM techniques based on a carrier-based PWM are proposed in [1], [15], and [16]. These PWM techniques are referred to as the simple, the maximum, and the constant boost control methods. Given that a simple control method has a constant shoot-through time during one switching period, the voltage stress across the switching devices is relatively high. In the maximum boost control method, all of the zero states are assigned as shoot-through states [15]. Although a maximum of voltage boost at a given modulation index can be achieved, the shoot-through duty ratio has a low-frequency ripple component.

To remove the ripple in the shoot-through duty ratio and obtain a higher boost capability, the constant boost control method introduced in [16] is used in the proposed topologies. Fig. 7 shows the pulse width modulation under the constant boost control method. The three-phase reference voltages V_a^*, V_b^*, and V_c^* are generated by injecting a third harmonic voltage with 1/6th of the fundamental voltage magnitude in the sinusoidal reference voltages. The shoot-through time is adjusted by comparing two shoot-through envelope signals V_p and V_n with the carrier signal. The switching device S_7 is in the conduction state during the shoot-through time, and the circuit for generating the gating signal of S_7 is shown in Fig. 8.

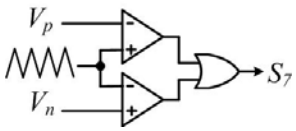


Fig. 8. Circuit for generating the gating signal of S_7.

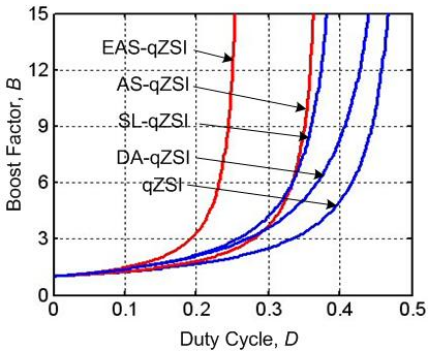


Fig. 9. Comparison of boost factors.

TABLE I
NUMBER OF COMPONENTS AT IMPEDANCE NETWORK

Topologies	Inductors	Capacitors	Switching devices	Diodes
AS-qZSI	2	2	1	2
EAS-qZSI	3	2	1	5
qZSI	2	2	0	1
SL-qZSI	3	2	0	4
DA-qZSI	3	3	0	3

The range of modulation index M can be extended from 1 to $2/\sqrt{3}$ by the constant boost control method. The relationship between the maximum modulation index M with the shoot-through duty ratio is expressed as:

$$M = \frac{2}{\sqrt{3}}(1-D). \tag{29}$$

IV. COMPARISON OF THE AS-QZSI AND EAS-QZSI WITH OTHER TOPOLOGIES

This section describes a comparison of the boost factor, the number of components used at the impedance network, and the voltage stress of the switches between the proposed topologies and other topologies.

A. Boost Factor

Fig. 9 shows the boost factors of the classic qZSI, SL-qZSI, DA-qZSI, AS-qZSI, and EAS-qZSI, in order to compare the voltage boost capability by using (1), (2), (3), (12), and (25). The boost factors of the proposed topologies are higher than that of the classic qZSI. The boost factor of AS-qZSI is lower or higher than those of both the SL-qZSI and DA-qZSI depending on the range of the shoot-through duty ratio. The proposed AS-qZSI topology has nearly the same boost capability as the SL-qZSI. Evidently, the EAS-qZSI has the highest boost factor among the five topologies.

B. Comparison of the Number of Components

Table I shows a comparison of the number of passive and active components used at the impedance network of the AS-qZSI, EAS-qZSI, classic qZSI, SL-qZSI, and DA-qZSI except for the inverter and LC filter. Compared with the SL-qZSI, the AS-qZSI needs one switching device more, but it can save one inductor and two diodes. Meanwhile, the EAS-qZSI requires an additional one diode and one switching device.

C. Voltage Stress Across the Switching Devices

The voltage stress across the switching devices of inverter V_s is identical to the peak dc-link voltage across the inverter bridge. In order to appropriately compare the voltage stress of the five topologies, the concept of equivalent dc voltage, which is defined as the minimum dc voltage necessary to generate an output voltage, is introduced [18]. The ratio between the voltage stress across the switching devices and the minimum dc voltage is expressed as V_s / ($G \cdot V_{in}$). Substituting (29) and the boost factors B of each topology into (27), the voltage stresses across the switching devices for the five topologies are given by

$$\frac{V_s}{GV_{in}} = \frac{\sqrt{3}G-1}{G} \text{ for classic qZSI} \tag{30}$$

$$\frac{V_s}{GV_{in}} = \frac{(4-2\sqrt{3}G)(4-\sqrt{24G^2-16\sqrt{3}G+16})}{G[(4-2\sqrt{3}G)^2-2(4-2\sqrt{3}G)(A_1)-(A_1)^2]} \text{ for SL-qZSI}$$

$$\frac{V_s}{GV_{in}} = \frac{(3\sqrt{3}G)^2}{G[(4\sqrt{3}G)^2-12\sqrt{3}G(A_2)+2(A_2)^2]} \text{ for DA-qZSI}$$

$$\frac{V_s}{GV_{in}} = \frac{(A_3-\sqrt{3}G)(2\sqrt{3}G-4)}{G[(2\sqrt{3}G-4)(8-7\sqrt{3}G+3A_3)+(3\sqrt{3}G-4-A_3)^2]}$$

for AS-qZSI

$$\frac{V_s}{GV_{in}} = \frac{(A_4-2\sqrt{3}G)(2\sqrt{3}G-4)}{G[(2\sqrt{3}G-4)(12-14\sqrt{3}G+4A_4)+(4\sqrt{3}G-4-A_4)^2]}$$

for EAS-qZSI

where $A_1 = 2\sqrt{3}G-\sqrt{24G^2-16\sqrt{3}G+16}$,

$A_2 = 3\sqrt{3}G-2-\sqrt{3G^2+4\sqrt{3}G+4}$, $A_3 = \sqrt{15G^2-8\sqrt{3}G}$

$A_4 = \sqrt{36G^2-16\sqrt{3}G}$.

Fig. 10 shows the voltage stress ratios of the five topologies with a variation of the ac voltage gain G. The classic qZSI has the highest voltage stress of the switches. The voltage stress of the proposed AS-qZSI is similar with that of the SL-qZSI at the overall range of the ac voltage gain, and the proposed EAS-qZSI has the lowest voltage stress ratio.

To verify the theoretical analysis of the proposed topologies, simulation studies are carried out with the PSIM

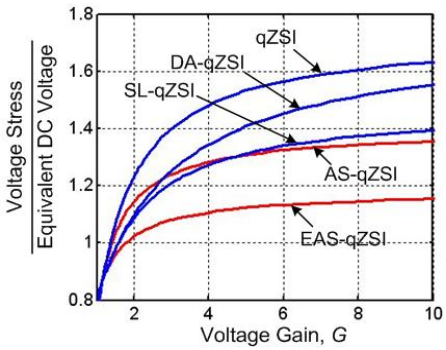


Fig. 10. Comparison of voltage stress ratios.

TABLE II
PARAMETERS USED AT SIMULATION AND EXPERIMENT

Parameters	Value
DC input voltage , V_{in}	40 V
Inverter frequency, f	60 Hz
Switching frequency, f_s	5 kHz
Capacitor (ESR), $C_1 = C_2$	1000 µF (65 mΩ)
Inductor, $L_1 = L_2 = L_3$	1 mH
Output LC filter, L_f	0.6 mH
Output LC filter, C_f	100 µF

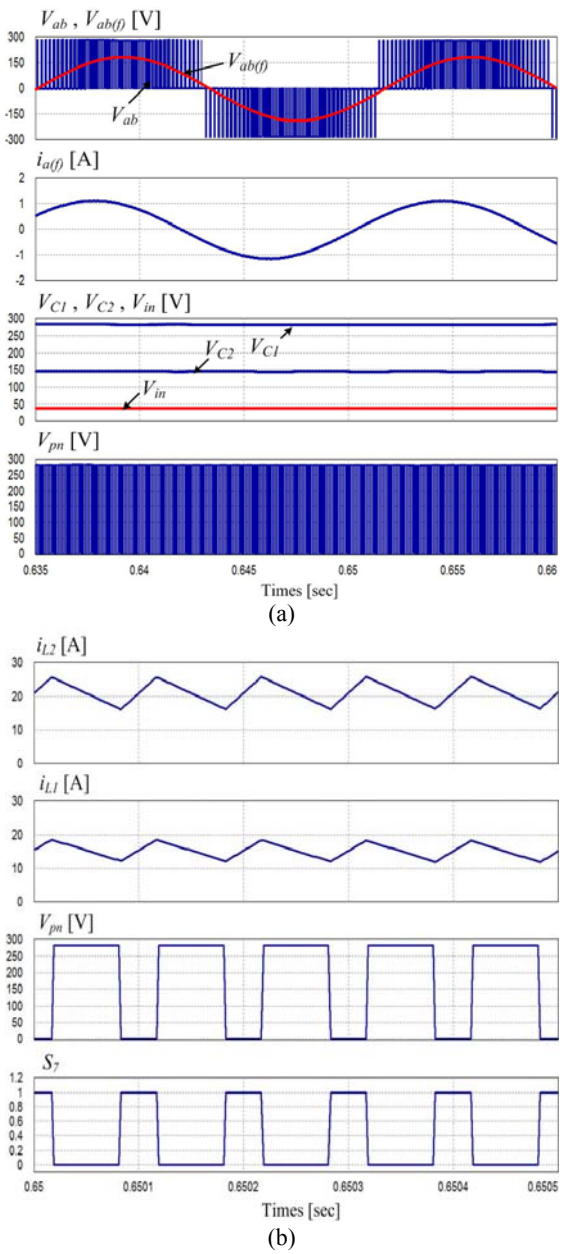


Fig. 11. Simulation result of AS-qZSI at $M = 0.76$ and $D = 0.34$: (a) ac voltage and current, capacitor voltages, and dc input and dc-link voltages, (b) two inductor currents, dc-link voltage, and S_7 signal.

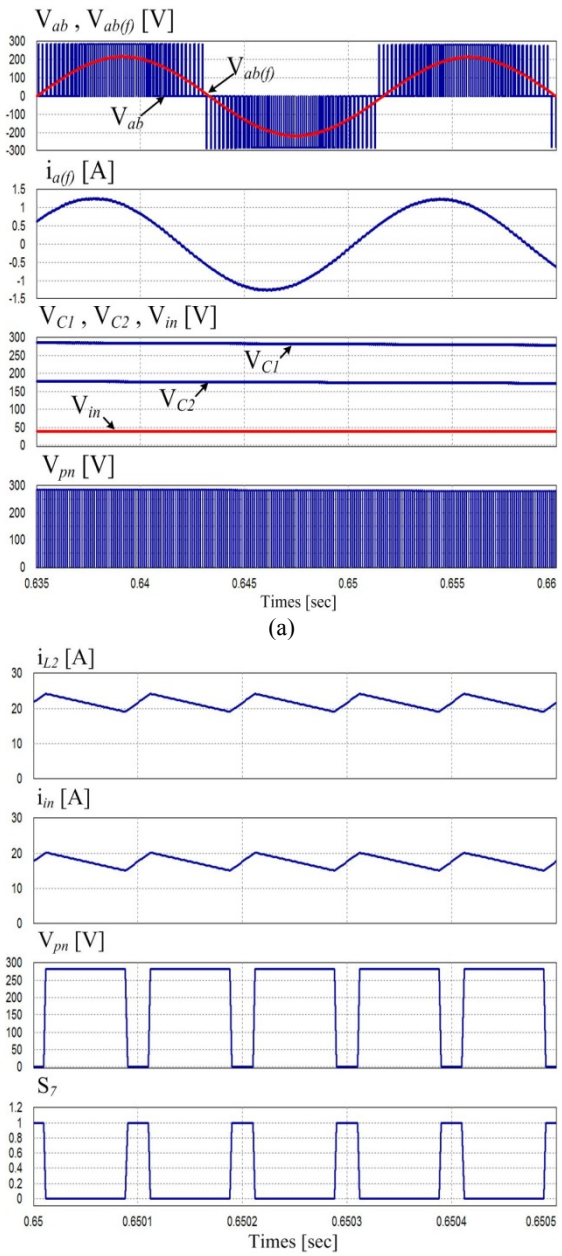
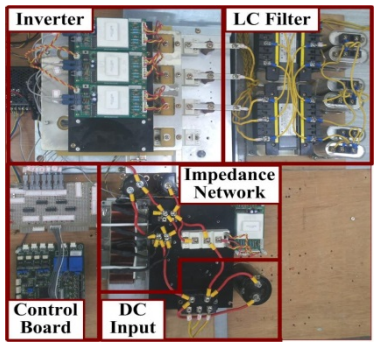
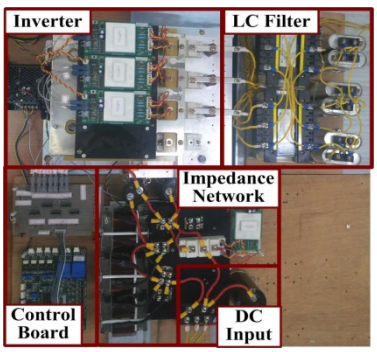


Fig. 12. Simulation result of EAS-qZSI at $M = 0.88$ and $D = 0.237$: (a) ac voltage and current, capacitor voltages, and dc input and dc-link voltages, (b) two inductor currents, dc-link voltage, and S_7 signal.

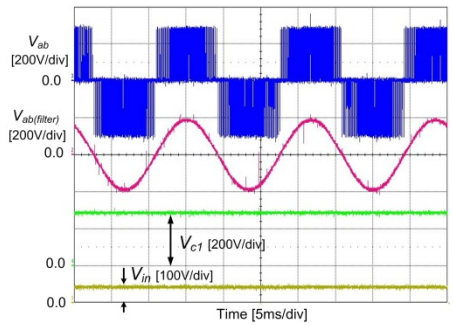


(a)

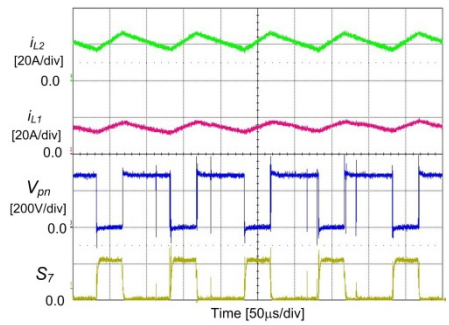


(b)

Fig. 13. Photographs of laboratory prototype. (a) AS-qZSI. (b) EAS-qZSI.



(a)



(b)

Fig. 14. Experimental results of AS-qZSI at M = 0.76 and D = 0.34. (a) Line-to-line voltages, capacitor and dc input voltages. (b) Inductor currents, dc-link voltage, and S_7 signal.

program. In the simulations, all of the components are assumed to be ideal, and a three-phase resistor of 100 Ω is connected at the output terminal as load. The parameters of the power converter used in the simulation and the experiment are shown in Table II.

Fig. 11 shows the simulation results of the AS-qZSI under the constant boost control at M = 0.76 and D = 0.34. From Fig. 11(a), the capacitor voltages V_{c1} and V_{c2} are boosted to 280 V and 170 V from 40 V, respectively, and a filtered line-to-line voltage of 130 V_{rms} can be obtained. Fig. 11(b) shows the waveforms of the two inductor currents, the dc-link voltage, and the gating signal of the switching device S_7. In the shoot-through state, the two inductor currents increase, and the dc-link voltage becomes zero. In the non-shoot-through state, the two inductor currents decrease and the dc-link voltage is 280 V, which is the same as capacitor voltage V_{c1}.

Fig. 12 shows the simulation results of the EAS-qZSI under the constant boost control at M = 0.88 and D = 0.237. From Fig. 12(a), the dc-link voltage is boosted to 280 V and the rms value of the line-to-line voltage is 150 V.

B. Experimental Results

Fig. 13 shows photographs of the prototypes of both the AS-qZSI and EAS-qZSI made at the laboratory for experimental verification. The prototypes are composed of a three-phase inverter, an impedance network, an LC filter for filtering the thee-phase output voltage and current, and a control board. The proposed topologies are controlled by a 32-bit high-performance DSP with a sampling period of 100 μsec. The switching frequency of the inverter is determined to be 5 kHz, and the shoot-through state is controlled twice during one switching period T_s, as shown in Fig. 7. The experiment is carried out with the same parameters and operating conditions used in the simulations.

V. Simulation and Experimental Results

A. Simulation Results

Fig. 14 shows the experimental results of the AS-qZSI when M = 0.76 and D = 0.34, which are the same operating conditions as the simulation results shown in Fig. 11. As shown in Fig. 14(a), the capacitor voltage is boosted to 275 V, which is 5 V less than the capacitor voltage in the simulation results shown in Fig. 11(a) due to the voltage drop on the diodes and the parasitic components in the inductors and capacitors. The rms value of the line-to-line voltage filtered by an LC filter is 126 V, which is also slightly lower than the simulation results. Fig. 14(b) shows the experimental waveforms of the two inductor currents, the dc-link voltage, and the gating signal of the switching device S_7.

Fig. 15 shows the experimental results for the EAS-qZSI when M = 0.88 and D = 0.237, which are the same operating conditions as simulation results shown in Fig. 12. As shown in Fig. 15(a), the capacitor voltage V_{c1} of the EAS-qZSI is nearly the same as that of the AS-qZSI. However, the

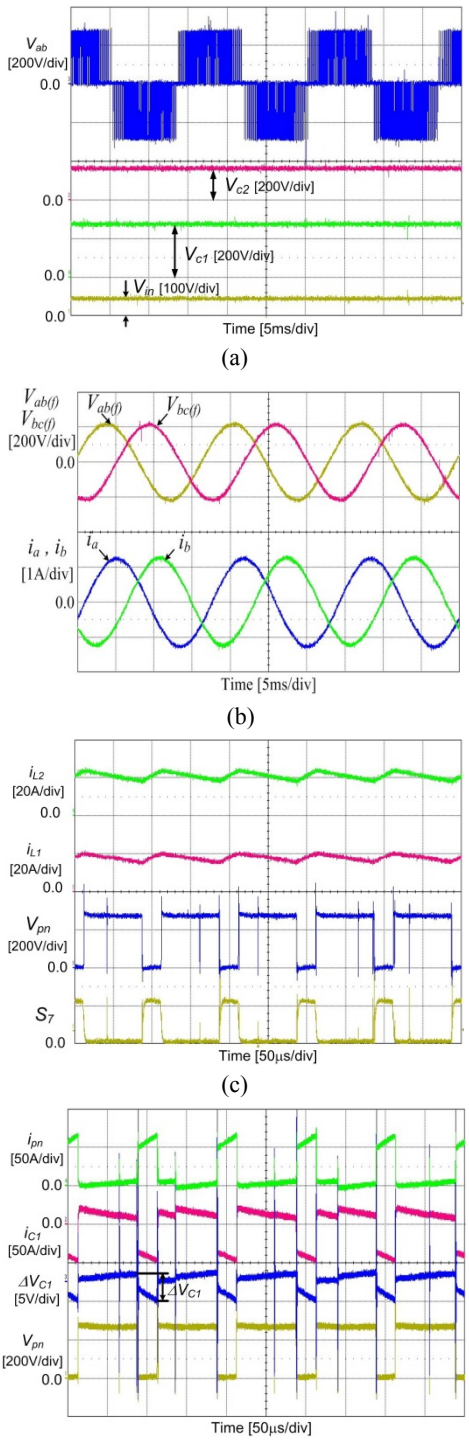


Fig. 15. Experimental results of EAS-qZSI at M = 0.88 and D = 0.237: (a) line-to-line voltage, capacitor voltages, and dc input voltage, (b) ac output voltages and currents filtered by LC filter, (c) inductor currents, dc-link voltage, and S_7 signal, (d) dc-link and capacitor currents, and capacitor voltage ripple.

shoot-through duty ratio decreases from 0.34 to 0.237. Fig. 15(b) shows the two-phase output voltages and currents filtered by the LC filter. An ac output voltage of about 148 V_{rms} can be generated, and the phase current lags the line-to-line voltage by 30° at the resistive load condition. Fig. 15(c) shows the experimental waveforms of the inductor and input currents, the dc-link voltage, and the gating signal of the switching device S_7. The inductor current ripples are lower than those of the AS-qZSI under the same peak dc-link voltage. It can be seen that the experimental results are nearly consistent with both the theoretical analysis and the simulation results. Fig. 15(d) shows a capacitor voltage ripple of 3.5 V generated by the capacitor current variation. The capacitor voltage rapidly changes at the transition from the non-shoot-through state to the shoot-through state due to the ESR in the capacitor, and the capacitor voltage ripple component is only 1.27 % of the capacitor voltage.

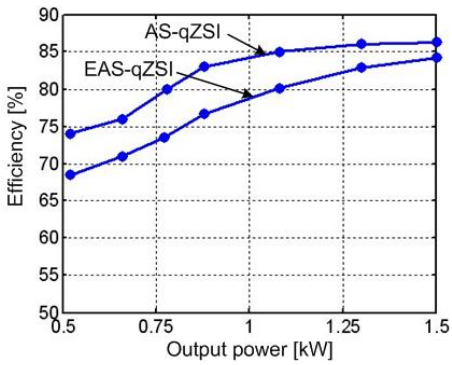


Fig. 16. Efficiency of EAS-qZSI and AS-qZSI.

Fig. 16 shows the efficiency of the proposed AS-qZSI and EAS-qZSI. The efficiency of the EAS-qZSI is lower than that of the AS-qZSI, because the EAS-qZSI has two more diodes.

VI. Conclusions

This paper proposed two types of novel topologies based on the qZSI. These topologies are the AS-qZSI and the EAS-qZSI. In comparison to the classic qZSI and the DA-qZSI, the proposed AS-qZSI provides a higher boost capability and a lower voltage stress across the switching devices of the inverter by adding only one switching device and one diode in the quasi-Z-source impedance network. The boost capability and the voltage stress of the AS-qZSI are similar to those of the SL-qZSI. However, the volume and cost of the power converter can be reduced by saving one inductor and two diodes in the impedance network, although one extra switching device is required. The proposed EAS-qZSI offers a much higher boost factor and a lower voltage stress across the switching devices.

Based on the experimental results, the dc-link voltage of the proposed topologies can be boosted seven times with respect to the dc input voltage. The AS-qZSI generates a line-to-line voltage of 126 V_{rms}, and the line-to-line voltage of EAS-qZSI can be increased by 15 % of the AS-qZSI under the same boost factor. The efficiency of the EAS-qZSI is lower than that of the AS-qZSI, because the EAS-qZSI has

two more diodes. The proposed topologies are applicable to renewable power generation with low-voltage energy sources such as photovoltaic arrays and fuel-cell stacks.

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