JPE 16-5-9

http://dx.doi.org/10.6113/JPE.2016.16.5.1706
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Modified Switched-Diode Topology for Cascaded Multilevel Inverters

Raghavendra Reddy Karasani[†], Vijay B. Borghate[*], Prafullachandra M. Meshram[**], and H. M. Suryawanshi[*]

[†,*]Dept. of Electrical Eng., Visvesvaraya National Institute of Technology (VNIT), Nagpur, India
[**]Dept. of Electrical Eng., Yeshwantrao Chavan College of Engineering (YCCE), Nagpur, India

Abstract

In this paper, a single phase modified switched-diode topology for both symmetrical and asymmetrical cascaded multilevel inverters is presented. It consists of a Modified Switched-Diode Unit (MSDU) and a Twin Source Two Switch Unit (TSTSU) to produce distinct positive voltage levels according to the operating modes. An additional H-bridge synthesizes a voltage waveform, where the voltage levels of either polarity have less Total Harmonic Distortion (THD). Higher-level inverters can be built by cascading MSDUs. A comparative analysis is done with other topologies. The proposed topology results in reductions in the number of power switches, losses, installation area, voltage stress and converter cost. The Nearest Level Control (NLC) technique is employed to generate the gating signals for the power switches. To verify the performance of the proposed structure, simulation results are carried out by a PSIM under both steady state and dynamic conditions. Experimental results are presented to validate the simulation results.

Key words: Multilevel inverter, Single phase inverters, Switched-diode topologies

I. INTRODUCTION

Employing multilevel inverters (MLIs) for medium to high voltage and high power applications has been gaining importance since the mid 1970s. The main features of MLIs are their abilities in reducing the dv/dt in the synthesized output phase voltage waveform and a reduction of the THD. In contrast, multi pulse converters utilize magnetic components to achieve desired voltage levels in the output voltage waveforms. The presence of magnetic components, their complexity of control, prone to failure, amount of loss and size make them inferior. The evolution of multilevel inverters started with the three classical structures namely the diode clamped multilevel inverter, also known as neutral point clamped (NPC), the capacitor-clamped multilevel inverter or flying capacitor (FC), and the cascade H-bridge (CHB). Further, many topologies have emerged and find their potential applications in distributed energy systems, flexible alternating current transmission (FACTS) and high voltage DC (HVDC) transmission [1], [2]. The classical CHB is remold into two power cells, each of which consist of a half bridge and a source for renewable energy applications [3].

The MLIs use power semiconductor switches in significant numbers to synthesize a smoother stair case output voltage waveform. The main issues to cope with in MLIs to generate multilevel voltages, are circuit complexity, control and efficiency. A reduction of the power electronic switches in MLI topologies has created a huge interests in academia and in the industry. Reduced switch count MLI topologies have been categorically presented and some of them are symmetrical and some of them are asymmetrical [4].

In brief, these emerging topologies are classified as Type-I, Type-II, Type-III and hybrid MLIs on the basis of their structures as shown in Fig.1. In Type III topologies, the basic unit is derived from a three leg 2-level inverter. This derived unit can generate 5-levels in output voltage using two equal DC sources, i.e. symmetrical mode [7]. The algorithms are proposed to define the magnitude of the DC sources i.e. asymmetric mode. The basic unit in the asymmetrical mode requires both unidirectional and bidirectional switches [8]. In the symmetrical mode, the generalization of higher level generation needs only unidirectional switches [9]-[11]. By incorporating two additional switches to the basic unit [7], the

Manuscript received Dec. 24, 2015; accepted May 9, 2016
Recommended for publication by Associate Editor Liqiang Yuan.
[†]Corresponding Author: raghu.vnitnagpur@gmail.com
Tel: +91-9960761474, Visvesvaraya Nat'l Inst. of Tech. (VNIT)
[*]Dept. of Electrical Eng., Visvesvaraya Nat'l Inst. of Tech. (VNIT), India
[**]Dept. of Electrical Eng., Yeshwantrao Chavan Coll. of Eng. (YCCE), India

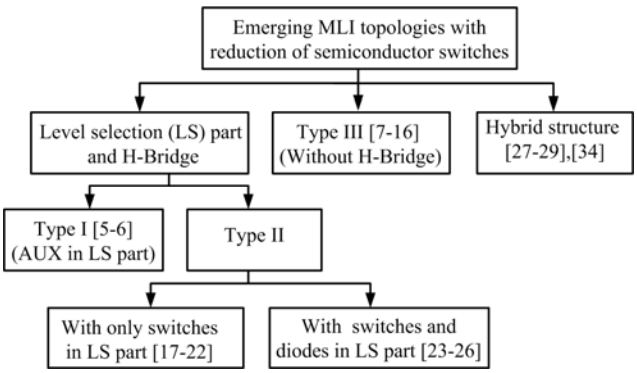

Fig. 1. Classification of emerging MLI topologies with reduced witch count.

maximum voltage levels can be achieved [12]. The basic unit needs bidirectional switches in the middle leg in the asymmetric mode. The basic unit uses a switch surrounded by four diode bidirectional configurations and these basic units are cascaded [13]. The basic unit is reconstructed in a cross connected manner so as to reduce the voltage stress [14]-[16].

In Type I and II topologies, the inverter has a level selection (LS) part to produce an even number of unidirectional voltage levels. They are also equipped with an H-Bridge for polarity reversal to synthesize an odd number of output voltage levels of either polarity. The Type I LS part consists of an Auxiliary (AUX) switch of a bidirectional nature, formed by a switch surrounded by four diodes [5], [6].

In Type II topologies, the inverter has only switches [17]-[22] or switches and diodes [23]-[25] in its level selection part. Bi-directional switches are used in a series connected sub-multilevel inverter to synthesize various voltage levels [17]. The gate drives requirement for each bidirectional switch are the same as a unidirectional switch at the cost of doubling the number of IGBTs / MOSFETs.

A Modified Topology is proposed to reduce the switch count, as a staircase type [18], by employing all of the unidirectional switches. The reduction in the switch count is further assessed with a modified level selection part by connecting DC sources in series/parallel [19]. A multi cell arrangement is presented to reduce the bidirectional count requirement in the level selection part [20]. The bidirectional switches are further reduced by replacing them with unidirectional switches for the top and bottom arms of the level section part [21]. A basic unit has been constructed and further cascaded to get more voltage levels in the output [22]. A tremendous decrement in the switch count is achieved in the switched-diode topologies [23]-[26], where only unidirectional switches are employed in the level selection part along with one diode in each cell. The hybrid structures are proposed for single phase [27] and three phase [28], [29], [34] operations.

A modified switched diode unit (MSDU) is constructed in this paper. This MSDU enables the advantages of a reduced switch count, a reduced diode count, improvement in efficiency and a simpler control. The proposed MLI is tested with the low switching frequency NLC control technique.

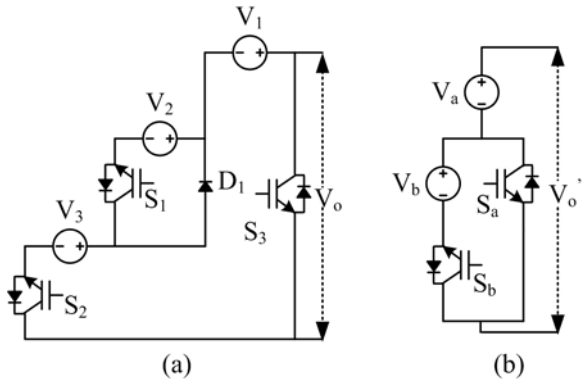

Fig. 2. Proposed multilevel inverter units. (a) Modified switch diode unit (MSDU) and (b) Twin switch twin source unit (TSTSU)

TABLE I
SWITCHING STATES OF MSDU

No.	Switching States			Vo
	S_1	S_2	S_3	
1	0	0	1	0
2	0	1	0	V_1+V_3
3	1	1	0	$V_1+V_2+V_3$

TABLE II
SWITCHING STATES OF TSTSU

No.	Switching States		Vo
	S_a	S_b	
1	1	0	V_a
2	0	1	V_a+V_b

II. PROPOSED MODEL

The proposed MLI is a Type III topology and it is made up of three essential parts described as follows:

A. Modified Switched Diode Unit (MSDU)

The MSDU is made up of three unidirectional IGBT switches S_1, S_2, S_3, one diode D_1 and three isolated DC sources V_1, V_2, V_3 as depicted in Fig. 2(a). The switching states of the power switches for the MSDU are shown in Table I, which shows that it can generate three different levels of 0, (V_1+ V_3) and (V_1+ V_2+ V_3) in the output voltage and that these three levels are of positive polarity. The occurrence of short circuits caused by the power switch pair (S_2, S_3) should be avoided by not turning ON, while S_1 is in OFF. In order to generate more voltage levels it is possible to cascade the MSDUs, enabling it for higher voltage applications. The output voltage of each unit MSDU is indicated by V_{o1}, V_{o2}…V_{oP}.

B. Twin Switch Two Source Unit (TSTSU)

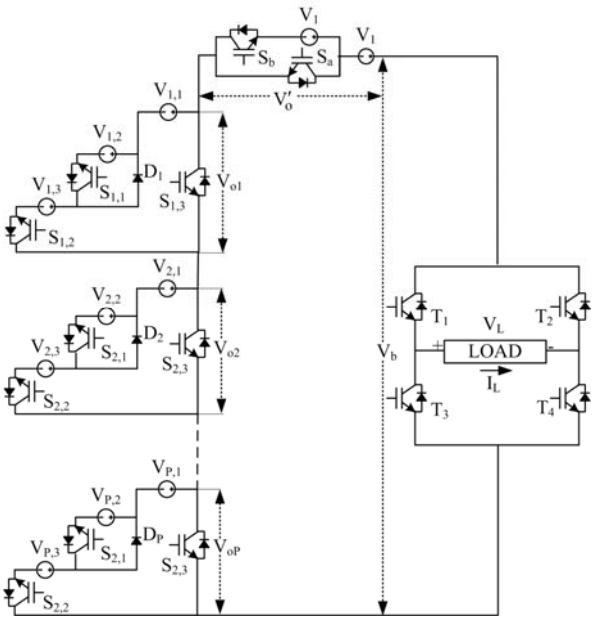

Fig. 3. Proposed cascaded multilevel inverter topology.

The TSTSU is made up of two isolated DC sources V_a, V_b and two unidirectional power IGBT switches S_a, S_b as depicted in Fig. 2(b). The switching states of the power switches for the TSTSU are shown in Table II, which can generate two different levels of V_a, V_a+V_b in the output voltage. These two levels are of positive polarity. Short circuits can be avoided by not turning on both of the switches S_a, S_b at the same instant. Doing so may lead to a circulating current in the TSTSU, which may damage the power switches. The TSTSU is connected in series with the MSDU so that all of the required voltage levels can be synthesized.

C. Polarity reversal part (Conventional H-bridge):-

A conventional H-bridge having four power IGBT switches (T_1-T_4) can produce three different levels, which includes the zero, positive and negative levels of the applied voltage at the bridge input. The voltage V_b across the terminals of the bridge input have only positive voltage levels which are given by:

$$V_b(t) = V_{o1}(t) + V_{o2}(t) + \cdots V_{op}(t) + V_o' \quad (1)$$

By adding a H-bridge in cascaded connection, as depicted in Fig. 3, the positive levels are enabled through the bridge, when the IGBTs (T_1, T_4) are ON. Then the load voltage V_L is equal to $+V_b$. When the IGBTs (T_2, T_3) are ON, the load voltage V_L is equal to $-V_b$. The zero voltage level is done by turning on either (T_1, T_2) or (T_3, T_4).

III. OPERATING MODES

The feature of the proposed MLI is its ability to operate in both symmetrical and asymmetrical modes. In this section the mathematical expressions of various parameters are derived, which are helpful in the comparative analysis to make it realizable.

A. Symmetrical Mode

In this mode, the magnitude of the DC voltage sources in each unit of the MSDU and the TSTSU are set equal.

$$V_{j,1} = V_{j,2} = V_{j,3} = V_{dc} \quad for \quad j = 1,2,\cdots,P \quad (2)$$

The number of levels 'L' produced in this mode can be related mathematically with the number of isolated DC sources 'S' used by the equation:

$$L = 2S + 1 \quad (3)$$

If 'P' number of MSDUs is connected in cascade, the number of sources used 'S' and the number of levels 'L' produced in this mode of operation by the proposed inverter, along with the number of IGBTs 'G' used and the number of additional power diodes 'D' used are given by the following equations, respectively:

$$S = 3P + 2 \quad (4)$$

$$L = 6P + 5 \quad (5)$$

$$G = 3P + 6 \quad (6)$$

$$D = P \quad (7)$$

All of the switches in the proposed topology are unidirectional power switches. Hence, the number of gate driver circuits 'GD' is equal to the number of IGBTs G, which is expressed as:

$$GD = G = 3P + 6 \quad (8)$$

The maximum output voltage produced $V_{L,\max}$ is given by:

$$V_{L,\max} = (3P + 2)V_{dc} \quad (9)$$

The voltage and current ratings of the switches in a multilevel converter play an important role in the cost and realization of the converter. In the proposed topology, the currents of all the switches are equal to the rated current of the load. However, this is not the case for the voltage. The Peak Inverse Voltages (PIV) from Fig. 2 is mathematically expressed as follows:

$$V_{Sa} = V_{Sb} = V_1 \quad (10)$$

$$V_{Sj,1} = V_{Dj} = V_{j,2} \quad (11)$$

$$V_{Sj,2} = V_{Sj,3} = V_{j,1} + V_{j,2} + V_{j,3} \quad (12)$$

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_1 + V_{L,\max} \quad (13)$$

The total PIV of the proposed inverter is the sum of all the PIVs in the MSDU, TSTSU and H-bridge, which is expressed as:

$$PIV = \sum_{j=1}^{P} \text{MSDU}_j + \text{TSTSU} + \text{H-Bridge} \quad (14)$$

$$PIV = \left[\left(2(3P) + 2P\right) + 2 + 4(3P + 2)\right]V_{dc} = (20P + 10)V_{dc} \quad (15)$$

Symmetrical multilevel inverters have attractive features in terms of modularity in construction, ease of control and the ready availability of equal DC sources.

B. Asymmetrical Mode

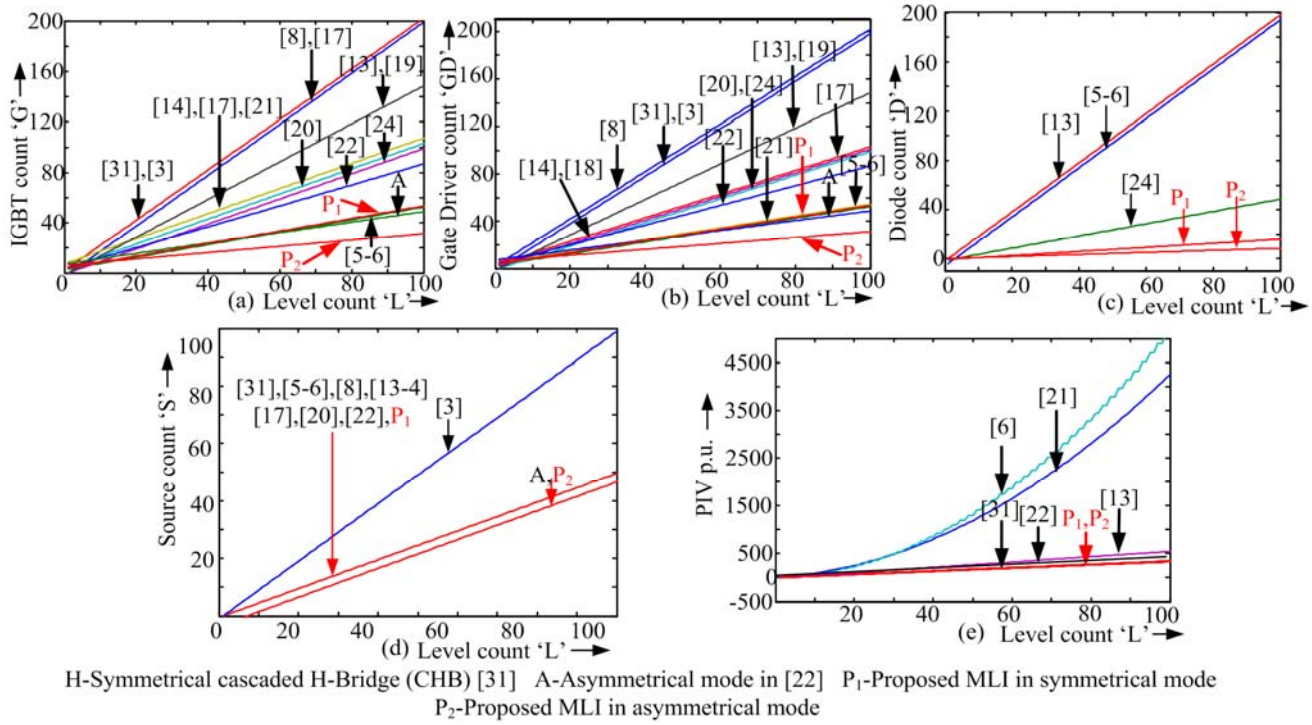

Fig. 4. Comparison of parameters with level count 'L'. (a) IGBT count 'G', (b) Gate Driver count 'GD'(c) Diode count 'D', (d) Source count 'S', and (e) PIV p.u..

Employing different dc voltages with proper ratios can improve the output voltage total harmonic distortion (THD), which improves the power quality. In this mode, the magnitude of the DC sources used in the TSTSU and the first MSDU are same, while in the other MSDUs are maintained at double the value of that in the first unit, for the generalized proposed structure illustrated in Fig 3.

$$V_1 = V_{1,1} = V_{1,2} = V_{1,3} = V_{dc} \tag{16}$$

$$V_{j,1} = V_{j,2} = V_{j,3} = 2V_{dc} \text{ for } j = 2,3,\cdots,P \tag{17}$$

$$L = 12P - 1 \tag{18}$$

$$V_{L,\max} = (6P-1)V_{dc} \tag{19}$$

Equations (6)-(8) are also valid for the asymmetrical mode, as per equation (14).

$$PIV = (40P\text{-}10)V_{dc} \tag{20}$$

The asymmetrical MLIs have an edge over the symmetrical structures in generating a larger number of voltage levels in the load output voltage. Hence, the quality of load voltage waveform is further improved.

IV. Comparative Analysis

Various topologies have been presented for MLIs. The asymmetrical topologies presented in [6] and [20] are the best in synthesizing more levels in inverter output voltage with the same number of DC sources used in the symmetrical modes. The realization of asymmetrical MLIs, which has to be provided from DC voltage sources with different values, can be very costly and difficult. As mentioned before, in the symmetric multilevel inverters, the values of all of the DC voltage sources are equal leading for easier realization possibility and lower design cost. However, the symmetric topologies can produce a lower number of voltage levels in comparison with the asymmetric topologies.

To have the same condition, the proposed topology in the symmetric mode P_1 is compared with the symmetric MLI topologies presented in [3], [5]-[6], [8], [13]-[14], [17]-[19], [22], [24] and with the symmetrical CHB [31]. The asymmetrical operation of the proposed multilevel inverter P_2 is also compared along with the asymmetrical operation of the topology in [22] represented as 'A' in Fig 4 (a)-(e). The comparison is done in view of optimizing the number of IGBTs, the number of diodes used, the number of driver circuits, the number of sources used and the PIV (p.u.) with an increasing number of levels in the output voltage is presented in Fig. 4 (a)-(e).

The Fig. 4(a) reveals the fact that the proposed inverter is the one with the minimum number of switches. Fig. 4(b) shows the gate drive count is minimum for proposed inverter in both the symmetric mode P_1 and the asymmetrical mode P_2. From Fig. 4(c) it can be concluded that the proposed inverter is the best choice when it comes to usage to achieve a minimum number of diodes. Fig. 4(d) shows that all of the symmetrical converters generate a number of levels that is double the number of sources, while the symmetrical mode requires

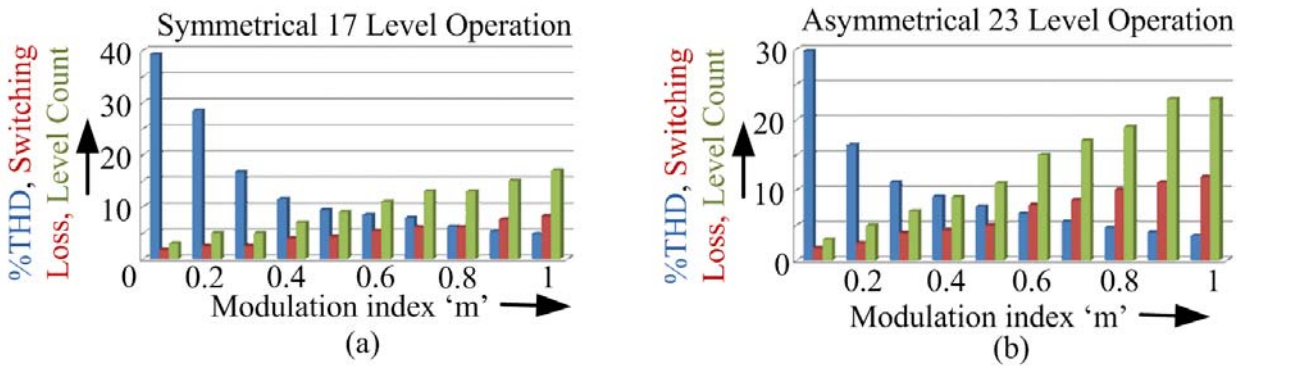

Fig. 5. Variation of %THD, Switching loss and Level count with change in modulation index 'm'.(a) symmetrical 17 level operation and (b) Asymmetrical 23 level operation.

TABLE III
COMPARISON OF RECENT TOPOLOGIES FOR OPTIMUM L/G RATIO ON SINGLE PHASE BASIS

Topology	Level count L	IGBT count G	L/G
Sym. in [22]	15	14	1.07
Asym. in [22]	21	14	1.5
[27]	5	8	0.625
Asym. in [28]	5	16/3	0.937
[29]	5	18/3	0.833
Sym. in [34]	9	24/3	1.125
Asym. in [34]	19	36/3	1.58
Sym. proposed P_1	17	12	1.416
Asym. proposed P_2	23	12	1.916

fewer sources for the same number of levels generation. Fig. 4(e) shows the PIV of the proposed inverter which is nearer to [31], [22]. However the topologies in [14]-[16] are the best since they are specially designed to reduce the PIV as a compromise against a larger number of IGBTs than the proposed topology. By changing the modulation index 'm' the level count 'L' is changed and as a result, the %THD and the switching loss are also changed. The variation of the %THD, switching loss and Level count 'L' with the modulation index 'm' are shown in Fig 5(a)-(b) for the symmetrical and asymmetrical modes, respectively. It is observed that for both the modes L and the switching loss increases, the % THD decreases with increases in m. The ratio of the level count to the IGBT count (L/G) should be optimum. A comparison is done with the recently proposed topologies [22], [27]-[29], [34] for the single phase under both the symmetrical and asymmetrical modes of operation as presented in Table 3. This shows that the proposed MLI has an optimum L/G ratio for both of the modes.

V. CONTROL SCHEME

The proposed MLI can operate at both the fundamental switching frequency and high switching frequency PWM. A

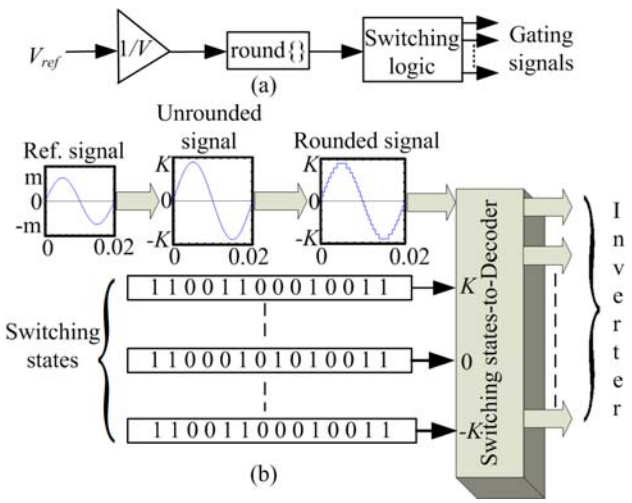

Fig. 6. Nearest level control technique. (a) block diagram and (b) Graphical representation.

wide variety of modulation and control methods have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM) [10-11],[30], selective harmonic elimination (SHE-PWM), space vector modulation (SVM) etc. The complexity of the SVM algorithm increases with the number of levels [30]-[32]. In the SHE, the offline computation of a large amount of switching angles and storing them is a tedious task for employing the proposed MLI.

The NLC technique [2], [34] facilitates the synthesizing of a very high number of voltage levels by approximating the amplified voltage reference ($K*V_{ref}$) to the closest generable voltage level of the converter, as depicted in Fig. 6(a)-(b). The corresponding mathematical equations are given by:

$$V_{ref} = mV_m \sin(\omega t) \tag{21}$$

$$K = \frac{V_m}{\left(\frac{L-1}{2}\right)V} \tag{22}$$

$$V_L = V\ round(V_{ref}/V) \tag{23}$$

VI. SIMULATION RESULTS

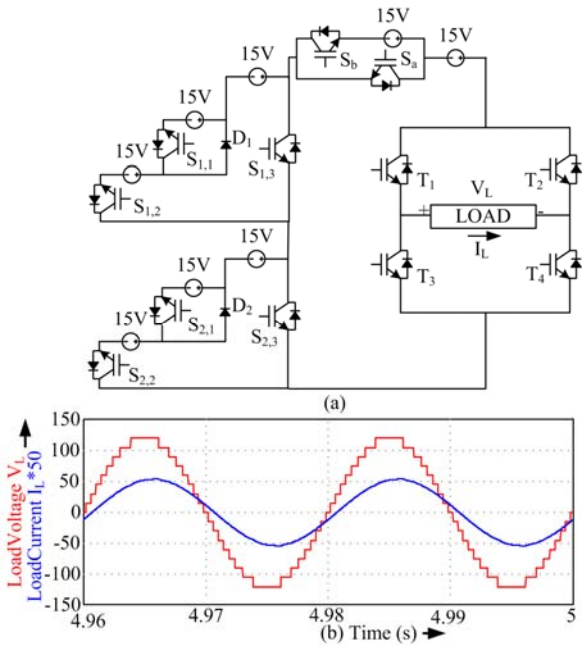

Fig. 7. Simulation results in symmetrical mode. (a) Symmetrical mode connection diagram and (b) Load voltage and current waveforms.

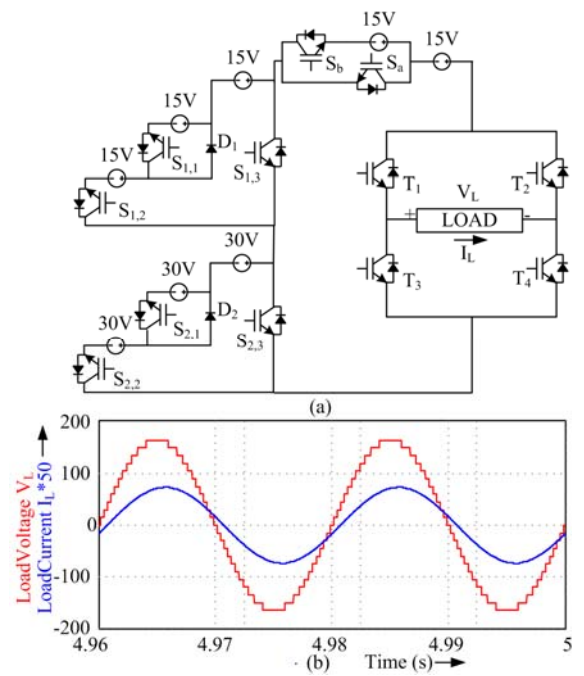

Fig. 8. Simulation results in asymmetrical mode. (a) Asymmetrical mode connection diagram and (b) Load voltage and current waveforms.

The proposed MLI is simulated using PSIM 9.3 for both the symmetrical and asymmetrical modes. As shown in Fig. 7(a) and Fig. 8(a), one TSTSU and two MSDUs are used. In the symmetrical mode, all of the DC source voltages are kept at 15V. Meanwhile, in the asymmetrical mode, DC sources of 15V are used in the TSTSU and in the first MSDU and 30V are used in the second MSDU.

TABLE IV
SWITCHING STATES FOR PROPOSED 17-LEVEL SYMMETRICAL MLI

No.	V_L	Conducting switches
1	120	$S_{1,1}$, $S_{1,2}$, $S_{2,1}$, $S_{2,2}$, $S_{2,3}$, S_b, T_1, T_4
2	105	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, $S_{2,1}$, $S_{2,2}$, $S_{2,3}$, S_a, T_1, T_4
3	90	$S_{1,2}$, $S_{2,2}$, S_b, T_1, T_4
4	75	$S_{1,2}$, $S_{2,2}$, S_a, T_1, T_4
5	60	$S_{1,1}$, $S_{1,2}$, $S_{2,3}$, S_a, T_1, T_4
6	45	$S_{1,2}$, $S_{2,3}$, S_a, T_1, T_4
7	30	$S_{1,3}$, $S_{2,3}$, S_b, T_1, T_4
8	15	$S_{1,3}$, $S_{2,3}$, S_a, T_1, T_4
9	0	T_1,T_2 or T_3,T_4
10	-15	$S_{1,3}$, $S_{2,3}$, S_a, T_2, T_3
11	-30	$S_{1,3}$, $S_{2,3}$, S_b, T_2, T_3
12	-45	$S_{1,2}$, $S_{2,3}$, S_a, T_2, T_3
13	-60	$S_{1,1}$, $S_{1,2}$, $S_{2,3}$, S_a, T_2, T_3
14	-75	$S_{1,2}$, $S_{2,2}$, S_a, T_2, T_3
15	-90	$S_{1,2}$, $S_{2,2}$, S_b, T_2, T_3
16	-105	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, $S_{2,1}$, $S_{2,2}$, $S_{2,3}$, S_a, T_2, T_3
17	-120	$S_{1,1}$, $S_{1,2}$, $S_{2,1}$, $S_{2,2}$, $S_{2,3}$, S_b, T_2, T_3

TABLE V
SWITCHING STATES FOR PROPOSED 23-LEVEL ASYMMETRICAL MLI

No.	V_L	Conducting switches
1	165	$S_{1,1}$, $S_{1,2}$, $S_{2,1}$, $S_{2,2}$, S_a, T_1, T_4
2	150	$S_{1,1}$, $S_{1,2}$, $S_{2,1}$, $S_{2,2}$, S_b, T_1, T_4
3	135	$S_{1,1}$, $S_{1,2}$, $S_{2,2}$, S_a, T_1, T_4
4	120	$S_{1,3}$, $S_{2,1}$, $S_{2,2}$, S_a, T_1, T_4
5	105	$S_{1,3}$, $S_{2,1}$, $S_{2,2}$, S_b, T_1, T_4
6	90	$S_{1,3}$, $S_{2,2}$, S_a, T_1, T_4
7	75	$S_{1,1}$, $S_{1,2}$, $S_{2,3}$, S_a, T_1, T_4
8	60	$S_{1,1}$, $S_{1,2}$, $S_{2,3}$, S_b, T_1, T_4
9	45	$S_{1,2}$, $S_{2,3}$, S_b, T_1, T_4
10	30	$S_{1,3}$, $S_{2,3}$, S_a, T_1, T_4
11	15	$S_{1,3}$, $S_{2,3}$, S_b, T_1, T_4
12	0	T_1,T_2 or T_3,T_4
13	-15	$S_{1,3}$, $S_{2,3}$, S_b, T_2, T_3
14	-30	$S_{1,3}$, $S_{2,3}$, S_a, T_2, T_3
15	-45	$S_{1,2}$, $S_{2,3}$, S_b, T_2, T_3
16	-60	$S_{1,1}$, $S_{1,2}$, $S_{2,3}$, S_b, T_2, T_3
17	-75	$S_{1,1}$, $S_{1,2}$, $S_{2,3}$, S_a, T_2, T_3
18	-90	$S_{1,3}$, $S_{2,2}$, S_a, T_2, T_3
19	-105	$S_{1,3}$, $S_{2,1}$, $S_{2,2}$, S_b, T_2, T_3
20	-120	$S_{1,3}$, $S_{2,1}$, $S_{2,2}$, S_a, T_2, T_3
21	-135	$S_{1,1}$, $S_{1,2}$, $S_{2,2}$, S_a, T_2, T_3
22	-150	$S_{1,1}$, $S_{1,2}$, $S_{2,1}$, $S_{2,2}$, S_b, T_2, T_3
23	-165	$S_{1,1}$, $S_{1,2}$, $S_{2,1}$, $S_{2,2}$, S_a, T_2, T_3

The conducting switches are listed in Table 4 and Table 5 for operation of both modes, respectively. The results are obtained with a resistive-inductive (R-L) load with R=110Ω, L=80mH at a modulation index of m=1.0. The load voltage

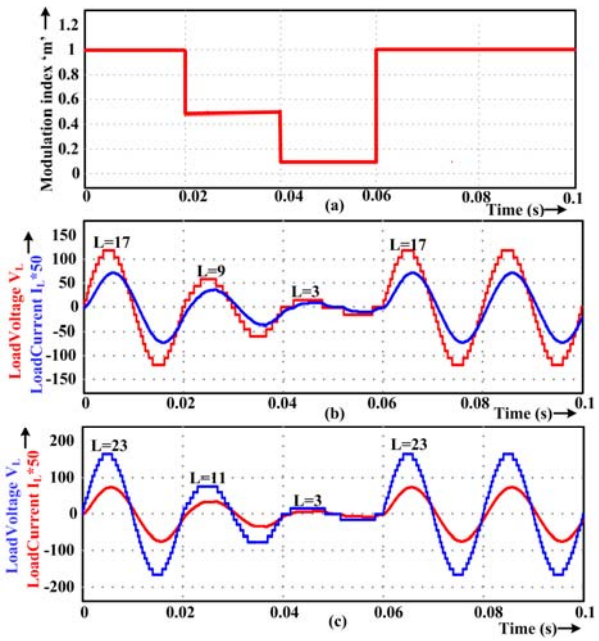

Fig. 9. .Dynamic response (a) Step changes in modulation index 'm', (b) Load voltage and current waveforms in symmetrical mode and (c) Load voltage and current waveforms in asymmetrical mode.

and current waveforms are given in Fig. 7(b) and Fig. 8(b) of both modes, respectively. It can be observed that the symmetrical mode gives 17 levels and that the asymmetrical mode gives 23 levels in its output voltage. The phase voltage

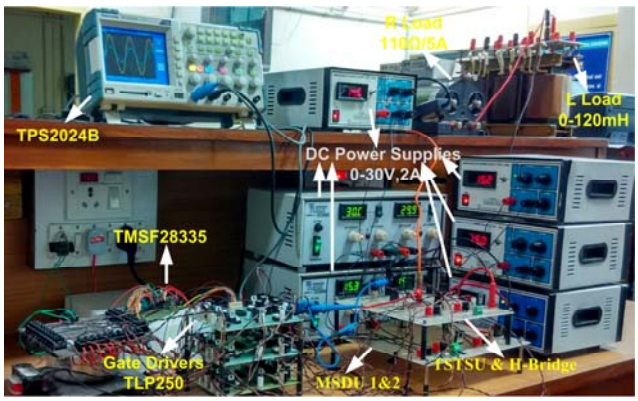

Fig. 10. Experimental set-up in the laboratory.

THD obtained in the symmetrical mode is 4.84% and in asymmetrical mode it is 3.55%.

To analyze the dynamic behavior of the proposed MLI, a step change in the modulation index 'm' is considered for both the symmetrical and asymmetrical modes of operation. A step change of m=0.5 having a duration of 1 cycle (i.e.20ms) is applied at=0.02 sec, and another step change of m=0.1 having a duration of 1 cycle is applied at t=0.04 sec as shown in Fig. 9(a). The level count 'L' gets reduced to 3 from 17 in the load voltage for respective step changes in the symmetrical mode as shown in Fig. 9(b). The variations of the load voltage and the current during step changes in the asymmetrical mode are shown in Fig. 9(c).

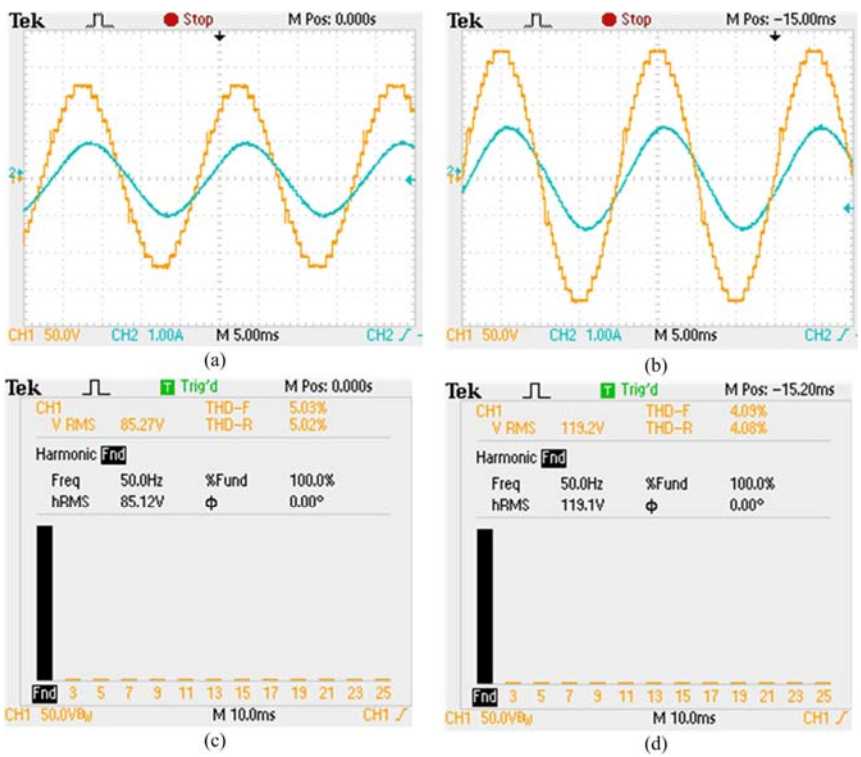

Fig 11. Load Voltage (50V/div) and current (1A/div) waveforms for modulation index m=1.0 (a) Symmetrical mode 17-level operation and (b) Asymmetrical mode 23-level operation. Harmonic spectrum of load voltage waveform. (c) Symmetrical mode 17-level operation and (d) Asymmetrical mode 23-level operation.

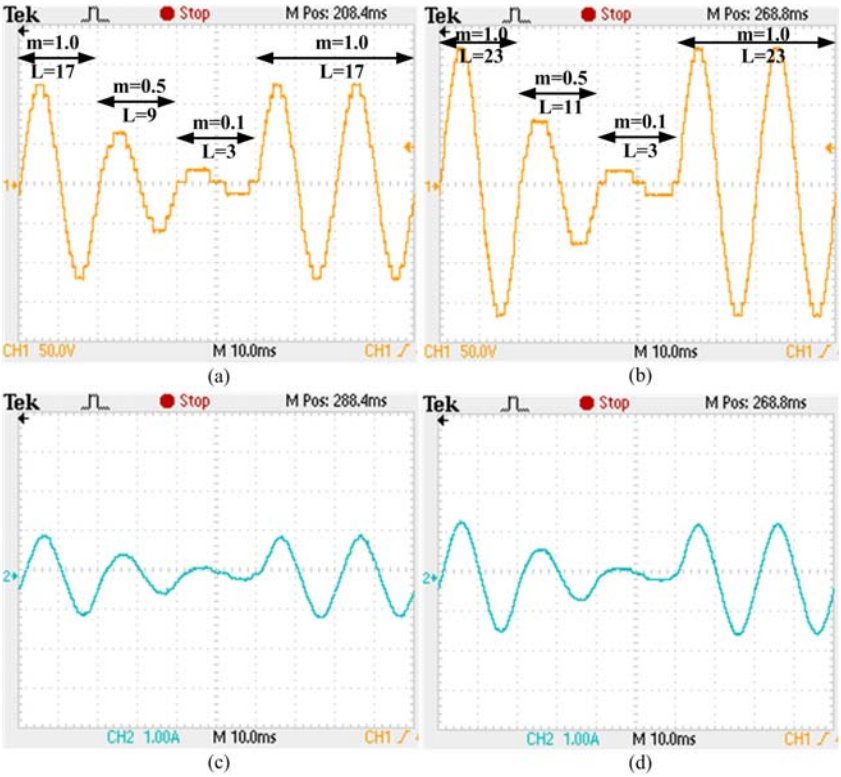

Fig 12. Response of proposed MLI to step changes in modulation index 'm'.(a),(c) Voltage (50V/div) and current (1A/div) waveforms for symmetrical mode 17-level operation and (b),(d) Voltage (50V/div) and current (1A/div) waveforms for asymmetrical mode 23-level operation.

VII. Experimental Results

To validate the simulation and theoretical results, a low power, single-phase, prototype is built as shown in Fig. 10. The NLC control algorithm is implemented digitally by using a DSP TMS32F28335 with code composer studio 5.3.0. The inverter is built with IRG4PH50UD IGBTs and RURP15120 ultrafast recovery Diodes as switching devices. The amplification and the isolation from the power circuit is provided by a driver TLP250. The prototype is tested with a resistive-inductive load of R=110Ω and L=72mH. A power scope of TEKTRONIX, Model No. TPS2024B, is used for recording the harmonic content.

In the symmetrical mode of operation, the proposed MLI is supplied by eight isolated DC voltage sources of 15V, to synthesize an inverter output voltage peak value of ±120 V through 17 levels in steps of 15V at 50Hz. The voltage and current waveforms are shown in Fig. 11(a). A harmonic analysis of the voltage waveform is depicted in Fig. 11(c). It shows that the %THD is 5.03%.

In the asymmetrical mode of operation, the TSTSU, and the first MDSU are supplied from isolated DC sources of 15V, and the second MDSU is supplied by isolated DC sources of 30V to achieve an inverter output voltage peak value of ±165V through 23 levels in steps of 15V at 50Hz. The voltage and current waveforms are shown in Fig. 11(b). A harmonic analysis of the voltage waveform is depicted in Fig. 11(d), it shows that the %THD is 4.09%.

The dynamic behavior of the proposed MLI is assessed by considering the step changes in the modulation index 'm'. The load voltage V_L of the inverter and the level count 'L' change according to the step change in the modulation index 'm' as described by (21). Variations in the load voltage V_L and load current I_L waveforms for step changes in the modulation index 'm' for 0.5 and 0.1 are presented in Fig. 12(a) and (c) for the symmetrical mode, and in Fig. 12(b) and (d) for the asymmetrical mode, respectively.

VIII. Conclusions

A modified switched-diode topology for a cascaded multilevel inverter has been proposed and a comparative analysis has been done in view of different aspects such as the number of switching components, number of gate drivers, number of sources, and PIV with respect to the level count for both the symmetrical and asymmetrical operating modes. Simulation results are presented and validated by conducting experiment on the proposed inverter in both operating modes under steady state and dynamic conditions. The obtained experimental results show the ability of the proposed inverter to generate all of the levels with a reduced number of switches.

REFERENCES

[1] J Rodrigues, J. S. Lai, and F. Z. Feng, "Multilevel inverters: a survey of topologies controls and applications," *IEEE Trans. Ind. Electron*., Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[2] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)," *IEEE Trans. Power Electron.*, Vol. 30, No. 1, pp. 450-462, Jan. 2015.

[3] G. Waltirch and I. Barbi, "Three-phase cascaded multilevel inverter using power cells with two inverter legs in series," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2605-2612, Aug. 2010.

[4] K. K. Gupta, A. Rajan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Trans. Power Electron*., Vol. 31, No. 1, pp. 135-151, Jan. 2016.

[5] G. Ceglia, V. Grau, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, A. Millan, and M. I. Gimenez, "A new multilevel inverter topology," in *Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems*, Vol. 1, pp. 212-218, Nov. 2004.

[6] C. I. Odeh and D. B. N. Nnadi, "Single-phase 9-level hybridised cascaded multilevel inverter," *IET Power Electron*., Vol. 6, No. 3, pp. 468–477, Mar. 2013.

[7] E. Babaei, M. T. Haque, and S. H. Hosseini, "A novel structure for multilevel converters," in *International Conference on Electrical Machines and Systems*, Vol. 2, pp. 1278-1283, Sep. 2005.

[8] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Electric Power Systems Research*, Vol. 77, No. 8, pp. 1073-1085, Jun. 2007.

[9] Y. Ounejjar, K. Al-Haddad, and L. A. Gregoire, "Packed U cells multilevel converter topology: theoretical study and experimental validation," *IEEE Trans. Ind. Electron,* Vol. 58, No. 4, pp. 1294-1306, Apr. 2011.

[10] K. K. Gupta and S. Jain., "Multilevel inverter topology based on series connected switched sources," *IET Power Electronics*, Vol. 6, No. 1, pp. 164-174, Jan. 2013.

[11] K. K. Gupta and S. Jain, "Comprehensive review of a recently proposed multilevel inverter," *IET Power Electronics*, Vol. 7, No. 3, pp. 467–479, Mar. 2014.

[12] K. K. Gupta and S. Jain, "A multilevel voltage source inverter (VSI) to maximize the number of levels in output waveform," *International Journal of Electrical Power & Energy Systems*, Vol. 44, No. 1, pp. 25-36, Jan. 2013.

[13] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Trans. Power Electron*, Vol. 29, No. 12, pp. 6712-6724, Dec.2014.

[14] M. F. Kangarlu, E. Babaei, and M. Sabahi, "Cascaded cross-switched multilevel inverter in symmetric and asymmetric conditions," *IET Power Electronics*, Vol. 6, No. 6, pp. 1041-1050, Jul. 2013.

[15] A. Ajami, M. R. J Oskuee, M. T. Khosroshahi, and A. Mokhberdoran, "Cascade-multi-cell multilevel converter with reduced number of switches," *IET Power Electronics,* Vol. 7, No. 3, pp. 552–558, Mar. 2014.

[16] A. Ajami, M. R. J Oskuee, A. Mokhberdoran, and A. V. den Bossche, "Developed cascaded multilevel inverter topology to minimise the number of circuit devices and voltage stresses of switches," *IET Power Electronics*, Vol. 7, No. 2, pp. 459-466, Feb. 2014.

[17] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Conversion and Management*, Vol. 50, No. 11, pp. 2761-2767, Nov. 2009.

[18] W. K. Choi and F. S. Kang, "H-bridge based multilevel inverter using PWM switching function," in *31st International Telecommunications Energy Conference (INTELEC)*, pp. 1–5, Oct. 2009.

[19] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2643-2650, Aug. 2010.

[20] J. Ebrahimi, E. Babaei, and G. B Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 2, pp. 655-667, Feb. 2012.

[21] M. F. Kangarlu, E. Babaei, and S. Laali, "Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources," *IET Power Electronics*, Vol. 5, No. 5, pp. 571-581, May 2012.

[22] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 2, pp. 922-929, Feb. 2015.

[23] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electronics*, Vol. 7, No.1, pp. 96-104, Jan. 2014.

[24] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Switched-diode structure for multilevel converter with reduced number of power electronic devices," *IET Power Electronics*, Vol. 7, No. 3, pp. 648-656, Mar. 2014.

[25] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Novel topologies for symmetric, asymmetric, and cascade switched-diode multilevel converter with minimum number of power electronic components," *IEEE Trans. Ind. Electron*., Vol. 61, No. 10, pp. 5300-5310, Oct. 2014.

[26] V. Singh, S. Pattnaik, S. Gupta, and B. Santosh, "A single phase cell based asymmetrical cascaded multilevel inverter," *Journal of Power Electronics*, Vo. 16, No. 2, pp. 532-541, Mar. 2016.

[27] A. Masaoud, H. W. Ping, S. Mekhilef, and H. O. Belkamel, "A new five-level single-phase inverter employing a space vector current control," *Electric Power Components and Systems*, Vol. 42, No. 11, pp. 1121-1130, May 2014.

[28] A. Masaoud, H. W. Ping, S. Mekhilef, and A. Taallah,

"Novel configuration for multilevel DC-link three-phase five-level inverter," *IET Power Electronics*, Vol. 7, No. 12, pp. 3052-3061, Dec. 2014.

[29] M. M. Masaoud, S. Mekhilef, and M. Ahmed, "Three-phase hybrid multilevel inverter with less power electronic components using space vector modulation," *IET Power Electronics*, Vol. 7, No. 5, pp. 1256-1265, May 2014.

[30] M. M. Renge and H. M. Suryawanshi, "Multilevel inverter to reduce common mode voltage in AC motor drives using SPWM technique," *Journal of Power Electronics,* Vol. 11, No. 1, pp. 21-27, Jan. 2011.

[31] I. Ahmed and V. B. Borghate, "Simplified space vector modulation technique for seven-level cascaded H-bridge inverter," *IET Power Electronics*, Vol. 7, No. 3, pp. 604-613, Mar. 2014.

[32] A. Matsa, I. Ahmed, and M. A. Chaudhari, "Optimized space vector pulse-width modulation technique for a five-level cascaded H-bridge inverter," *Journal of Power Electronics*, Vol. 14, No. 5, pp. 937-945, Sep. 2014.

[33] I. Ahmed, V. B. Borghate, A. Matsa, P. M. Meshram, H. M. Suryawanshi, M. A. Chaudhari, "Simplified space vector modulation techniques for multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 31, No. 12, pp. 8483-8499, Dec. 2016.

[34] R. Karasani, V. B. Borghate, P. M. Meshram, H. M. Suryawanshi, S. Sabyasachi, "A three phase hybrid cascaded modular multilevel inverter for renewable energy environment," *IEEE Trans. Power Electron.*, Vol. PP, No, 99, p. 1, Mar. 2016.

Raghavendra Reddy Karasani received his B.Tech degree in Electrical and Electronics Engineering from Sri Chundi Ranganayakulu Engineering College (SCREC), Guntur, India, in 2003; and his M.Tech in Power Control and Drives from the National Institute of Technology (NIT), Rourkela, India, in 2008. He worked as an Assistant Professor in the Department of Electrical and Electronics Engineering, Sir C R Reddy College of Engineering, Eluru, West Godavari, Andhra Pradesh, India. He is presently working towards his Ph.D. degree at Visvesvaraya National Institute of Technology (VNIT), Nagpur, India. His current research interests include power electronic converters, electrical drives, FACTS and renewable energy systems.

Vijay B. Borghate was born in 1960. He received his B.E. (Electrical), M.Tech. (Integrated Power System), and Ph.D. degrees from Visvesvaraya Natonal Institute of Technology (VNIT),Nagpur, India, in 1982, 1984, and 2007, respectively. He worked as an Engineer for the Maharashtra State Electricity Board, India, from 1985 to 1985. He became a Lecturer at VNIT (then VRCE), Nagpur, India, in 1985; where he is presently working as an Professor in the Department of Electrical Engineering. His current research includes resonant converters and multilevel converters.

Prafullachandra M. Meshram received his B.E., M.Tech. and Ph.D. degrees in Electrical Engineering from Visvesvaraya National Institute of Technology (VNIT), Nagpur, India, in 1991, 2003, and 2015, respectively. He is presently working as an Associate Professor in the Department of Electrical Engineering, Yeshwantrao Chavan College of Engineering (YCCE), Nagpur, India. He received best paper presentation awards for two of his papers at the IEEE Int. Conf. ECTICON 2005, Thailand. His current research interests include multilevel converters, especially Modular Multilevel Converters (MMC) and VSC-HVDC transmission systems.

H. M. Suryawanshi received his B.E. degree in Electrical Engineering from Walchand College of Engineering, Sangli, India, in 1988; his M.E. degree in Electrical Engineering from the Indian Institute of Science, Bangalore, India, in 1994; and his Ph.D. degree from Nagpur University, Nagpur, Nagpur, India, in 1999. He is presently working as a Professor in the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur, India. His current research interests are in the field of power electronics, emphasizing developmental work in the area of resonant converters, power factor correction, active power filters, FACTS devices, multilevel converters, high-frequency electronic ballasts, and electric drives. Prof. Suryawanshi is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. He is a Fellow of the Indian National Academy of Engineering (FNAE), IETE(I), and IE(I). He was the recipient of the Bimal Bose Award in 2009 from the IETE for his leadership in power electronics in India.