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A Novel Zero-Crossing Compensation Scheme for Fixed Off-Time Controlled High Power Factor AC-DC LED Drivers

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Abstract

A fixed off-time controlled high power factor ac-dc LED driver is proposed in this paper, which employs a novel zero-crossing-compensation (ZCC) circuit based on a fixed off-time controlled scheme. Due to the parasitic parameters of the system, the practical waveforms have a dead region. By detecting the zero-crossing boundary, the proposed ZCC circuit compensates the control signal V_{COMP} within the dead region, and is invalid above this region. With further optimization of the parameters K_R and K_τ of the ZCC circuit, the dead zone can be eliminated and lower THD is achieved. Finally, the chip is implemented in HHNEC 0.5μm 5V/40V HVCMOS process, and a prototype circuit, delivering 7~12W of power to several 3-W LED loads, is tested under AC input voltage ranging from 85V to 265V. The test results indicate that the average total harmonic distortion (THD) of the entire system is approximately 10%, with a minimum of 5.5%, and that the power factor is above 0.955, with a maximum of 0.999.

Key words: Fixed Off-Time, LED Driver, Power Factor Correction, Total Harmonic Distortion, Zero-Crossing Compensation

I. INTRODUCTION

Recently, light-emitting diodes (LEDs) have become popular solid-state lighting sources [1]-[3], as have AC/DC LED drivers. However, distortion of the input current resulting from nonlinear components in the AC power supply equipment, results in a lower power factor (PF). In addition, there is still some input current distortion due to the system's parasitic parameters and non-ideal characteristics, especially in the zero-crossing zone of the input voltage [4], [5]. The increasing demands on the conversion efficiency and power factor of power electronic equipment have resulted in the birth of harmonic standards such as Energy Star 2.0 [6], IEC 1000-3-2 and IEEE/ANSI 519.

Many academic studies have been conducted to reduce input current distortion to obtain much lower THD and a higher power factor. In [5], the phase delay technique is adopted to compensate for the phase lead, which reduces both the zero-crossing distortion and the THD. However, the dead angle of the input current, which results in higher THD, has not been completely eliminated. The input current zero-crossing distortion is reduced by detecting the dead zone boundary, and the system switched the topological structure due to the auxiliary switch in [7]. However, there is a lot of input current distortion during the auxiliary switch point. Moreover, the additional control circuit and discrete devices increase the power consumption and cost. The study in [8] adds a periodic self-starting timer block to force the power switch "ON", solving the dead angle problem of the input current and significantly reducing the distortion near the input voltage zero-crossing points. However, this additional compensation module cannot control the turn-on time of the power switch according to the input voltage in the dead region. As a result, it is limited in terms of obtaining much lower THD.

This paper proposes a novel zero-crossing compensation scheme applied to fixed off-time controlled high power factor AC-DC LED drivers. By detecting the zero-crossing boundary, the proposed ZCC circuit compensates the control signal, which modulates the power switch in the dead region. With further optimization of the parameters of the ZCC circuit, the dead zone is eliminated and lower THD is achieved.

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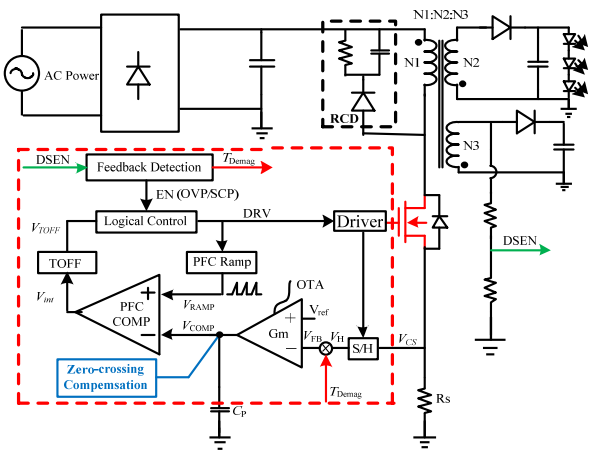


Fig. 1. Fixed off-time system structure.

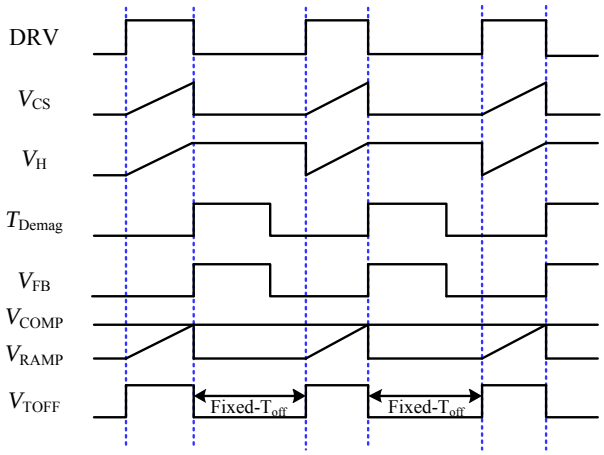


Fig. 2. The ideal work waveform.

In Section II, the fixed off-time controlled high PF AC-DC LED driver is described. The ZCC principle and the detailed parameter optimization procedure are described in Section III. Section IV demonstrates the effectiveness of the proposed method with the proposed zero-crossing compensation for improving the input current distortion through tests of the real circuit. Finally, section V presents some conclusions.

II. Fixed Off-time Controlled System

A. System Construction

The fixed off-time controlled system is based on the Flyback topology, which consists of a rectifier bridge, RCD circuit, transformer, NMOS power switch, and a series of diodes, resistors and capacitances, as is shown in Fig. 1. The resister R_S detects the primary-side current and achieves V_{CS}. The S/H (sample and hold) module samples V_{CS} and outputs the signal V_H. The feedback detection module processes the signal DSEN from the auxiliary winding and obtains the demagnetization time T_{Demag}, over voltage protection (OVP) and short circuit protection (SCP) signal. The module Gm amplifies the difference between V_{ref} and V_{FB}, which is equal to V_H multiplied by T_{Demag}. The zero-crossing compensation (ZCC) module is attached to the output of the OTA. The PFC COMP module compares the signals V_{COMP} and V_{RAMP} from the PFC ramp module, and exports the comparison result V_{int} to control the module TOFF. TOFF is a multi-vibrator which outputs V_{TOFF}. V_{TOFF} has a low level and maintains this state for a fixed period of time when V_{int} changes to a high level. Then it turns to a high level and waits for the next high level of V_{int}. The logical control module determines whether DRV follows V_{TOFF}. DRV is always kept low when the enable signal EN is at a high level, or it follows V_{TOFF} when EN is invalid at a low level. The PFC Ramp module generates a fixed slope ramp signal when DRV is high and keeps a low voltage when DRV is low. The driver module is a driving circuit, which aims at enhancing the driving capability of DRV to drive the power MOSFET. When DRV is high, V_H samples V_{CS} timely and holds the last sample value when DRV is at a low level.

B. Ideal Operation Principle

Ideally, the fixed off-time controlled system is operated as the work waveform shown in Fig. 2. V_H samples V_{CS} when DRV is high and holds the last sampling value when DRV is low. Then it is multiplied by T_{Demag} from the Feedback Detection module and obtains the signal V_{FB}. Therefore, V_{FB} can be expressed as:

$$V_{FB} = \frac{I_{ppk} \cdot R_s \cdot T_{Demag}}{T_s} = \frac{I_{spk} \cdot R_s \cdot T_{Demag}}{n \cdot T_s} \quad (1)$$

where, I_{ppk} is the peak current of the primary-side. R_S is the primary side sampling resistor. n is the turns ratio between the primary and secondary coil. T_{Demag} is the demagnetization time of the auxiliary winding, and T_S is the switch period.

Since there is a large capacitance attached to the port V_{COMP}, V_{COMP} is relatively constant. During the long period from t to $t+\Delta t$, equation (2) can be easily achieved.

$$\int_t^{t+\Delta t} (V_{ref} - V_{FB}) = 0 \quad (2)$$

where, V_{ref} is the reference voltage contacted to the positive input of OTA.

When DRV is high, the PFC Ramp produces a fixed slope ramp signal compared with V_{COMP}. When V_{RAMP} reaches V_{COMP}, V_{int} becomes high level and triggers the TOFF module. Meanwhile, the TOFF outputs a fixed time low voltage and then returns a high voltage while waiting for the next high level of the trigger signal V_{int}. Therefore, the modulation signal V_{TOFF} is achieved. Under normal working conditions, there is no OVP or SCP signal. Therefore, EN is always invalided and the DRV signal follows the signal V_{TOFF}.

The average output current can be described as:

$$I_{out} = \frac{1}{2} I_{spk} \cdot \frac{T_{Demag}}{T_s} = \frac{n \cdot I_{ppk} \cdot T_{Demag}}{2 \cdot T_s} = \frac{n \cdot V_{ref}}{2 \cdot R_S} \quad (3)$$

where, I_{out} is the average output current. I_{spk} is the peak current of the second-side. R_S is the sampling resistor contacted to the

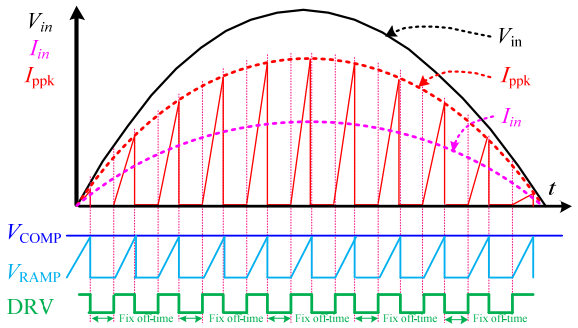


Fig. 3. Ideally work waveforms within one period.

power switch. Therefore, the average output current can be kept constant.

According to the above analysis, since V_{RAMP} increases at a fixed slope when DRV is high, the power switch conduction time can be expressed as:

$$T_{on} = k \cdot V_{COMP} \tag{4}$$

where, Ton is the conduction time of the power switch. k is the constant coefficient related to the fixed slope of VRAMP. Thus, the primary current can be shown as:

$$I_{ppk} = \frac{V_{in} \cdot |\sin(\omega t)|}{L_p} \cdot T_{on} = \frac{V_{in} \cdot k \cdot V_{COMP}}{L_p} \cdot |\sin(\omega t)| \tag{5}$$

where, V_{in} is the amplitude of the input line voltage. ω is angular frequency of the input voltage. L_p is the value of the primary inductance.

Therefore, the average input current meets the following condition:

$$I_{in} = \frac{I_{ppk} \cdot T_{on}}{2(T_{on} + T_{off})} = \frac{V_{in} \cdot k^2 \cdot V_{COMP}^2}{2L_p (k \cdot V_{COMP} + T_{off})} \cdot |\sin(\omega t)| \tag{6}$$

where, T_{off} is the switch off period, and I_{in} is the average input current.

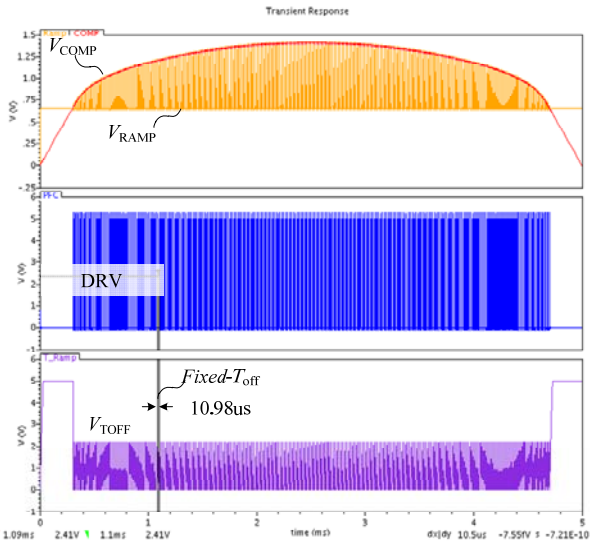
Ideal work waveforms within one period are shown in Fig. 3. V_{COMP} is kept constant and the average input current I_{in} follows the sinusoidal input voltage.

In this cycle, the normal power switch modulation signal is achieved, as well as a high power factor and a constant output current.

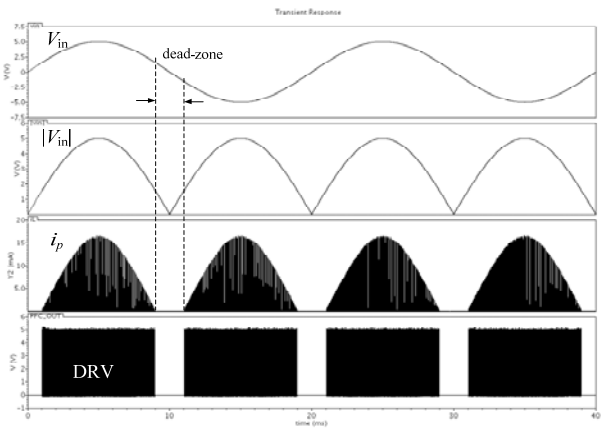
C. Practical Operation Phenomenon without the Proposed Zero-Crossing Compensation

However, due to the parasitic parameter and nonlinear characteristics of the system, there is a dead zone when the input voltage approaches the zero-crossing region [5], [9]-[10], and V_{COMP} is not constant during the entire input voltage range. Due to the variable of V_{COMP}, in the dead zone, the power switch is kept 'OFF' and the primary current is always zero. The IC driver cannot generate the normal modulation signal to drive the switch 'ON' or 'OFF'.

A practical waveform without the proposed zero-crossing compensation is presented in Fig. 4. DRV is the modulation signal of the power switch. T_{OFFR_AMP} is the signal to generate



(a) Operation waveforms about V_{COMP}, V_{RAMP}, DRV and V_{TOFF} within one period.



(b) Transient performances of primary current i_P and DRV in several input voltage V_{in} periods.

Fig. 4. The simulation results.

the fixed off-time signal, and i_p is value of the primary current. Undoubtedly, there is a dead zone where the input current cannot follow the sinusoidal input voltage in the entire range, which results in a heavy current distortion and decreases the power factor.

In order to decrease the input current distortion and to increase the power factor, this paper proposes a novel compensation circuit to remove this dead region.

III. Zero-Crossing Compensation Analysis

A. Zero-Crossing Compensation Principle

To solve the dead zone problem, a novel zero-crossing compensation module is introduced. As shown in Fig. 1, the proposed zero-crossing compensation is connected to the output of the OTA. The proposed ZCC circuit is shown in Fig. 5. By detecting V_{COMP} and comparing it with the preset voltage,

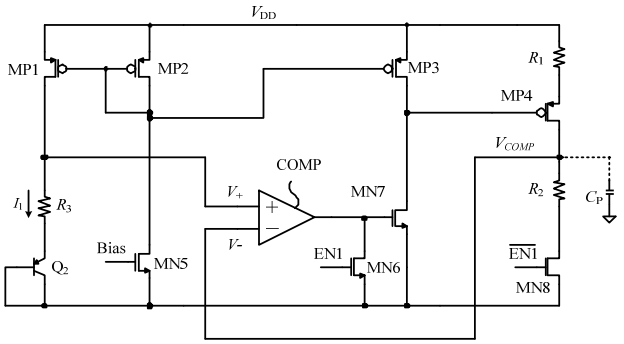


Fig. 5. The proposed zero-crossing compensation circuit.

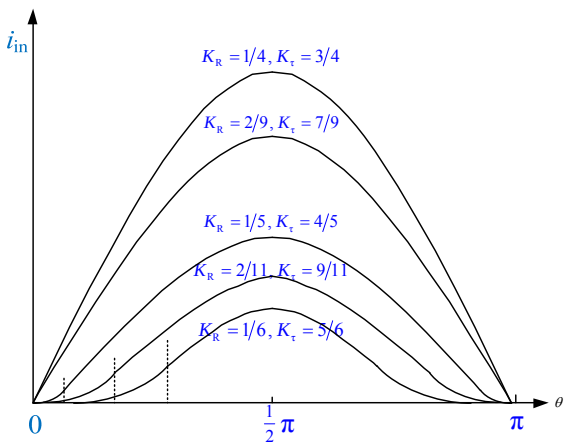


Fig. 6. Different input current waveforms with variable K_R and $K\tau$.

the ZCC circuit recognizes the boundary of the dead zone and compensates the value of V_{COMP}. Consequently, V_{COMP} can be kept relatively constant and the system can output a normal modulation signal to drive the power switch in the entire input voltage range.

According to Fig. 5, MP1 and MP2 make up a current mirror. MN5 is biased by a signal Bias. MN6 and MN8 are controlled by enabling signal EN1, which is invalid and maintains a low voltage under normal operation conditions. COMP is a comparator. The resistor R_3 and the PNP transistor Q_2 compose a voltage reference. The voltage reference V_+ is connected to the positive input of the comparator COMP. Thus, V_+ meets:

$$V_+ = I_1 \cdot R_3 + V_{EB} \tag{7}$$

where, V_{EB} is the voltage drop between the emitter and the base of the transistor Q_2. I_1 is the current through R_3 and Q_2.

The output voltage V_{COMP} is a feedback signal which connects to the negative input of COMP. When V_{COMP} is lower than V_+, V_{COMP} can be expressed as:

$$V_{COMP} = \frac{R_2}{R_1 + R_2} \cdot V_{DD} = K_R \cdot V_{DD} \tag{8}$$

where, $K_R = R_2/(R_1+R_2)$, and V_{DD} is the supply voltage of the ZCC circuit. Therefrore, the compensation module is affected by V_+ and K_R.

In the real circuit, the external compensation capacitor CP should to be taken into account as shown in Fig. 5. Therefore, the output voltage of the compensation module can be rewritten as:

$$V_{COMP} = \frac{R_2 / (sR_2C_P + 1)}{R_2 / (sR_2C_P + 1) + R_1} \cdot V_{DD} \tag{9}$$

Then, the time domain expression of the right branch circuit in Fig. 5 can be expressed as:

$$R_1 \cdot \left(C_P \cdot \frac{dv_C(t)}{dt} + \frac{v_C(t)}{R_2} \right) + v_C(t) = V_{DD}(t) \tag{10}$$

where, $v_C(t)$ is the instantaneous value of V_{COMP}. The ZCC circuit can only work when V_{COMP} is lower than V_+. Therefore, the output voltage $v_C(t)$ of the ZCC circuit can be expressed as:

$$v_C(t) = K_R \cdot V_{DD} \left(1 - e^{-\frac{K_\tau \cdot t}{C_P}} \right) + V_+ \cdot e^{-\frac{K_\tau \cdot t}{C_P}} \tag{11}$$

where, $K_\tau=(R_1\times R_2)/(R_1+R_2)$, $K_R=R_2/(R_1+R_2)$ and $V_+=I_1\times R_3+V_{EB}$. V_{COMP} keeps jumping between $v_C(t)$ and V_{COMP_0} (V_{COMP_0} is the output voltage of the OTA module in Fig.1, when the ZCC circuit is not taken into account.). Finally, the complete expression of V_{COMP} can be described as:

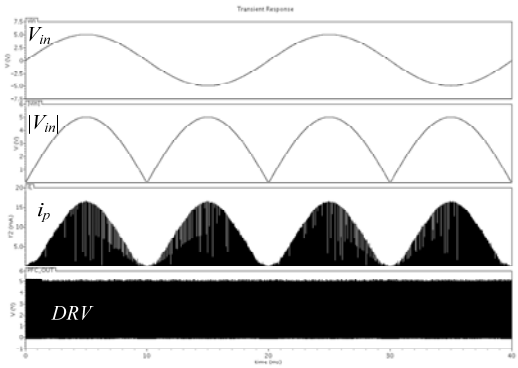
$$V_{COMP} = \begin{cases} \frac{1}{2} \cdot v_C(t) + \frac{1}{2} \cdot V_{COMP\_0}, & V_{COMP\_0} < V_+ \\ V_{COMP\_0}, & V_{COMP\_0} \geq V_+ \end{cases} \tag{12}$$

As a result, V_{COMP} can be kept relatively constant during the entire input voltage range. In addition, the dead zone can be eliminated by optimizing V_{COMP}.

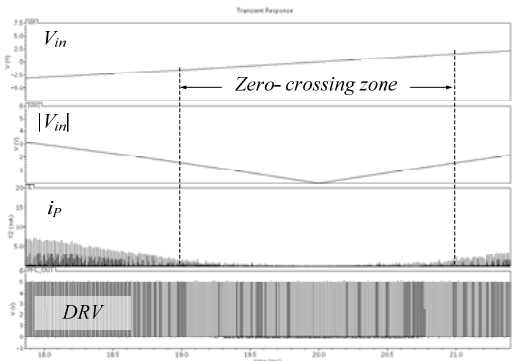
B. Zero-Crossing Compensation Circuit Optimization

From equation (12), V_{COMP} is related to the coefficients K_R and K_τ. From equation (6), V_{COMP} influences the average input current. With different values of K_R and K_τ, V_{COMP} can be variable after compensation, as well as the average input current i_{in} within the zero-crossing zone. Fig. 6 shows different average input current waves with various values of K_R and K_τ .

In order to simplify the coefficients K_R and K_τ, the value of R_2 was set as 1. As shown in Fig. 6, when K_R=1/6 and K_τ=5/6, in every half cycle, the input current can generally follow the input voltage's change. However, the input current wave has a distortion about half the time. Therefore, this set of data cannot solve the input current distortion problem near the zero-crossing zone. When K_R=2/11 and K_τ=9/11, in every half cycle, the input current is similar to a sinusoid wave. However, there is still distortion about two fifths of the time. When K_R=1/5 and K_τ=4/5, in every half cycle, the input current is more similar to a sinusoid wave and the distortion zone is decreased to about one tenth of the time. Therefore, in this set of data, the distortion can almost be ignored. With further increasing of K_R and decreasing of K_τ, when K_R=2/9 and K_τ=7/9, the input current wave is in accordance with a sinusoid wave and has almost no distortion. When K_R=1/4 and K_τ=3/4, the input current wave is also sinusoid and has almost no distortion. However, the average input current is much higher when compared with the last set of data.



(a) In several V_{in} periods.



(b) Near the zero-crossing of V_{in}.

Fig. 7. Transient simulation results of primary current i_P and DRV with proposed zero-crossing scheme.

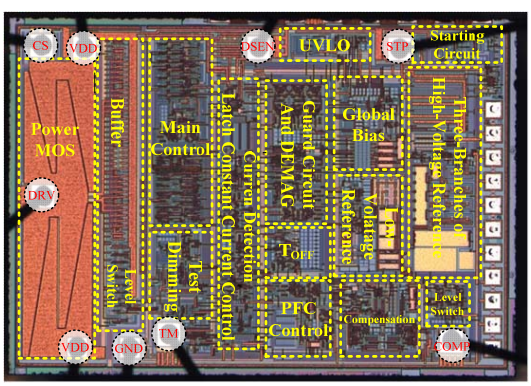


Fig. 8. Micrograph of the fabricated chip.

According to the above discussion, with the proposed ZCC module, the input current distortion during the dead zone can be effectively solved. By optimizing the two coefficients, the simulation results are presented as Fig. 7. With the proposed ZCC module, the input current is no longer zero in the dead zone and the average input current can follow variations of V_{in}.

IV. Experiment Results

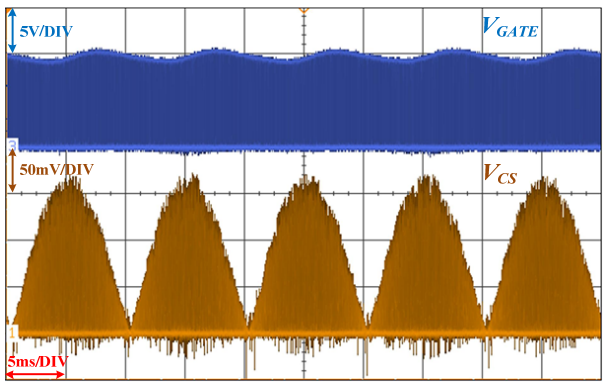
The IC is implemented in HHNEC 0.5μm 5V/40V HVCMOS process. A micro-graph of the fabricated chip is shown in Fig. 8, and the die size with PADs is 1950μm×2730μm.

Fig. 9. Photograph of the test circuit prototype.

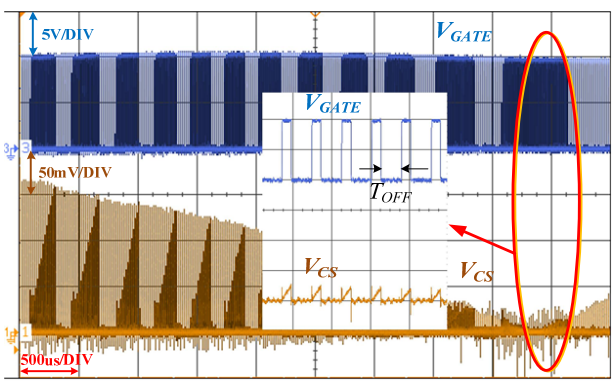
A test circuit prototype of the designed chip is shown in Fig. 9. The AC operating voltage of the PCB is 85V~265V and the output power is 7~12W.

A. Test waveforms

Fig. 10 shows the gate voltage V_{GATE} of the power switch MOSFET, and V_{CS} is the multiplication of i_p and R_S, in which i_P is the current flowing through the primary-side inductance, and R_S is the primary-side current sensing resistor. Obviously, the envelope of the primary peak current presents a sinusoidal

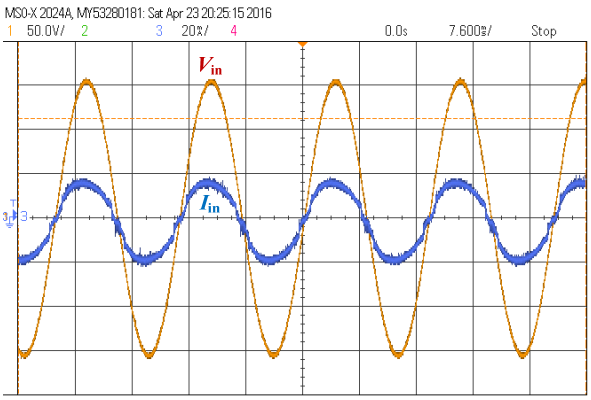


(a) Within Multi cycles.

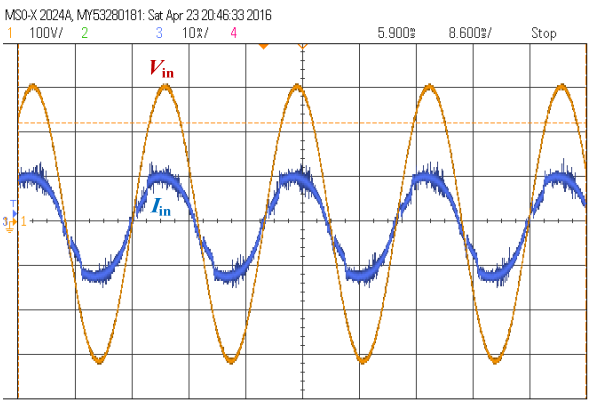


(b) In a quarter of one cycle, around zero-crossing point.

Fig. 10. The test waveform of the driving signal VGATE and the voltage drop VCS of primary sampling resistor RS.



(a) under AC sources of 110V/60Hz.



(b) under AC sources of 220V/50Hz.

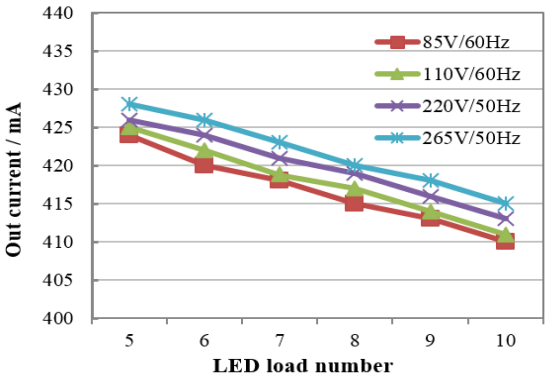
Fig. 11. The test waveforms of input AC voltage V_{in} and current I_{in}.

waveform and there is no dead zone around the zero-crossing point. The IC driver can output a normal modulation signal in the entire input range and fix the off-time in 10.7μs, even in the zero-crossing region. As a result, high power factor and lower THD are achieved in the fixed off-time controlled high power factor LED driver with the proposed zero-crossing compensation scheme.

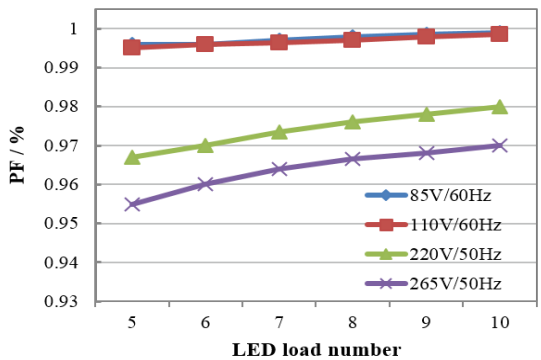
Fig. 11(a) shows test waveforms of the input AC voltage V_{in} and current I_{in} under AC sources of 110V/60Hz, while Fig. 11(b) shows test waveforms of the input AC voltage V_{in} and current I_{in} under AC sources of 220V/50Hz. Clearly, the test waveforms of the input AC current I_{in} present sinusoidal waveforms and there is no obvious dead zone around the zero-crossing point under both 110V/60Hz and 220V/50Hz in Fig. 11.

B. The System Performance with Different Inputs

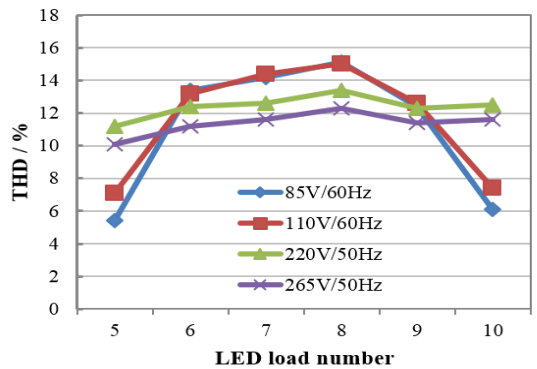
The load is composed of 5~10 cascaded 3W LEDs. Fig. 12 shows the output current, PF, THD and conversion efficiency under four different inputs and different numbers of LED loads. As shown in Fig. 12(a), the output current is slightly affected by different output powers. In Fig. 12(b), the average PF under 85V/60Hz AC and 110V/60Hz AC inputs are 2~3% larger than that under 220V/50Hz AC, and 3~4% larger when compare to the 265V/50Hz AC input condition. As shown in



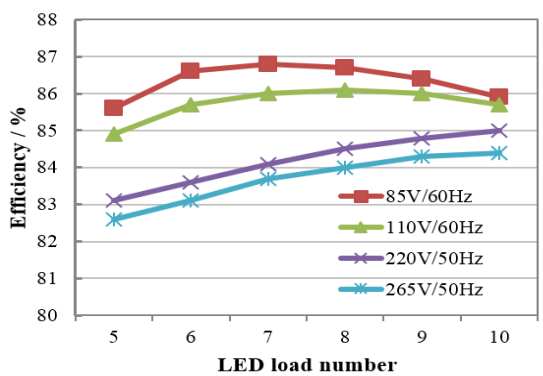
(a) The output current varieties under different loads.



(b) The PF varieties under different loads.



(c) The THD varieties under different loads.



(d) The conversion efficiency varieties under different load.

Fig. 12. The system performance with 85V/60Hz, 110V/60Hz, 220V/50Hz and 265V/50Hz inputs voltage.

TABLE I
PROPOSED CONVERTER COMPARED WITH SOME PUBLISHED APPROACHES

Index	This Paper	[11]	[12]	[13]
Technology	0.5μm CMOS	0.35μm BCD	0.35μm BCD	0.6μm CMOS
AC input voltage	85~265V	180~260V	85~265V	90~270V
Topology	Flyback	Flyback	Flyback	Flyback
Output Power	7-12W	5-11W	5-10W	9.5W
Output Current	420mA	340~400mA	340mA	370mA
Efficiency	0.82-0.86	0.82-0.83	0.82-0.85	Max:89.7%
Power Factor	0.955~0.999	0.935~0.98	0.94~0.98	>90%
Typical THD	10%	NA	15%	20%

Fig. 12(c), fluctuations in the THD are relatively mild under 220V/50Hz AC and 265V/50Hz AC with load changes, around the center value 10%. However, they are fairly obvious under 85V/60Hz and 110V/60Hz, from 5.5% to 15.1%. Finally, the conversion efficiency is above 82.5% under different input voltages and loads, as shown in Fig. 12(d).

Finally, Table I summarizes a comparison of the signal stage AC/DC converters presented in [11], [12] and [13] with the proposed converter in terms of circuit implementation and performance. The proposed converter achieves a relatively constant output current (=420mA) and a high efficiency (>82%). The efficiency obtained in this paper is equivalent to the typical efficiencies obtained in [11] and [12]. However, it is slightly lower than the LED Driver presented in [13]. Nevertheless, the key point of the proposed ZCC scheme in this paper is to improve the power factor (PF) and to decrease the THD rather than increase the efficiency. From Table I, it can be seen that the LED Driver with zero-crossing compensation can obtain a high PF above 0.95 and a maximum of 0.999 which is larger than the LED Drivers presented in [11], [12] and [13]. Meanwhile, the average THD is decreased to approximately 10% which is obviously lower than that in [12] and [13]. With the proposed ZCC scheme in a fixed off-time controlled high power factor AC/DC LED driver, the dead zone can be completely eliminated by further optimization of K_R and K_τ. Thus, the average input current can always follows the input voltage even in the zero-crossing zone.

V. CONCLUSION

This paper proposes a fixed off-time controlled high power LED driver with the proposed zero-crossing compensation. Based on the designed circuit, this paper verifies the feasibility of this compensation strategy, discusses the main parameters of the dead region, and optimizes the average input current waveform. The ZCC principle and the detail parameter optimization process are described. Finally, the chip is implemented using HHNEC 0.5μm 5V/40V HVCMOS, and the chip layout area is 1950μm×2730μm. Experimental results show that at 85-265V/AC input voltage and 7-12W output power, the system with the proposed zero-crossing compensation can obtain a high PF above 0.955, with a maximum of 0.999, and an average THD of 10%, with a minimum of 5.5%.

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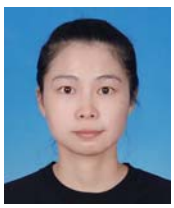

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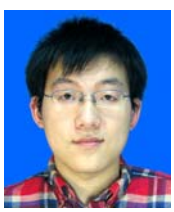

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