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A Novel Compensator for Eliminating DC Magnetizing Current Bias in Hybrid Modulated Dual Active Bridge Converters

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Abstract

This paper proposes a compensator to eliminate the DC bias of inductor current. This method utilizes an average-current sensing technique to detect the DC bias of inductor current. A small signal model of the DC bias compensation loop is derived. It is shown that the DC bias has a one-pole relationship with the duty cycle of the left side leading lag. By considering the pole produced by the dual active bridge (DAB) converter and the pole produced by the average-current sensing module, a one-pole-one-zero digital compensation method is given. By using this method, the DC bias is eliminated, and the stability of the compensation loop is ensured. The performance of the proposed compensator is verified with a 1.2-kW DAB converter prototype.

Key words: DC bias, Dual active bridge converter, Efficiency

I. INTRODUCTION

Residential electricity consumption has been increasing all over the world for the past several years. This increasing electricity consumption trend is attributed to the increasing number of home appliances and consumer electronics. Thus, small power household PV generation systems (300W~2000W) have been widely encouraged for use in the residential sector to power these devices as an auxiliary power supply.

A fundamental type of household PV system [1] is shown in Fig. 1. This PV system uses a bidirectional converter to store solar energy in the battery when the output power of the PV panel is higher than the power absorbed by the load. In addition, the bidirectional converter transfers this stored energy to the load when the output power of the PV panel is lower than the power absorbed by the load. In high-voltage-ratio applications, the dual active bridge (DAB) converter, shown in Fig. 2, has attracted the attention of many researchers [2], [3]. In the early stages of development, the single phase shift modulation (SPSM) was generally used due to its simplicity in implementation and good dynamic response characteristic [4]. However, SPSM fails to provide a good efficiency characteristic when the voltage transfer ratio increases, especially at light loads [5]. When the performance of microcontrollers was improved and many of them were commercialized with moderate pricing, some complex control methods like triangular modulation (TRM), modified triangular modulation (MTRM) [6], and trapezoidal modulation (TZM) were proposed to improve the light load efficiency of DAB converters when the voltage transfer ratio increases [7]. Nowadays, in applications which require a large voltage transfer ratio, hybrid modulation which employs both SPSM and TRM is always used.

However, the DC bias characteristics are seldom mentioned in these modulations. This is explained by the fact that the voltage-second products in these modulation methods are regarded as zero during a switching period [8]-[12]. Unfortunately, this assumption is not always satisfied in real applications because the voltage-second product is always unbalanced. Actually, this will happen in all of the power converters that employ high frequency transformers [13], [14]. At first, some DC bias compensation methods were proposed to suppress the DC bias in phase shift full bridge converters [15], [16]. The earliest control method to eliminate the DC

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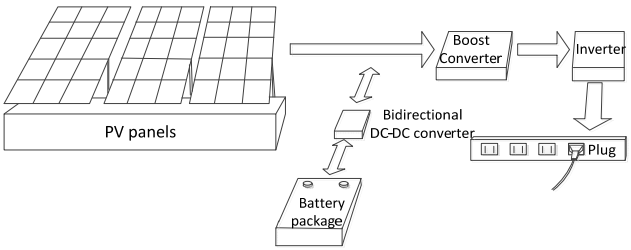


Fig. 1. Schematic of the household PV system.

bias of DAB converters was presented in [17]. However, only one operation condition is considered in this method, and a peak-current detector which is hard to realize in the DAB converters is needed. In [18], two different control loops (flux control and duty cycle based current mode control) were introduced, and a tertiary winding was added to inject a current equal to the DC bias. According to the description, if the output voltage needs to be controlled, there are three loops, which makes the stability of the DAB converter a serious problem. In the same year, a dual loop control method (including a loop to control the output voltage regulation) was introduced to suppress the DC bias [19]. The problem is that only the schematic of the dual loop control was given. A procedure for improving the stability of the introduced loop is not mentioned. In addition, these three methods can only be used in SPSM; they are are not the right choice for hybrid modulation schemes. The most recent article related to DC bias is [20]. However, this algorithm mainly focuses on the elimination of the transient DC bias to improve the transient response.

To overcome these problems, this paper proposes a novel DC bias compensation method to suppress the main DC bias in hybrid modulated DAB converters that employ TRM and SPSM. An average current sensing method is employed to detect the DC bias of the DAB converter. The procedure to achieve this average current sensing method is described in detail. Then a small signal model of the compensation loop is modeled. The design of the compensation loop is given. Finally, a prototype is built to demonstrate the validity of this method.

II. Problems Caused by the DC Bias and the Proposed DC Bias Compensator

A. Generation of the DC Bias

Fig. 2 shows a typical DAB converter without DC blocking capacitors. There are definitely two places that cause current DC bias; the primary side and the secondary side of the transformer. They are the power inductance L (including the leakage inductance of the transformer), and the secondary side magnetic inductance L_{m2}. Ideally, the primary side current has no DC bias, since the structure of the DAB converter is symmetrical. However, the DC bias of the

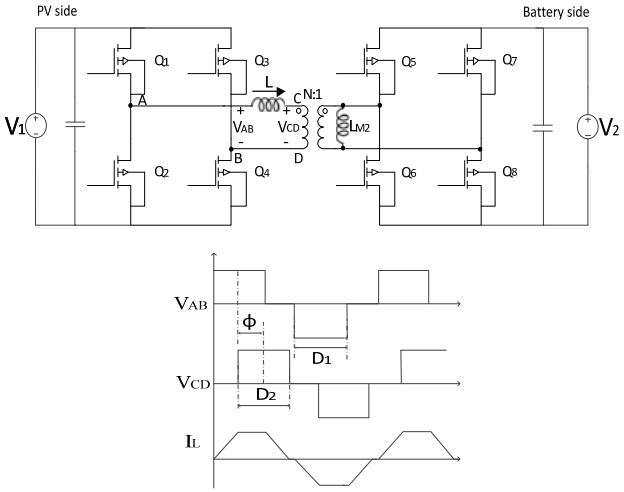


Fig. 2. Schematic of the DAB converter's power stage and its key waveforms.

magnetizing current appears in real applications. This is because that the voltage–second balances of the magnetic elements are not achieved. There are usually four reasons for these imbalances: 1) unbalanced pulse-width modulation (PWM) signals generated by the controller; 2) unbalanced parasitic parameters of the components, such as parasite resistance, parasite inductance and so on; 3) different switching ON/OFF characteristics; 4) nonlinearities of the magnetic cores.

Both L and L_{m2} can produce DC biases if the voltage-seconds on them are unbalanced. The DC biases of L and L_{m2} are affected by $V_{AB}(\mathrm{t})$ and $V_{CD}(\mathrm{t})/N$. A problem is that if both of the primary side and the secondary side DC biases are compensated by control loops, there must be two loops to compensate the DC bias. This means that there is a very complex stability design problem. In fact, the secondary side DC bias can be suppressed very well without using a compensator. The DC bias on an inductor, caused by the parasite resistance imbalance of the full bridge, can be analyzed by the model shown in Fig. 3(a). When Q_1 and Q_4 are open, the resistance of the current path is R_1. When Q_2 and Q_3 are open, the resistance of the current path is R_2. A mismatch of R_1 and R_2 causes the DC bias of the inductor current. It is assumed that the current waveform is symmetrical. The DC bias caused by this mismatch can be expressed as:

$$I_{bias} = \frac{x_1 - x_2}{2} \tag{1}$$

Where:

$$x_1 = V \frac{\frac{1-e^{-\frac{R_2 T_S}{2L}}}{R_2} - \frac{e^{-\frac{R_2 T_S}{2L}}\left(1-e^{-\frac{R_1 T_S}{2L}}\right)}{R_1}}{1-e^{-\frac{(R_1+R_2)T_S}{2L}}} \tag{2}$$

$$x_2 = V \frac{\frac{1-e^{-\frac{R_1 T_S}{2L}}}{R_1} - \frac{e^{-\frac{R_1 T_S}{2L}}\left(1-e^{-\frac{R_2 T_S}{2L}}\right)}{R_2}}{1-e^{-\frac{(R_1+R_2)T_S}{2L}}} \tag{3}$$

Where T_s is the switching frequency. If R_1 and R_2 are not the same, x_1 will not be the same as x_2. Then there is a DC

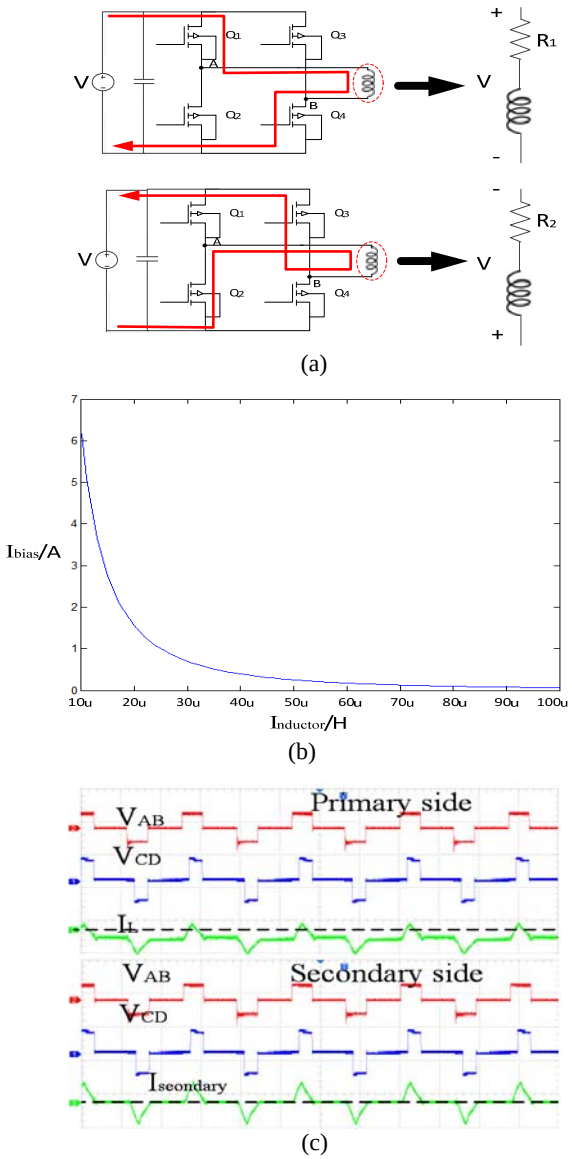


Fig. 3. (a) Model of the parasite resistance mismatch. (b) Relationship between the DC bias and the inductance in this model. (c) Measured waveforms of the primary side current and the secondary side current.

bias. Here $R_1 = 0.1$, $R_2 = 0.2$, $T_s = 27\mu s$, and $V = 60V$. The relationship between I_{bias} and L is illustrated in Fig. 3(b). It can be found that the DC bias of the inductor caused by a mismatch of the parasite resistances of the bridge legs is reversely proportional to the inductance.

This conclusion can be used in the DAB converter. The secondary side DC bias is caused by two factors. They are the inducted current of the primary side, and the DC bias of L_{m2}. However, the DC bias of L_{m2} from the primary side gets through L_{m2} at last. This is due to the fact that it causes a ripple on the battery side. This ripple increases the DC bias of L_{m2} until the DC bias of L_{m2} from the primary side is totally absorbed by L_{m2}. Therefore, the secondary side DC bias is entirely caused by the voltage-second imbalance of the

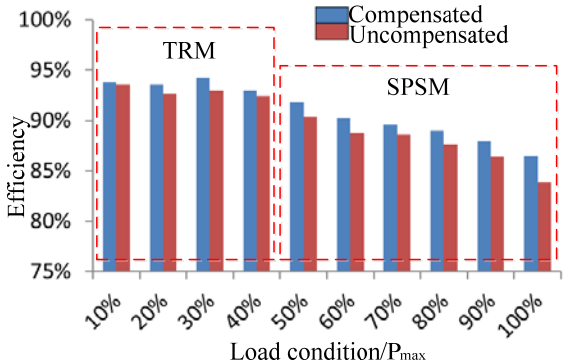


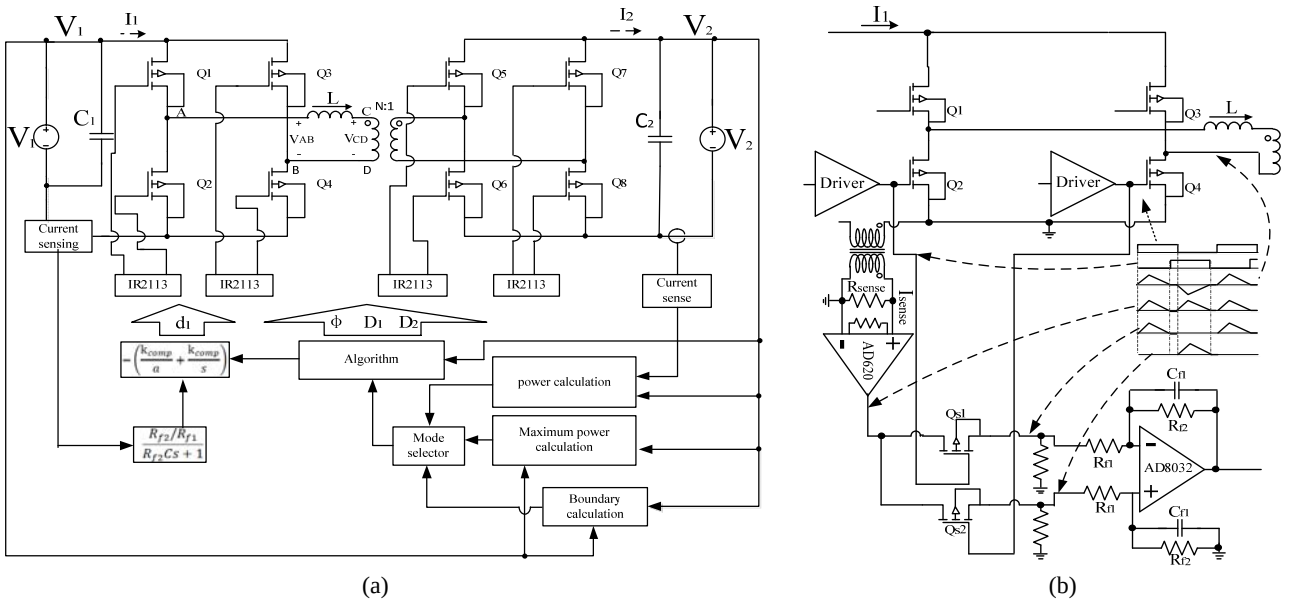
Fig. 4. Comparison between the measured efficiencies of the compensated and the uncompensated DAB converter.

secondary side bridge on L_{m2}. The model shown in Fig. 3 shows that the larger the inductance is, the smaller the parasite resistance imbalances' effect becomes. The value of L_{m2} in the prototype is 0.9 mH. It is big enough to suppress the DC bias caused by the mismatch of the parasite resistances. However, the primary side DC bias is affected by the parasite resistance mismatch largely because the value of L is about 14μH, and the voltage added to the power inductor is large during the operation of the DAB converter. One of the test results of the DC biases on the primary side and the secondary side is shown in Fig. 3 (c). In this figure, the DC bias on the primary side is much larger when both of them are not compensated.

B. Problem Caused by the DC Bias

A conventional controller stabilizes the output voltage V_o of the DAB converter by controlling the phase shift between V_{AB} and V_{CD}, the inner duty cycle D_1 of V_{AB}, and the inner duty cycle D_2 of V_{CD} [6]. Since the controller has no information on the DC bias, it cannot rebalance the voltage–second product of the magnetic elements. Therefore, the conventional controller cannot remove the DC bias of the primary side current.

When DC bias is generated, the primary current increases in either the positive direction or the negative direction. The first problem is that it increases both the conduction loss and the current stress. Another problem is the saturation of the magnetic core. The third problem is its effect on the ZVS characteristics of the MOSFETs. Finally, it also causes audio-frequency noise. In the design of the DAB converter, the ZVS is an important problem that needs to be considered. If DC bias exists, the current in one of the upper-left-side MOSFETs increases at the switching-on transient. This phenomenon increases the switching loss. To verify the bad effect of the DC bias, an experiment is conducted on a 1.2kW (the maximum power when the input voltage and the output voltage are 106V and 60V) prototype. The input voltage is 40V and the output voltage is 60V (under this condition, the maximum power is about 450W). The output voltage is



(a) (b)

Fig. 5. (a) Schematic of the DAB converter with the proposed DC bias compensation. (b) Schematic of the proposed average current sensing module.

controlled by a voltage-mode controller, which is achieved in a TMS320f28335 digital signal processor. Fig. 4 shows the efficiencies of the converter both with and without the DC bias. It can be seen that the DC bias decreases the overall efficiency of the DAB converter. For the aforementioned reasons, there is no doubt that the DC bias must be eliminated to keep the reliability and efficiency of DAB converters.

C. Proposed Compensator

The DAB converter with the proposed compensator is shown in Fig. 5. The current sensing module detects the current of I_1. Then the detected current is chopped into two parts. The first part is defined as I_{1-Q_4}, and the second part is defined as I_{1-Q_2} (these two parts are synchronous with the driver signals of Q_4 and Q_2). The difference between I_{1-Q_4} and I_{1-Q_2} is averaged by a low pass filter which consists of R_{f1}, R_{f2} and C_{f1}. The averaged values of I_{1-Q_4} and I_{1-Q_2} are set as $I_{1-Q_4,av}$ and $I_{1-Q_2,av}$. The basic control logic is that if $I_{1-Q_4,av} > I_{1-Q_2,av}$, which means that the DC bias is positive, the duty cycle of Q_1 is decreased with $\hat{d}_1$ to suppress this DC bias. The magnitude of the primary current is balanced after several switching periods. There are two control loops which eliminate the DC bias and stabilize the output voltage. The loop of the compensator consists of two parts. They are a average current sensing module and a PI module (achieved in a TMS320f28335). The average current sensing module consists of a current sensing module, two MOSFETs, and a low pass subtracter. The two MOSFETs are driven by the gate drive signals of Q_4 and Q_2. The main loop of the DAB converter consists of 5 modules to achieve a hybrid modulation which employs TRM and SPSM. The specifications of this loop are not discussed here.

The average current method detects the average value of $I_{1-Q_4,av}(t) - I_{1-Q_2,av}(t)$. This average value has a relationship with the DC bias, and is expressed as:

$$I_{bias}(t) \approx \left(I_{1-Q_4,av}(t) - I_{1-Q_2,av}(t)\right)k \tag{4}$$

Where k is a constant corresponding to the modulation method. In this paper, SPSM and TRM are used, and the calculation of k is dependent on the modulations. The parameter k is the small signal gain from the average currents' difference to the real average current value. In SPSM, the behavior of the small signal gain can be modeled as shown in Fig. 6(a). This behavior is based on the assumption that the inductor current is symmetrical. If there is a small signal perturbation $\hat{I}_{L,av}$ on $I_{L,av}$ there will be an increment of $\hat{I}_{L,av}$ on I_{1-Q4}. Because the duty cycle of the drive signal on Q_4 is 50%, it can be seen that the gain from $\hat{I}_{L,av}$ to $\hat{I}_{1-Q_4,av}$ is 0.5. It can also be seen that the gain from $\hat{I}_{L,av}$ to $\hat{I}_{1-Q_2,av}$ is -0.5. That is to say $k = 1$. In TRM, when $M < 1$ ($M = V_{CD}/V_{AB} = NV_2/V_1$), the behavior of the small signal gain can be modeled in Fig. 6(b). In the stage when $V_{AB}(t)$ is zero, the inductor current does not flow out of the left-side bridge. It flows around Q_2 and Q_4. Therefore, it can be seen that the gain from $\hat{I}_{L,av}$ to $\hat{I}_{1-Q_4,av}$ is $0.5D_1$, and the gain from $\hat{I}_{L,av}$ to $\hat{I}_{1-Q_2,av}$ is $-0.5D_1$. That is to say $k = D_1$. As shown in Fig. 6(c), it can be derived that $k = D_1$ when $M > 1$. In fact, SPSM can be regarded as a case of $D_1 = D_2$=1. Therefore, it can be seen that:

$$k = D_1 \tag{5}$$

III. Models of the DC Bias in the DAB Converter

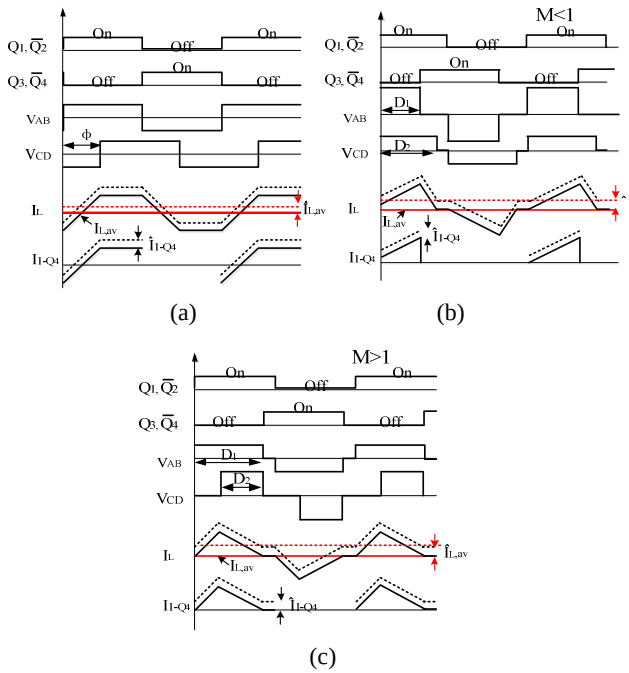


Fig. 6. Small signal relationships between $I_{L,av}(t)$ and $I_{1-Q_4,av}(t)$ in (a) SPSM (b) TRM, when $M < 1$ (c) TRM, when $M > 1$.

A. *Small Signal Behaviors of the DC Bias with Respect to the Duty Cycles*

In the primary side bridge, the small signal behaviors of the DC bias with respect to the duty cycles can be seen in Fig. 7. In SPSM, if there is a duty cycle increment on Q_1, the DC bias increases. Then, the average currents of $I_{1-Q_1,av}$ and $I_{1-Q_4,av}$ increase accordingly. On the contrary, the average currents of $I_{1-Q_2,av}$ and $I_{1-Q_3,av}$ decrease. Therefore, if the processor detects that the DC bias is negative, it should increase the duty cycle of Q_1 to compensate the DC bias, and vice versa. The same logic can also be used in the control of TRM to eliminate the DC bias. However, the control loop has a possibility of oscillating. Therefore, the small signal model in the frequency domain must be observed.

B. *Relationships between the DC Bias and the Duty Cycles in the Frequency Domain*

The hybrid modulation scheme used in PV systems employs TRM and SPSM. These two modulations produce different inductor current shapes. Therefore, the traditional geometry method used in [15] is not good for obtaining the transfer function from the duty cycle of d_1 to the bias current. In SPSM, the state space averaging method is used in a switching period as:

$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = A + B, 0 < t < \phi\frac{T_s}{2}$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = A - B, \phi\frac{T_s}{2} < t < d_1(t)T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = -(A + B), d_1(t)T_s < t < (0.5+0.5\phi)T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = B - A, (0.5+0.5\phi)T_s < t < T_s \quad (6)$$

Where $I_L(t)$ is the current in the primary side inductor, A is the amplitude of $V_{AB}(t)$, B is the amplitude of $V_{CD}(t)$, and R_{para} is the total parasite resistance of the DAB converter (the calculation of R_{para} can found in [22]). It is defined as:

$$R_{para} = R_{primary} + N^2R_{secondary} \quad (7)$$

Where:

$$R_{primary} = 2R_{switch} + R_L + R_{tr1} + R_{PCB,primary} \quad (8)$$
$$R_{secondary} = 2R_{switch} + R_{tr2} + R_{PCB,secondary} \quad (9)$$

Where R_{switch} is the on-resistance of the power switch, R_L is the parasite resistance of the power inductor, R_{tr1} is the parasite AC resistance of the transformer on the primary side, R_{tr2} is the parasite AC resistance of the transformer on the secondary side, $R_{PCB,primary}$ is the AC resistance of the PCB wire on the primary side, and $R_{PCB,secondary}$ is the AC resistance of the PCB wire on the secondary side. Then, the averaged equation can be derived from (6) as:

$$L\frac{dI_{L,av}(t)}{dt} + I_{L,av}(t)R_{para} = 2Ad_1(t) - A \quad (10)$$

In (10), $I_{L,av}(t)$ and $d_1(t)$ can be substituted by $I_{L,av} + \hat{I}_{L,av}$ and $d_1 + \hat{d}_1$. Where $I_{L,av}$ is the steady state part of $I_{L,av}(t)$, $\hat{I}_{L,av}$ is the small signal perturbation on $I_{L,av}$, d_1 is the steady state part of $d_1(t)$, and $\hat{d}_1$ is the small signal perturbation on d_1. Therefore:

$$L\frac{dI_{L,av}}{dt} + I_{L,av}R_{para} + L\frac{d\hat{I}_{L,av}}{dt} + \hat{I}_{L,av}R_{para} = 2Ad_1 + 2A\hat{d}_1 - A \quad (11)$$

Then, the small signal transfer function from $\hat{d}_1$ to $\hat{I}_{L,av}$ in the Laplace domain is:

$$H_{\hat{d}_1\hat{I}_{L,av}}(s) = \frac{\hat{I}_{L,av}}{\hat{d}_1} = \frac{2A}{Ls+R_{para}} \quad (12)$$

When in TRM and $M < 1$, the state equations can be expressed as:

$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = A - B, 0 < t < 0.5D_1T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = -B, 0.5D_1T_s < t < 0.5D_2T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = 0, 0.5D_2T_s < t < 0.5T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = B, 0.5T_s < t < d_1(t)T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = -A + B, d_1(t)T_s < t < (0.5 + 0.5D_1)T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = B, (0.5 + 0.5D_1)T_s < t < (0.5 + 0.5D_2)T_s$$
$$L\frac{dI_L(t)}{dt} + I_L(t)R_{para} = 0, (0.5 + 0.5D_2)T_s < t < T_s \quad (13)$$

Then the averaged equation can be derived as:

$$L\frac{dI_{L,av}(t)}{dt} + I_{L,av}(t)R_{para} = Ad_1(t) - 0.5A \quad (14)$$

In (14), $I_{L,av}(t)$ and $d_1(t)$ can be substituted with $I_{L,av} + \hat{I}_{L,av}$ and $d_1 + \hat{d}_1$. Where $I_{L,av}$ is the steady state part of $I_{L,av}(t)$, $\hat{I}_{L,av}$ is the small signal perturbation on $I_{L,av}$, d_1 is the steady state part of $d_1(t)$, and $\hat{d}_1$ is the small signal perturbation on d_1. Therefore:

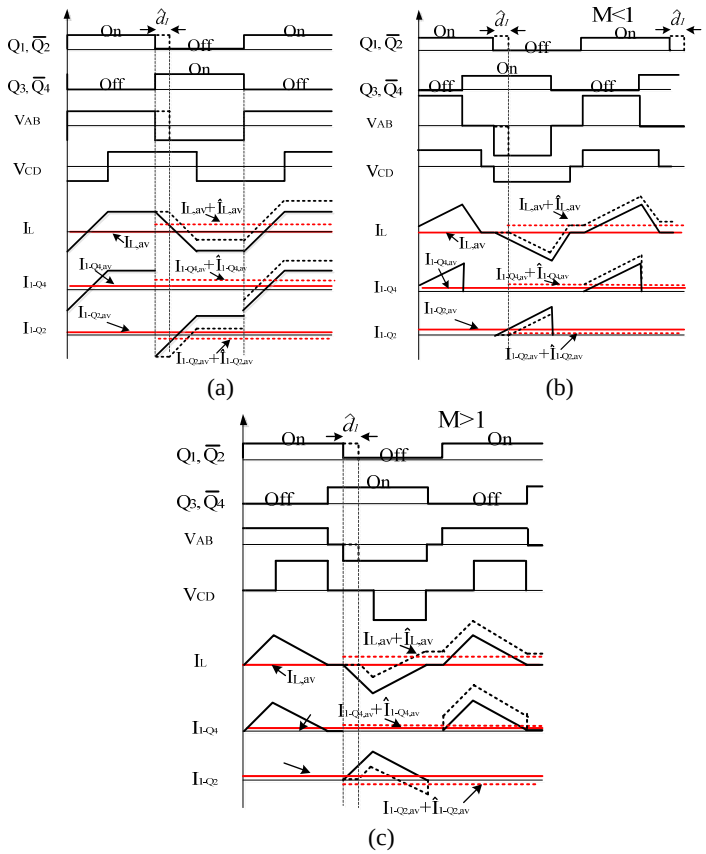


Fig. 7. Small signal relationships between $d_1(t)$, $I_{L,av}(t)$, $I_{1-Q_4,av}(t)$, and $I_{1-Q_2,av}(t)$ in (a) SPSM (b) TRM, when $M < 1$ (c) TRM, when $M > 1$.

$$L\frac{dI_{L,av}}{dt} + I_{L,av}R_{para} + L\frac{d\hat{I}_{L,av}}{dt} + \hat{I}_{L,av}R_{para} = Ad_1 + A\hat{d}_1 - 0.5A \quad (15)$$

Then the small signal transfer function from $\hat{d}_1$ to $\hat{I}_{L,av}$ in the Laplace domain is:

$$H_{\hat{d}_1\hat{I}_{L,av}}(s) = \frac{\hat{I}_{L,av}}{\hat{d}_1} = \frac{A}{Ls+R_{para}} \quad (16)$$

When in TRM and $M > 1$, the state equations can be expressed like those in SPSM. By using the same process, it can be obtained that:

$$\begin{aligned}
L\frac{dI_L(t)}{dt} + I_L(t)R_{para} &= A, 0 < t < (0.5D_1 - 0.5D_2)T_s \\
L\frac{dI_L(t)}{dt} + I_L(t)R_{para} &= A - B, (0.5D_1 - 0.5D_2)T_s < t < 0.5D_1T_s \\
L\frac{dI_L(t)}{dt} + I_L(t)R_{para} &= 0, \quad 0.5D_1T_s < t < d_1(t)T_s \\
L\frac{dI_L(t)}{dt} + I_L(t)R_{para} &= -A, \ d_1(t)T_s < t < (0.5 + 0.5D_1 - 0.5D_2)T_s \\
L\frac{dI_L(t)}{dt} + I_L(t)R_{para} &= B - A, \quad (0.5 + 0.5D_1 - 0.5D_2)T_s < t \\
&< (0.5 + 0.5D_1)T_s \\
L\frac{dI_L(t)}{dt} + I_L(t)R_{para} &= 0, (0.5 + 0.5D_1)T_s \ < t < T_s
\end{aligned} \quad (17)$$

Then the averaged equation can be derived as:

$$L\frac{dI_{L,av}(t)}{dt} + I_{L,av}(t)R_{para} = Ad_1(t) - 0.5A \quad (18)$$

In (18), $I_{L,av}(t)$ and $d_1(t)$ can be substituted with $I_{L,av} + \hat{I}_{L,av}$ and $d_1 + \hat{d}_1$. Where $I_{L,av}$ is the steady state part of $I_{L,av}(t)$, $\hat{I}_{L,av}$ is the small signal perturbation on $I_{L,av}$, d_1 is the steady state part of $d_1(t)$, and $\hat{d}_1$ is the small signal perturbation on d_1. Therefore:

$$L\frac{dI_{L,av}}{dt} + I_{L,av}R_{para} + L\frac{d\hat{I}_{L,av}}{dt} + \hat{I}_{L,av}R_{para} = Ad_1 + A\hat{d}_1 - 0.5A \quad (19)$$

Then the small signal transfer function from $\hat{d}_1$ to $\hat{I}_{L,av}$ in the Laplace domain is:

$$H_{\hat{d}_1\hat{I}_{L,av}}(s) = \frac{\hat{I}_{L,av}}{\hat{d}_1} = \frac{A}{Ls+R_{para}} \quad (20)$$

It can be found that all of the transfer functions from the duty cycles to the DC bias are one-pole functions. The positions of both poles are $R_{para}/(2\pi L)$. Therefore, in the design of the compensator, the position of the pole caused by the average current sensing module should be made to move away from $R_{para}/(2\pi L)$ to avoid oscillation.

The DC gains of (12), (16), and (20) are found to be $2A/R_{para}$, A/R_{para}, and A/R_{para}, respectively. They are finite, which means that the DC bias cannot be eliminated very well. Therefore, the integration must be done in the TMS32f28335.

IV. Design of the DC Bias Compensator

A. *Model of the Compensator*

The DC bias compensator is designed based on the

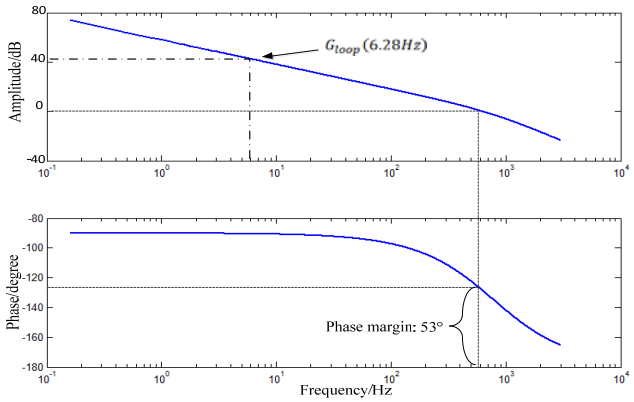


Fig. 8. Target Bode plot of the compensation loop.

proposed small signal model. The bias compensator is designed as follows:

$$G_{comp}(s) = k_{comp}\frac{\frac{s}{a}+1}{s} = \frac{k_{comp}}{a} + \frac{k_{comp}}{s} \quad (21)$$

Where k_{comp}/a is the high-frequency gain of the compensator, and a is the position of the zero. The compensator is a PI controller. The integration can be expressed as:

$$\int_0^t e(\tau)d\tau \approx \frac{t}{n}e\left(\frac{t}{n}\right) + \frac{t}{n}e\left(\frac{2t}{n}\right) + \cdots + \frac{t}{n}e(t) \quad (22)$$

Where $e(\tau)$ is the error signal between I_{Q_1}, and I_{Q_3}. This equation means that the integration can be achieved in the DSP. Then the PI can be expressed in the DSP as:

$$\text{Proportion: } P = e(t)\frac{k_{comp}}{a} \quad (23)$$

$$\text{Integration: } \begin{cases} I = I + e(t)k_{comp}T_s, & \text{if } e(t) < 0 \\ I = I - e(t)k_{comp}T_s, & \text{if } e(t) > 0 \end{cases} \quad (24)$$

The compensation is designed according to the positions of the poles produced by the average current sensing module and $H_{\hat{d}_1\hat{i}_{L,av}}(s)$. The transfer function of the average current sensing module is expressed as:

$$H_{ACS}(s) = G_m R_{sense} G_{AD620}\frac{R_{f2}/R_{f1}}{R_{f2}C_{ACS}s+1} \quad (25)$$

Where G_m is the gain of the mutual inductor. Then, the loop gain of the compensator is expressed as:

$$G_{loop}(s) = -\frac{1}{k}H_{\hat{d}_1\hat{i}_{L,av}}(s)H_{ACS}(s)G_{comp}(s) = \begin{cases} -\frac{2A}{Ls+R_{para}}\frac{1}{D_1}G_m R_{sense}G_{AD620}\frac{R_{f2}/R_{f1}}{R_{f2}C_f s+1}k_{comp}\frac{\frac{s}{a}+1}{s}, SPSM \\ -\frac{A}{Ls+R_{para}}\frac{1}{D_1}G_m R_{sense}G_{AD620}\frac{R_{f2}/R_{f1}}{R_{f2}C_f s+1}k_{comp}\frac{\frac{s}{a}+1}{s}, \ TRM \end{cases} \quad (26)$$

The main specifications and parameters of the prototype's power stage are summarized in Table I. The total parasite resistance is about 0.16Ω. By inserting $R_{para} = 0.16\Omega$, $L = 14\mu H$ into (26), the position of the first pole is obtained at 1.137kHz. To get the average values of I_{Q_2} and I_{Q_4}, $R_{f2} = 1k\Omega$ and $C_f = 0.2uF$ are used. They produce a pole at a frequency of 796Hz. The positions of the two poles are very close. The stability is not good because the phase-frequency characteristic decreases too fast to a value of 180°. Therefore, the zero of the PI is set at 796Hz to offset the pole of the average current sensing module. That is to say $a = 2 \times 10^{-4}$. After the determination of the poles' positions, the gain at a frequency of 6.28Hz must be determined to ensure the phase margin of the control loop. The gain at a frequency of 6.28Hz is expressed as:

$$G_{loop}(6.28\text{Hz}) = \begin{cases} 2\frac{1}{D_1}A\frac{G_m R_{sense}G_{AD620}R_{f2}}{R_{f1}}k_{comp}, & SPSM \\ \frac{1}{D_1}A\frac{G_m R_{sense}G_{AD620}R_{f2}}{R_{f1}}k_{comp}, & TRM \end{cases} \quad (27)$$

The gain at a frequency of 6.28Hz depends on the modulation methods of the DAB converter. Therefore, the DSP should give different values to k_{comp} depending on the modulation methods. Finally, $G_{loop}(6.28\text{Hz})$ is set at 45dB to ensure a phase margin of 53 degrees. A bode plot of the designed compensator is shown in Fig. 8.

TABLE I
MAIN SPECIFICATIONS AND PARAMETERS OF THE PROTOTYPE CONVERTER'S POWER STAGE

Power flow from V_1 to V_2		Power flow from V_2 to V_1	
Parameter	value	Parameter	value
V_1	20~106V	V_1	60V
V_2	60V	V_2	60V
f_s	36kHz	f_s	36kHz
Maximum power	1.2kW	Maximum power	700W
L	14μH	L	14μH
N	1.11	N	1.11
C_1 and C_2	940μF	C_1 and C_2	940μF

TABLE II
COMPONENTS OF THE PROTOTYPE

Left side bridge	8×IRFB4321 MOSFET Electrolytic capacitor 2×500μF Toroidal inductor 13μF
Right side bridge	8×IRFB4321 MOSFET Electrolytic capacitor 2×500μF
Transformer	EE 65 65/34 ferrite core N:1=10:9 $L_{leak,primary}$=1μH, L_{m1}=1.4mH L_{m2}=0.9mH

B. *Interaction between the Compensator and the DAB Converter*

When $I_{L,av}$ varies, $I_{Q1,av}$ and $I_{Q2,av}$ vary. The variations of $I_{Q1,av}$ and $I_{Q2,av}$ affect the input power accordingly. If the input power varies, the output power is affected. Then the variation of the output power leads to a variation of the output voltage. On the other hand, the output voltage affects $I_{L,av}$ in turn. If there is a small signal increment on V_{CD}, there is a small signal increment on the slope of I_L. Then, $I_{L,av}$ varies. That is to say, if the duty cycle varies, the loop of $I_{L,av} \rightarrow V_o \rightarrow V_{CD} \rightarrow I_{L,av}$ is affected. If $I_{L,av}$ is affected, the loop of the compensator is affected. The phenomenon derived by this logic reasoning is called interaction between the loops (IBL). By this logic reasoning, it can be found that there is possibility to make the DAB converter unstable. However,

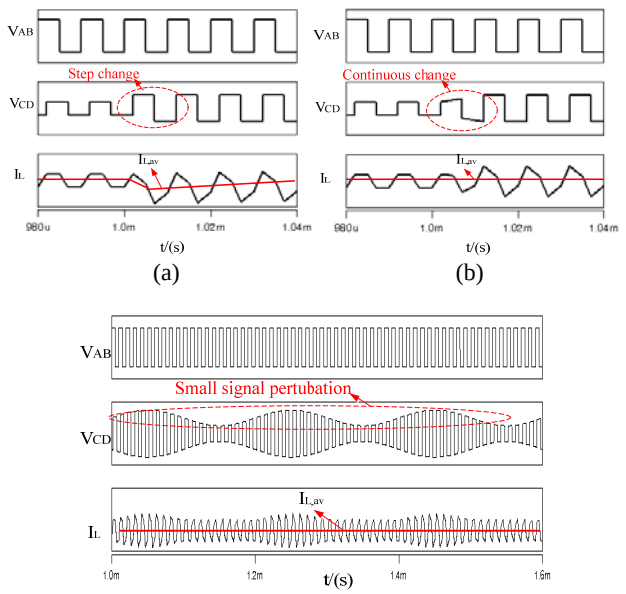


Fig. 9. Simulated results from saber. (a) Relationship between the DC bias and V_{CD} when V_o has a step change. (b) Relationship between the DC bias and V_{CD} when V_o has a continuous change. (c) Relationship between the DC bias and V_{CD} when V_o has a small signal perturbation (the amplitude of the small signal perturbation is exaggerated).

the IBL does not happen in real applications because the small signal gain from V_o to $I_{L,av}$ exists only in the condition where there is a step change in V_o. Two simulations in Saber software are made. The first simulation, which is under the condition of a step change, is shown in Fig. 9(a). The second simulation, which is under the condition of a continuous change is shown in Fig. 9(b). It can be seen that $I_{L,av}$ varies instantaneously when V_{CD} has a step change. The simulation of the step change is coincident with the analysis. However, if there is a continuous change, $I_{L,av}$ does not vary any more. If a small signal perturbation is added to V_o (exaggerated perturbation), the variation of V_o which is shown in Fig. 9(c) is continuous. Then, the small signal gain from V_o to $I_{L,av}$ is zero. Therefore, there is no need to consider the effect from V_o to $I_{L,av}$. That is to say, the loop of $I_{L,av} \rightarrow V_o \rightarrow V_{CD} \rightarrow I_{L,av}$ does not exist in the small signal model. In other words, the IBL does not exist in the DAB converter which uses the DC bias compensator. In the design of the DAB converter with the proposed compensator, it is only necessary to ensure the stabilities of the compensator loop and the loop which stabilizes the output voltage.

V. Experimental Results

The hybrid modulation scheme and the proposed DC bias compensation method in TRM and DPSM are implemented in a TMS320f28335 digital signal processor (DSP). This is a

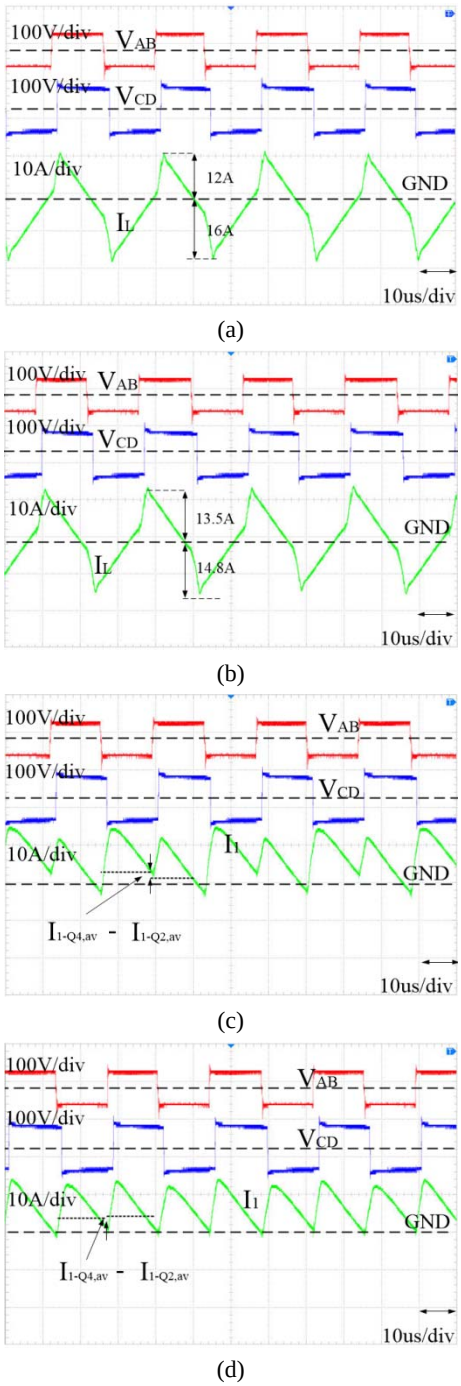
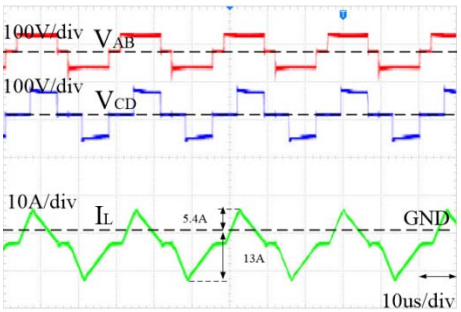
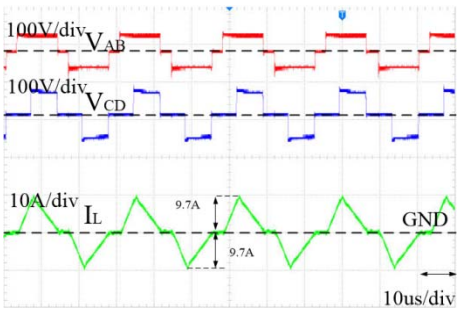


Fig. 10. Key waveforms for DAB during SPSM, M = 1.3 $P_o = 227W$, $V_{in} = 43V$, $V_0 = 58V$. (a) I_L without compensation. (b) I_L with compensation. (c) I_1 without compensation (d) I_1 with compensation.

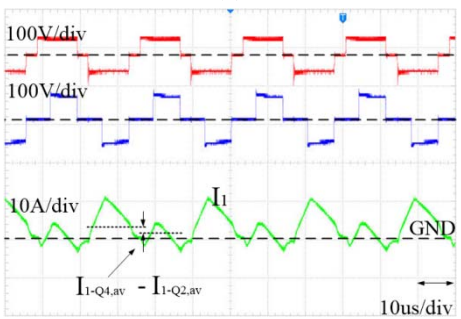
32 bits processor with a Single-Precision Floating-Point unit. It also has a 12 bits ADC which can acquire at least 0.8mV of voltage. Therefore, the proposed modulation scheme and the compensation methods can be achieved by this DSP. In the power stage, IRFB4321 MOSFETs are used as power switches due to their low on-resistance. All of the power switches consist of two MOSFETs. In the transformer, Litz wires are used to reduce the copper loss. The mutual



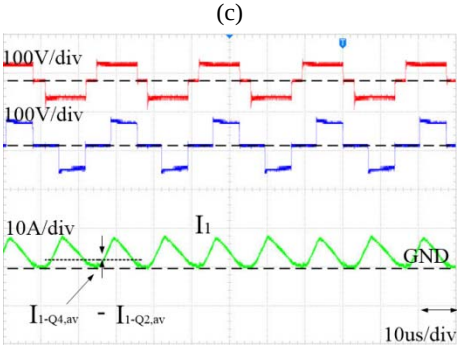
(a)



(b)



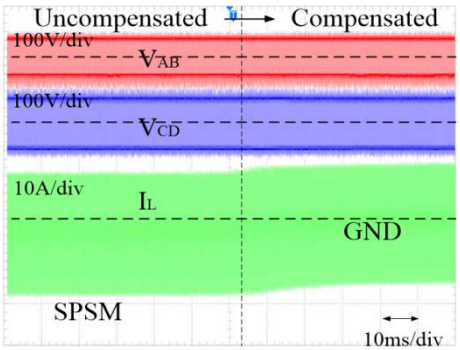
(c)



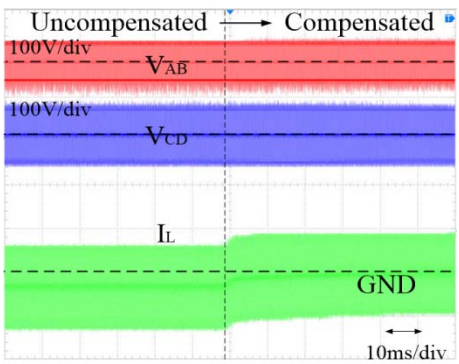
(d)

Fig. 11. Key waveforms for DAB during TRM, M = 1.3 $P_o = 205W$, $V_{in} = 43V$, $V_0 = 58V$. (a) I_L without compensation (b) I_L with compensation. (c) I_1 without compensation. (d) I_1 with compensation.

inductor's turn ratio is selected as 1:2000, the gain of AD620 is 2V/V, and $R_{sense} = 20\Omega$. Q_{s1} and Q_{s1} are 0803GMT MOSFETs. Fig. 10 (a) and (c) show the inductor current and I_1 of the uncompensated DAB converter during SPSM. It can be seen that the upper-peak current value is 12A, while the lower-peak current is 16A, and that I_1 has a two-period oscillation, which means that DC bias exists in the inductor



(a)



(b)

Fig. 12. Key waveforms of the transitions from the uncompensated condition to the compensated condition in (a) SPSM. (b) TRM.

current. Fig. 10 (b) and (d) show the inductor current and I_1 of the compensated DAB converter during SPSM. Although it can be seen that the upper-peak current value is 13.5A, while the lower-peak current is 14.8A, and that I_1 has a very small two-period oscillation, the DC bias is definitely suppressed because the inductor current is a little asymmetrical. Therefore, the upper and lower peak current values are not exactly equal to each other. Fig. 11 (a) and (c) show the inductor current and I_1 of the uncompensated DAB converter during TRM. In TRM, the DC bias is slightly bigger than that in SPSM. The upper-peak current value is 5.4A, while the lower-peak current is 13A. It can be seen that there is a very big two-period oscillation in I_1. After compensation, the upper peak current and the lower peak current are both 9.7A, and the two-period oscillation is eliminated as shown in Fig. 11 (b) and (d). To further demonstrate the improvements of this compensation, the transitions from the uncompensated conditions to the compensated conditions in both the SPSM and the TRM are shown in Fig. 12 (a) and (b). During the transitions, a digital filter is used. The logic is that, in TRM, if the sensed current value gets into the preset region of SPSM, and the variable i increases by 1. If the sensed current value gets out of this preset region of SPSM, the variable i decreases by 1. When i increases to 5, the filter allows the transition from SPSM to TRM, and vice versa. Finally, the efficiencies of the

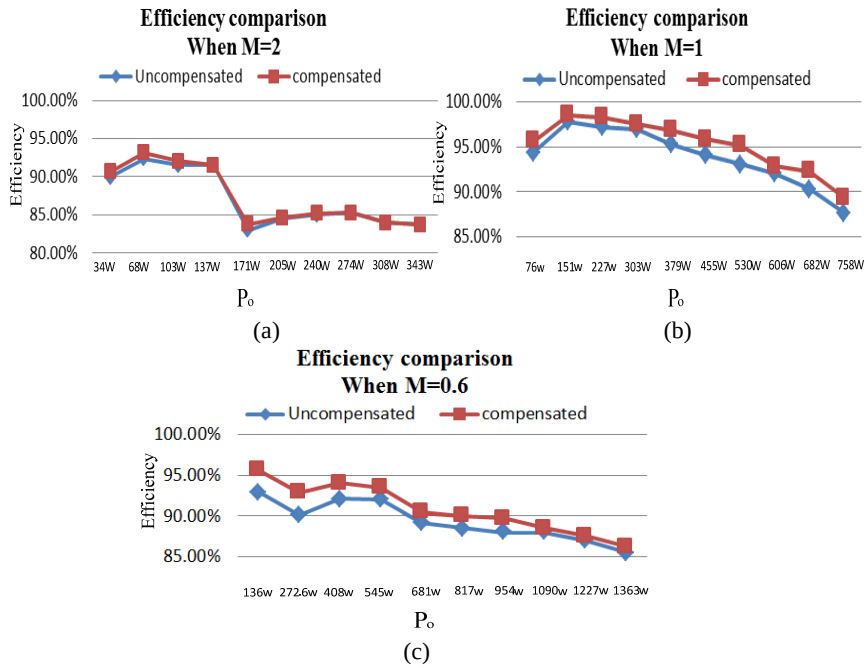


Fig. 13. Efficiency comparisons between the compensated converter and uncompensated converter when $V_0 = 58V$. (a) $M = 2$. (b) $M = 1$. (c) $M = 0.6$.

compensated and uncompensated DAB converters are compared in Fig. 13. This comparison shows that the improvements exist in all of the conditions. When $M = 2$, the improvement is relatively small because the DC bias is small. However, when $M = 1$ and $M = 0.6$, the improvements increase to an average value of 2%.

VI. CONCLUSION

It is found that the efficiency of a DAB converter decreases when DC bias exists. To overcome this problem, this paper proposes a DC bias compensation method to suppress the DC bias of hybrid modulated DAB converters that employ TRM and SPSM. Small signal models of the compensation loops in both the SPSM and the TRM are made to ensure the stability of the proposed method. The design of this compensation is given. Experimental results are given to show that the compensation method can work properly and that the overall efficiency of the DAB converter is improved by about 2% when the proposed method is used.

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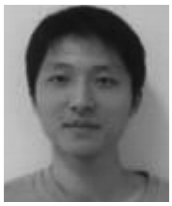

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