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Proton and γ-ray Induced Radiation Effects on 1 Gbit LPDDR SDRAM Fabricated on Epitaxial Wafer for Space Applications

Mi Young Park[1]†, Jang-Soo Chae[1], Chol Lee[1], Jungsu Lee[1], Im Hyu Shin[1], Ji Eun Kim[2]
[1]Korea Advanced Institute of Science and Technology, Daejeon 34141, Korea
[2]Korea Polar Research Institute, Incheon 21990, Korea

We present proton-induced single event effects (SEEs) and γ-ray-induced total ionizing dose (TID) data for 1 Gbit low-power double data rate synchronous dynamic random access memory (LPDDR SDRAM) fabricated on a 5 μm epitaxial layer (54 nm complementary metal-oxide-semiconductor (CMOS) technology). We compare our radiation tolerance data for LPDDR SDRAM with those of general DDR SDRAM. The data confirms that our devices under test (DUTs) are potential candidates for space flight applications.

Keywords: LPDDR, DDR, SDRAM, single event effects, total ionizing dose

1. INTRODUCTION

Double data rate synchronous dynamic random access memory (DDR SDRAM) has been frequently used for space applications because of its high data rate. Hence, it follows that low-power DDR (LPDDR) SDRAM, which is DDR SDRAM that is modified slightly to reduce power consumption, should also be considered for space use because space systems have strict limitations on power consumption. Consequently, the Satellite Technology Research Center (SaTReC) at the Korea Advanced Institute of Science and Technology (KAIST) is developing high density and low-power consuming LPDDR SDRAM modules with 3-dimensional bare die stacks of several LPDDR SDRAM chips for space applications.

In space, electronic devices are exposed to various types of radiation including electrons, heavy ions, and high-energy protons. These radiation particles may cause integrated circuits (ICs) to experience a total ionizing dose (TID) effect or single event effects (SEEs) including single event upset (SEU), burst error, single event functional interrupt (SEFI), and single event latch-up (SEL).

In general, the stacking procedure itself does not significantly affect the radiation performance; thus, the final radiation hardness of our LPDDR SDRAM modules is ultimately subject to a unit chip (3D PLUS 2012). Because the TID and SEE data for LPDDR SDRAM have never been reported, a survey for radiation-hardened LPDDR SDRAM candidates and an analysis of the radiation characteristics of those candidates must be conducted before developing LPDDR SDRAM modules for space applications.

Although the TID response of ICs may be improved by the use of shielding, shielding is not an effective means of improving the SEE response, usually because of the extremely penetrating nature of particles present in natural space environment. In general, while some probability of SEU is acceptable in a space mission, SEL is not. Even a single SEL is usually unacceptable. Thus, design changes to improve SEL response are important for space-grade ICs. One method of improving the SEL response of ICs is to use an epitaxial substrate, which functions by limiting the charge collection volume and by decreasing the substrate series resistance (Dodd et al. 2001). This approach has been used to manufacture radiation-hardened ICs for many years and has worked effectively with heavy ion-induced latch-up.

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†**Corresponding Author**
E-mail: mypark@kaist.ac.kr, ORCID: 0000-0001-6902-2935
Tel: +82-42-350-8632, Fax: +82-42-861-0064

Table 1. Details of DUT

	Description
Part number	H5MS1G62
Manufacturer	SK Hynix
Type	LPDDR SDRAM
Technology	54 nm CMOS
Density	1 Gbit (4 banks × 16 Mbit × 16 I/O)
Power supply	$V_{DD} = V_{DDQ} = 1.70\text{~}1.95$ V
Interface	LVCMOS 1.8 V
Epitaxial layer thickness	5 μm

For this reason, 1 Gbit LPDDR SDRAM fabricated on a 5 μm epitaxial layer from SK Hynix is chosen and analyzed for its radiation hardness characteristics.

The significance of this paper is as follows:

1) The first suggestion of proton-induced SEE data for LPDDR SDRAM;
2) The first suggestion of proton-induced SEE data for a SDRAM fabricated on an epitaxial layer.

In this paper, we demonstrated proton-induced SEE with a primary emphasis on SEU, burst error, SEFI, and SEL and γ-ray-induced TID data for 1 Gbit LPDDR SDRAM fabricated on a 5 μm epitaxial layer from SK Hynix.

2. DEVICE UNDER TEST (DUT) PREPARATION

As mentioned above, an LPDDR SDRAM is a DDR SDRAM slightly modified to reduce power consumption without performance degradation. The low-power features of the LPDDR SDRAM include reduced supply voltage (1.8 V), partial array self-refresh, temperature compensated self-refresh, and a deep power down mode. Table 1 and Fig. 1 present the details and functional block diagram of the DUT (SK Hynix 2015).

Because the range (> 6.5 mm) of the protons used in our experiments is significantly greater than the thickness (1.65 mm) of the epoxy mold compound of the DUT package, the protons can penetrate sufficiently deep into the active regions of the DUTs without removing the epoxy mold compound of the DUTs. For experimental convenience, 11 mm × 11 mm × 1.65 mm land grid array (LGA) packages were used. Fig. 2(a) shows a photocopy of the DUT.

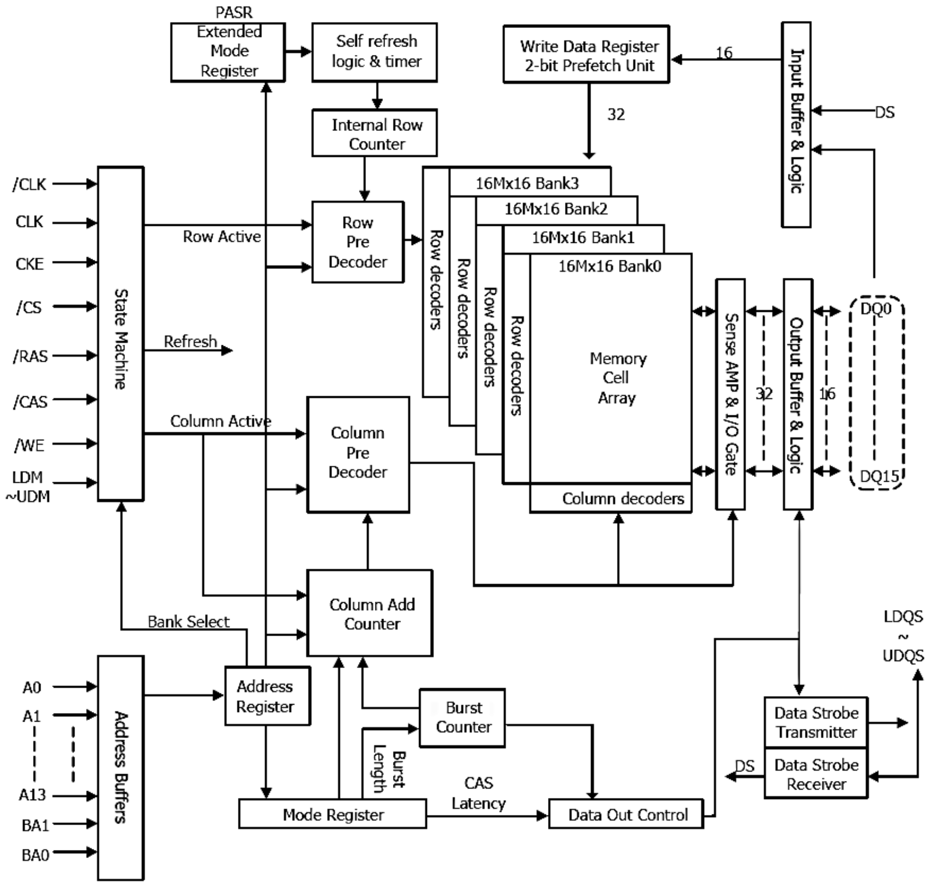
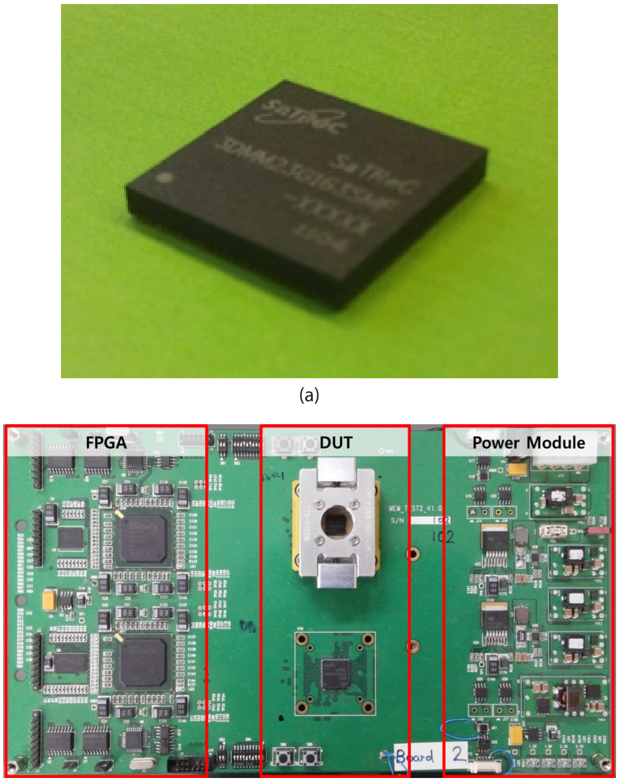


Fig. 1. Functional block diagram of 4 banks x 16 Mbit x 16 I/O LPDDR SDRAM.



(a)

(b)

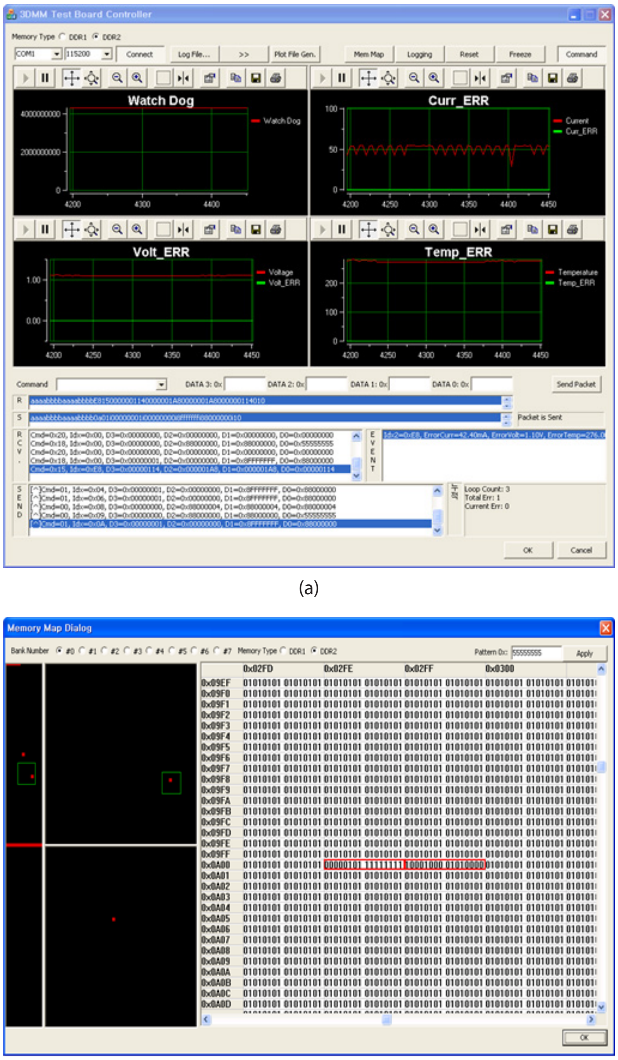
Fig. 2. (a) DUT and (b) test board.

3. TEST EQUIPMENT

The test system is equipped with a test board, power supply with a general purpose interface bus (GPIB) to remotely control the power, a personal computer (PC) with software program to control and monitor the DUT functions and printed circuit board (PCB) power, and a PC to remotely monitor and control the test. Fig. 2(b) displays the test board. It is capable of operating a DUT at a clock frequency of up to 200 MHz with a Xilinx Spartan-6 field-programmable gate array (FPGA) and contains a socket to mount the DUTs. Because all the components, including the DUT, FPGA, and power modules, are on a single test board, special care must be taken for the location of the non-radiated components on the test board. Accordingly, all electronics except the DUT (top center in Fig. 2(b)) were located outside the diameter of the proton beam (~3 cm) to minimize the possibility of proton-induced degradation, as indicated in Fig. 2(b). The separation between the DUT and all other active components is greater than 5 cm.

The main functions of the test board are as follows:

- Biasing all components on the board;
- Reading/writing/comparing data for DUTs;
- Monitoring errors and status of DUTs (refer to Fig. 3);



```
R  aaaabbbbaaaabbbbE81500000001140000001A80000001A8000000114010
S  aaaabbbbaaaabbbb0a01000000010000000008fffffff8800000010
Packet is Sent

Cmd=0x20, Idx=0x00, D3=0x00000000, D2=0x00000000, D1=0x00000000, D0=0x00000000
Cmd=0x18, Idx=0x00, D3=0x00000000, D2=0x88000000, D1=0x88000000, D0=0x55555555
Cmd=0x20, Idx=0x00, D3=0x00000000, D2=0x00000000, D1=0x00000000, D0=0x00000000
Cmd=0x18, Idx=0x00, D3=0x00000001, D2=0x00000000, D1=0x8FFFFFFF, D0=0x88000000
Cmd=0x15, Idx=0xE8, D3=0x00000114, D2=0x000001A8, D1=0x000001A8, D0=0x00000114

Idx=0xE8, ErrorCurr=42.40mA, ErrorVolt=1.10V, ErrorTemp=276.0

[^]Cmd=01, Idx=0x04, D3=0x00000001, D2=0x00000000, D1=0x8FFFFFFF, D0=0x88000000
[^]Cmd=01, Idx=0x06, D3=0x00000001, D2=0x00000000, D1=0x8FFFFFFF, D0=0x88000000
[^]Cmd=00, Idx=0x08, D3=0x00000000, D2=0x88000004, D1=0x88000004, D0=0x88000004
[^]Cmd=00, Idx=0x09, D3=0x00000000, D2=0x88000000, D1=0x88000000, D0=0x55555555
[^]Cmd=01, Idx=0x0A, D3=0x00000001, D2=0x00000000, D1=0x8FFFFFFF, D0=0x88000000

Loop Count: 3
Total Err: 1
Current Err: 0
```

```
Pattern 0x: 55555555

        0x02FD            0x02FE            0x02FF            0x0300
0x09EF  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F0  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F1  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F2  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F3  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F4  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F5  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F6  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F7  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F8  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09F9  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09FA  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09FB  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09FC  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09FD  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09FE  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x09FF  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A00  01010101 01010101 00000101 11111111 10001000 01010000 01010101 01010101 010101
0x0A01  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A02  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A03  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A04  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A05  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A06  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A07  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A08  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A09  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A0A  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A0B  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A0C  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
0x0A0D  01010101 01010101 01010101 01010101 01010101 01010101 01010101 01010101 010101
```

(a)

(b)

Fig. 3. Control and monitoring errors and status of DUTs: (a) dialog for sending command/receiving telemetry and (b) memory error map.

- Logging:
  - Addresses, values, and time stamps of all errors;
  - Current values for the entire test board and DUT

4. TEST FACILITY

4.1 Proton-induced SEE Test Facility

The Korea multi-purpose accelerator complex (KOMAC) 100 MeV proton accelerator and the Korea Institute of Radiological & Medical Sciences (KIRAMS) MC-50 cyclotron facility were used for the proton-induced SEE tests. Figs. 4 and 5 are photographs of the radiation room for the KOMAC 100 MeV proton accelerator and KIRAM MC-50 cyclotron, respectively. The proton beams at KOMAC are 45 MeV

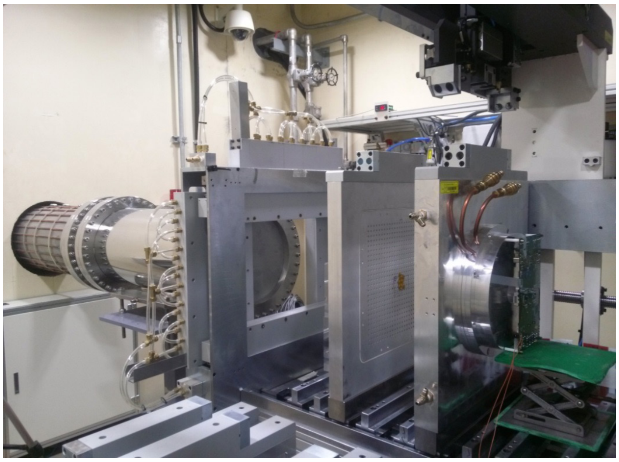


Fig. 4. Radiation room for KOMAC 100 MeV proton accelerator.

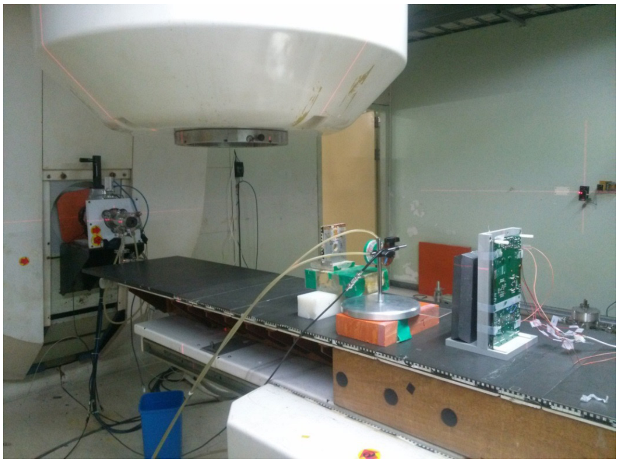


Fig. 5. Radiation room for KIRAMS MC-50 cyclotron facility.

and 94.5 MeV-energy pulsed beams. The proton beams at KIRAMS are 35 MeV and 45 MeV-energy continuous wave beams. All proton testing were performed at normal incidence. The properties of the proton beams used in our experiments are indicated in Tables 2 and 3.

4.2 γ-ray-induced TID Test Facility

The Co-60 gamma source for low-level gamma irradiation of the Korea Atomic Energy Research Institute (KAERI) was used for the TID test. Fig. 6 is a photocopy of the radiation room of the Co-60 gamma source. The TID level exposed to the DUTs was above 166 krad(Si) (dose rate: 35.4 krad(Si), exposure time: 4.7 hr). The irradiation conditions for the TID test are summarized in Table 4. Because all components including the DUT were on a single test board, all parts of the test board except the DUTs were required to be shielded from the γ-rays using lead bricks as indicated in Fig. 6. Dosimeters were placed on top of each sample.

Table 2. 100 MeV proton accelerator at KOMAC (pulsed beam)

Energy (MeV)	Range in silicon (mm)	Pulse repetition rate (Hz)	Pulse width (μs)	Flux (protons/cm^2·pulse)
44.4	10.1	1 or 2	100	$2.93 \cdot 10^8$
94.5	37.8	1 or 2	100	$3.00 \cdot 10^8$

Table 3. MC-50 cyclotron at KIRAMS (continuous wave beam)

Energy (MeV)	Range in silicon (mm)	Flux (protons/cm^2·s)
35	6.5	$1.99 \cdot 10^8$
45	10.1	$1.99 \cdot 10^8$

5. TEST DESCRIPTION

5.1 Proton-induced SEE Test

The primary focus of our proton-induced SEE experiments was to characterize the tolerance of the DUT to SEU, burst error, SEFI, and SEL. It is important to know the SEU, burst error, and SEFI cross section versus proton energy and to determine the SEL threshold proton energy because, in general, some probability of SEU, burst error, and SEFI is acceptable, whereas a single SEL is unacceptable in a space system.

Both functional testing and current monitoring were performed to detect SEU, burst error, and the SEFI cross section versus proton energy, and to determine the SEL threshold proton energy. Moreover, examination of memory error maps, re-initialization of the DUT, and recycling of the power supply were carefully performed to distinguish SEL from SEU, burst error, and SEFI.

The functional tests were performed at a clock frequency of 166 MHz with normal bias setting ($V_{DD} = V_{DDQ} = 1.8$ V). The entire memory device was tested using a checkerboard pattern (a logical series of ones and zeros) and dynamic tests were performed. The test flow was as follows (Ladbury et al. 2006):

- Write DUT with a checkerboard pattern;
- Read back and verify DUT repeatedly;
- Begin irradiation;
- Correct any error before continuing reading if the data stored in the DUT are determined to be changed;
- Terminate the test when the desired number of upsets is recorded or maximum fluence has been attained.

During testing, the supply current to the DUTs was monitored to detect any meaningful increase, which would indicate the occurrence of a latch-up. In our experiments, the SEL threshold current was set to a value ten percent higher than the static bias supply (Schwank et al. 2013).

All tests were conducted at room temperature and multiple devices were used to avoid TID degradation effects

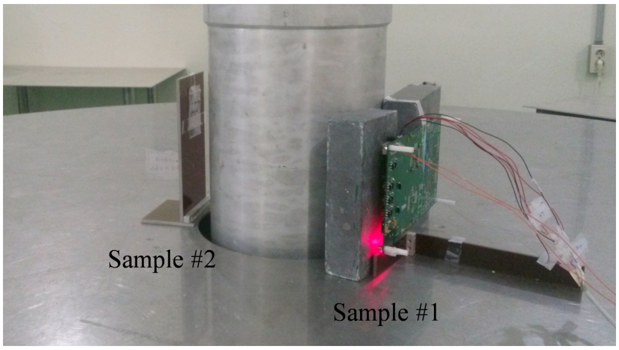


Fig. 6. TID test configuration.

and stuck bit accumulation. Different devices were used for each experiment. When stuck bits occurred, the device was replaced with a new, identical chip.

In this paper, data were classified into: (Ladbury et al. 2006; Koga et al. 2007)

- SEUs:
  SEUs cause a change of state in a memory cell. This type of event causes no permanent damage and the device can be reprogrammed for correct function after such an event has occurred.
- Burst errors:
  Burst errors cause upsets at many address locations, which could be as many as 1,000, with one ion strike. They can be written over with the original pattern (or other patterns). This type of event causes no permanent damage and the device can be reprogrammed for correct function after such an event has occurred.
- SEFIs:
  SEFIs cause components to malfunction. These are similar to burst errors. However, the device can no longer be reprogrammed for correct function. They require software conditioning (without power-up) for recovery.
- SELs:
  SELs cause parasitic n-p-n-p structures in complementary metal-oxide-semiconductor (CMOS) to trigger and generate high current flow, which can possibly lead even to the destruction of the DUT. SELs are not recovered by stopping the beam and reinitializing the DUT. They require power recycling for recovery.
- Stuck bits:
  Stuck bits are memory cells that always read as a fixed value, regardless of the data written to the cell. They persist after recycling power unless they anneal.

5.2 γ-ray-induced TID Test

In the TID test, we monitored only current variances and whether the DUTs functioned normally. No additional parametric measurements were made (Ladbury et al. 2006). Two samples were used with different test configurations. During irradiation, Sample #1 was operated by the test board, same as in the SEE test. Sample #2 was located separately and unbiased, as indicated in Fig. 6. The same test board and test procedures were used for the TID test for Sample #1 as those for the SEE test.

Table 4. Irradiation condition for TID test

Sample #	TID (krad(Si))	Time (hr)	Dose rate (krad(Si)/hr)	Test mode
1	166.0	4.7	35.4	Biased and functioned
2	200.6	4.7	42.7	Unbiased

6. DATA ANALYSIS

6.1 Proton-induced SEE Performance

Because there are many kinds of proton energies in space (Schwank et al. 2013), if some probability of single event effects is acceptable, a complete SEE cross section curve versus proton energy is required to calculate the error rates expected when using the device in a given radiation environment. The goal of SEE cross section is to minimize it; therefore, lower values of SEE cross section are more desirable. This cross section (σ) is calculated in units of cm^2/device or cm^2/bit (ESCC 2002; Koga et al. 2007)

$$\sigma = N/(F\cos\theta) \qquad (\mathrm{cm^2/device}) \tag{1}$$

$$\sigma = N/(F\cos\theta\, D) \qquad (\mathrm{cm^2/bit}) \tag{2}$$

where N is the number of events for SEEs, F is the particle fluence (particles/cm^2), θ is the incident angle of the proton beam measured with respect to the DUT surface normal, and D is the DUT density (bits). In this paper, the unit of cm^2/bit is used for data normalization among the different chips having different density.

To test the sufficient proton-induced SEE performance of the DUT, it was required that the experiment be performed with a radiation source where the proton energy was over a range from at least 20 to 180 MeV (Schwank et al. 2013). However, the maximum proton energy used in this experiment was 94.5 MeV because the maximum energy of the domestic proton accelerator is approximately 100 MeV. Therefore, this paper verifies that the DUT used in this experiment is a potential candidate for space application rather than a sufficient space compatible chip. To test the sufficient space compatibility of the DUT, additional experiment (heavy-ion SEE) with the support of a facility aboard would have to be performed later.

In our experiments, we observed only isolated SEUs in scattered memory address locations. No burst errors, SEFI, or SEL occurred in our experiments; however, Micron 1 Gbit DDR SDRAM experienced SEU, burst error, and SEFI (Koga et al. 2007). Hence, there was no requirement to recycle the power supply or reinitialize the DUT. Figs. 7-9 present the proton-induced SEE cross section data for the 1 Gbit LPDDR SDRAM from SK Hynix. In these figures, we plotted the SEE cross section data using error bars to represent statistical uncertainty owing to the finite number of events observed. Because the number of observed events in our experiments was small (< 20), even though the minimum fluence of our experiments was 10^{11} protons/cm^2, we used Swift's correction factors instead of Poisson statistics. This provides the statistical limits with 95 % confidence (essentially two sigma) (Swift & Johnston 2007).

Fig. 7 is the proton-induced SEU cross section curves for our 1 Gbit LPDDR SDRAM from SK Hynix, the Micron 1 Gbit DDR SDRAM (Koga et al. 2007), and the Samsung 1 Gbit and 512 Mbit DDR SDRAM (Ladbury et al. 2006). As indicated in Fig. 7, our DUT SEU cross section value was at least ten times less than that for the Micron and Samsung DDR SDRAM. Our DUT was fabricated in 54 nm CMOS technology node, whereas the Micron 1 Gbit DDR SDRAM, Samsung 1 Gbit DDR SDRAM, and Samsung 512 Mbit DDR SDRAM were fabricated in 90 - 110 nm, 100 nm, and > 100 nm CMOS technology node, respectively. Our DUT had higher density compared to the other devices. Although many CMOS technologies that are advanced in performance and density typically exhibit an SEU threshold drop with feature size (Dodd et al. 2010), Fig. 7 illustrates improved SEU characteristics with shrunken feature size. Ladbury et al. (2006) also demonstrated that reduced feature size does not necessarily correlate to reduced radiation performance. The SEU performance of the DUTs identifies them as effective candidates for space flight applications. It is interesting to note that our SEU cross section data normalized with beam fluence depend on the instantaneous beam flux (particles/cm^2·s). Fig. 7 indicates that the SEU cross section is inversely proportional to the instantaneous beam flux when the beam is on. The reason for this result is not yet understood; it is beyond the scope of this paper. To characterize DUT susceptibility to SEU for different instantaneous flux, a further rigorous analysis is required.

Fig. 8 presents the burst errors and SEFI cross section as a function of proton energy for our DUT and the Micron 1 Gbit DDR SDRAM (Koga et al. 2007). As mentioned previously, because we did not detect any sign of burst error or SEFI, we provided an upper limit to the occurrence of SEFI in Fig. 8. Although the possibility of burst errors and SEFI below the 94.5 MeV proton energy value cannot be definitely ruled out, this figure and the minimum fluence used (10^{11} protons/cm^2) suggests that the burst error and SEFI performance of our DUT are superior to those of the Micron 1 Gbit DDR SDRAM.

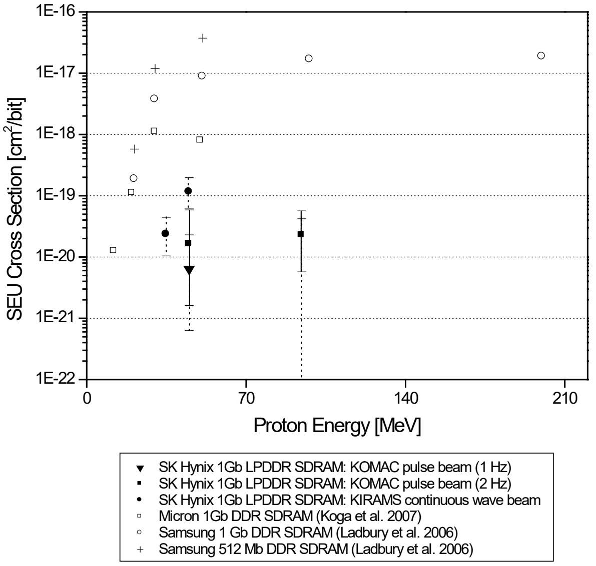


Fig. 7. Proton-induced SEU cross section.

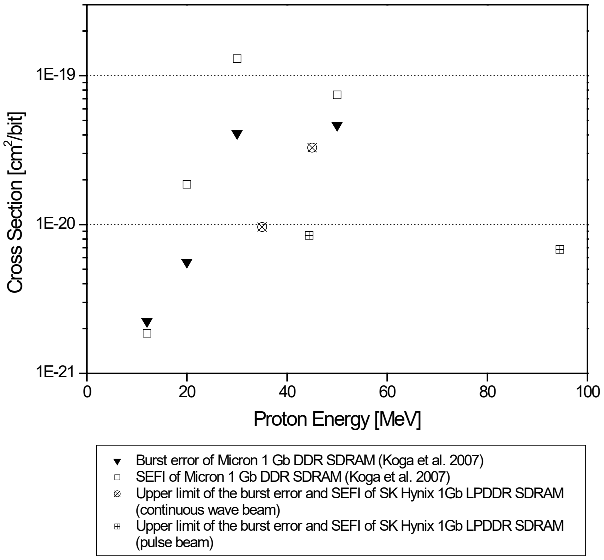


Fig. 8. Proton-induced burst error and SEFI cross section.

6.2 γ-ray-induced TID Degradation

The TID for a device in a space environment is dependent on mission orbit, mission life time duration, shielding

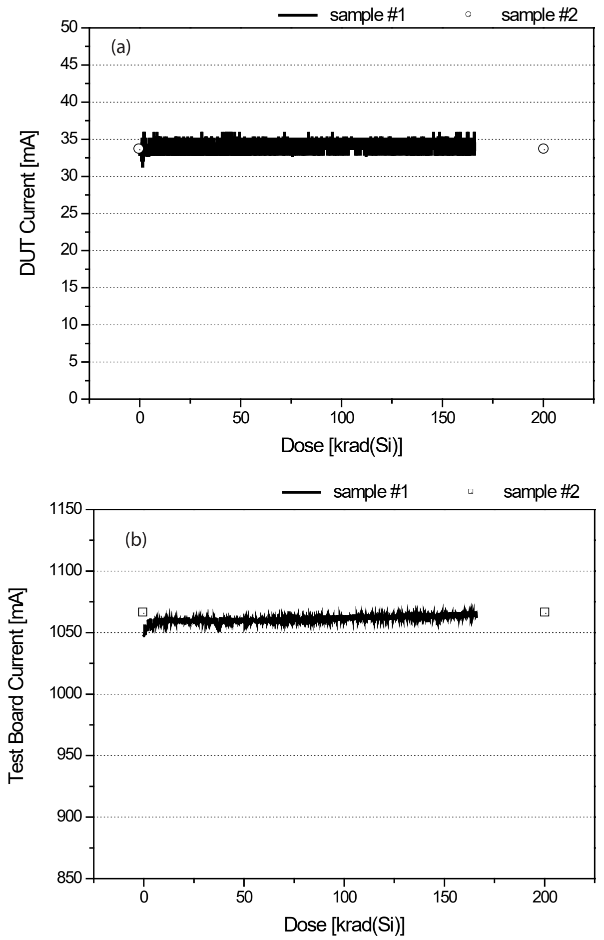


Fig. 9. Current consumption versus accumulated ionization dose: (a) DUT current (b) test board supply.

thickness, and other factors. If a geostationary orbit (GEO) satellite system with 5 mm Al shielding material has a mission duration of 18 years, the TID exposed to the satellite-borne equipment is approximately 88.4 krad(Si) (Hong & Heo 2010). The TID specification of radiation tolerant DDR SDRAM manufactured by 3D Plus is greater than 60 krad(Si).

For CMOS devices, TID tolerance has increased with device scaling (Dodd et al. 2010). In our experiments, TID data addressed only DUT current variances, supply current variances, and whether the DUTs functioned normally as the dose accumulated.

The biased and functioned DUT (Sample #1) performed with no errors and no apparent degradation to 166.0 krad(Si) irradiation. Fig. 9 indicates the DUT current consumption and test board supply current versus accumulated dose. Over the course of 166.0 krad(Si) irradiation, the current consumption increased by less than 0.5 %. For the unbiased DUT (Sample #2), the DUT functionality and current consumption were captured for only two points (before and after irradiation) because it was impossible to monitor them during irradiation. The results of Sample #2 were similar to those of the functioned DUT (Sample #1): it also indicated no errors and the current consumptions of DUT and test board supply after 200.6 krad(Si) irradiation demonstrated a similar level of the functioned DUT (Sample #1).

7. CONCLUSION

In space systems, which have strict limitations on power consumption and radiation hardness, it is important to use radiation-hardened low-power consuming ICs. This paper presented the proton-induced SEE and γ-ray-induced TID data for SK Hynix 1 Gbit LPDDR SDRAM fabricated on an epitaxial layer for the first time. The data confirmed that our DUTs could be effective candidates for space flight applications. Although the radiation tolerance data for the DUT suggested in this paper indicated excellent promise for use in space missions, heavy ion-induced SEE tests must be performed to complete the evaluation of radiation tolerance.

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