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A New Single-Phase Asymmetrical Cascaded Multilevel DC-Link Inverter

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Abstract

This paper presents a new single-phase asymmetrical cascaded multilevel DC-link inverter. The proposed inverter comprises two stages. The main stage of the inverter consists of multiple similar cells, each of which is a half-bridge inverter consisting of two switches and a single DC source. All cells are connected in a cascaded manner with a fixed neutral point. The DC source values are not made equal to increase the performance of the inverter. The second circuit is a folded cascaded H-bridge circuit operating at a line frequency. One of the main advantages of this proposed topology is that it is a modular type and can thus be extended to high stages without changing the configuration of the main stage circuit. Two control schemes, namely, low switching with selective harmonic elimination and sinusoidal pulse width modulation, are employed to validate the proposed topology. The detailed approach of each control scheme and switching pulses are discussed in detail. A 150W prototype of the proposed system is implemented in the laboratory to verify the validity of the proposed topology.

Key words: Cascaded multilevel inverter, DSPIC microcontroller, MLDC link inverter, SHE, SPWM.

I. INTRODUCTION

Multilevel inverters (MLIs) represent a significant advancement in the field of power electronics and have recently gained increasing attention because of their advantages over conventional two-level inverters. The most important features of MLI topologies include (a) their high voltage capability and (b) their output voltages that are very near the sinusoidal waveform with low total harmonic distortion (THD), which results in a small output filter. The most popular topologies used in MLIs are the neutral point clamped (NPC) inverters, flying capacitors inverters, and cascaded H-bridge (CHB) inverters [1]-[3].

CHB MLIs are divided into two main groups:(1) symmetric and (2) asymmetric. The symmetric structure of a CHB inverter uses equal and isolated DC voltage sources for each H-bridge cell. A CHB can generate up to the 2n + 1 level of the phase voltage depending on the modulation index (MI); here, "n" is the number of H-bridge inverters per phase. CHB DC sources are usually obtained from three-phase or single-phase diode-bridge rectifiers [3], [4], [5], [13]with the aid of transformers to provide electrical isolation. The construction processes for symmetrical and asymmetrical cascaded H-bridge inverters are almost similar, except that an asymmetrical CHB uses unequal and isolated DC voltage sources [6]. The most popular ratios for DC voltage sources are binary and tertiary ratios, which can generate up to $2^{(n+1)} - 1$ and 3^n levels of phase voltages, respectively.

Another type of CHB is called the multilevel DC-link inverter. The first multilevel DC-link inverter was introduced in 2003 [7]. As described in [8]-[14], multilevel DC-link inverters have gained significant attention in the last decade. They have been implemented for both single phase and three phases, including in symmetric and asymmetric topologies. Each arm consists of "n" cells connected in series to generate only positive voltage steps of the arm voltage. The basic cell consists of a single DC source and two switches; one switch is connected in series to the DC source, whereas the other switch is connected in parallel to the DC source. Thus, a basic cell is similar to a half-bridge inverter, and it can

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generate two voltage steps:0V and the DC source voltage. A single arm of "n" cells can generate up to n+1 steps and 2^n steps for symmetric and asymmetric topologies, respectively. Therefore, asymmetric topologies offer more advantages than symmetric topologies do because asymmetric topologies reduce the number of switches and gate drive circuits. Generally, a single-phase inverter requires an extra full-bridge circuit known as a folded cascaded or polarity generation circuit [15], [16]. The final output voltage is synthesized by the combination of the input DC voltages of all series-connected units [11], [17]. This topology exhibits modular characteristics because all its units are similar and share the same control strategy. Therefore, defective units can be replaced or bypassed without discontinuing the load by modifying the control method [18], [19].

Several topologies with a fixed neutral point for their DC sources have been proposed and described in the literature. A single-phase MLI with four input sources is proposed in [20]; this topology comprises three DC sources with a fixed neutral point. In [15], Najafi et al. propose the so-called "reversing voltage" MLI topology, which also has a fixed neutral point for its DC sources. These proposed topologies can be considered as one feature of the MLDC link inverter because they comprise two stages: one for voltage level generation and another for polarity generation. Unfortunately, an asymmetrical source configuration (binary or tertiary) cannot be implemented for existing systems because all subtractive and additive combinations of input voltage levels cannot be synthesized.

The present study proposes a new asymmetrical single-phase multilevel topology inverter. This topology is an extension of the MLDC link inverter topology proposed in [7], but it does need to isolate its DC sources. The paper is organized as follows. Section II describes and explains the general block diagram, configuration, and operating principles of the proposed inverter. Section III presents the modulation techniques that can be employed and the generation of switch pulses. Serving as a reference for inverter validity, Section IV provides the PSIM-simulated results and laboratory measurements. These results are used to verify the performance of the proposed MLI, the analysis of which is presented in Section II. Finally, Section V summarizes the proposed inverter concepts presented in the paper.

II. Operating Principles of Proposed Topology

Generally, single-phase hybrid multilevel topologies [7], [15], [21]-[23] generate output voltages using two cascaded circuits. The first circuit is called the level generation circuit, and it is responsible for level generating in positive polarity. This circuit normally requires high-frequency switches to generate the required levels, and its switches should feature high switching frequency capability. The second circuit is called the polarity generation circuit (folded cascaded circuit), and it is responsible for generating the polarity of the output voltage. This polarity generation circuit is a simple single-phase H-bridge inverter that is considered as a low-frequency component operating at a line frequency.

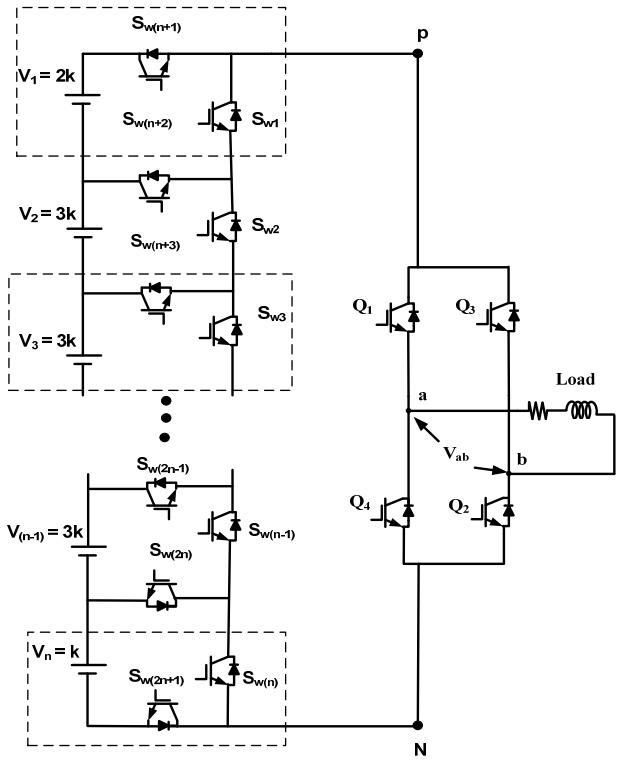


Fig. 1. General structure of the proposed single-phase asymmetrical cascaded inverter.

Fig. 1 shows the general structure of the proposed hybrid single-phase multilevel inverter. It consists of two circuits, namely, the level generation and polarity generation circuits. The proposed topology offers two main advantages:(1) a high level switch ratio (LSR) [9] resulting from unequal DC voltage values reduces the number of components used; (2) the DC sources are always connected in series (with a common neutral point).The general structure of the level generation circuit is shown in Fig. 1. It consists of "n" cells, each of which comprises a single DC source and two switches. The bottom and top cells are fixed cells with a DC source ratio of 1:2. The repeated cells in the middle are similar and show equal DC sources. Their value is three times the bottom DC source value. The ratio of the bottom DC source to the top one is 1:2 while each repeated cell has a DC value that is three times that of the bottom cell. The generation circuit comprises a total of "N_{sw}" switches, and it can generate arm voltage levels "N_L" for v_{pN}. The load voltage after the polarity circuit is composed of voltage levels (N_{LP}). N_L and N_{sw} can be evaluated using Equs. (1) and (2).

$$N_L = N_{sw} = 2n+1 \quad (1)$$

TABLE I
ON/OFF SWITCH OPERATIONS TO GENERATE SEVEN-LEVEL ARM VOLTAGE VPN FOR N= 3

State no.	V_{pN}	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	SW_7
1	0	ON	ON	ON	OFF	OFF	OFF	OFF
2	k	ON	ON	OFF	OFF	OFF	ON	ON
3	2k	OFF	ON	ON	ON	ON	OFF	OFF
4	3k	ON	OFF	ON	OFF	ON	ON	OFF
5	4k	ON	OFF	OFF	OFF	ON	ON	OFF
6	5k	OFF	OFF	ON	ON	OFF	ON	OFF
7	6k	OFF	OFF	OFF	ON	OFF	OFF	ON

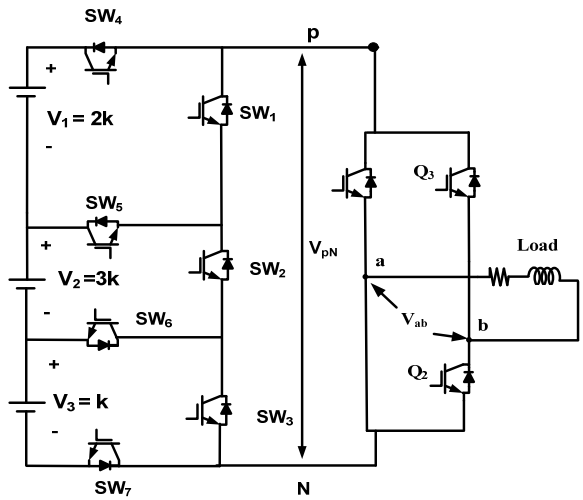


Fig. 2. (a) Proposed system configuration for n=3. (b)Output load voltage V_{ab}

$$N_{LP} = 2\,N_L - 1 = 4n+1 \quad (2)$$

For n=3, the bus (phase arm) voltage and output load voltage can be calculated in terms of the switch signals from the following equations:

$$V_{PN} = V_1\overline{SW_1} + V_2\overline{SW_2} + V_3\overline{SW_3} \quad (3)$$

$$\boldsymbol{V_{ab} = V_{PN}\,(Q_1 - Q_3)} \quad (4)$$

For simplicity, a three-cell (n=3) topology shown in Fig. 2(a) is tested, and its ON/OFF switch operation is given in Table I. This topology comprises seven switching states that can synthesize the 7 levels of the arm voltage v_{pN} and the 13 levels for V_{ab}, as shown in Fig. 2 (b). The direction of the switches SW4–SW7 must be properly chosen to prevent short circuits in the DC sources. Therefore, the two upper switches $\boldsymbol{SW_4}$and $\boldsymbol{SW_5}$ are connected in the opposite direction to the two lower switches $\boldsymbol{SW_6}$and $\boldsymbol{SW_7}$, respectively.

III. MODULATION TECHNIQUES FOR THE PROPOSED MLI

The MLI modulation techniques are divided into two categories according to the switching frequency used to operate the inverter switches: (a) low-frequency modulation techniques and (b) pulse-width modulation (PWM) techniques. In this work, both modulation techniques are studied and employed to generate sinusoidal output voltage waveforms, as explained in the following subsections.

A. Low-Frequency Modulation Techniques

Low-frequency modulation techniques are significant because they drastically reduce switching losses [24], [25]. Therefore, such techniques are considered and studied in detail. The three-cell arm inverter shown in Fig. 2 is considered to test the proposed single-phase MLI. The proposed inverter is simulated using a PSIM software package tool. In this method, the selective harmonic elimination (SHE) [3] technique is employed to eliminate the3rd, 5th, 7th, 9th, 11th, and 13th harmonic orders. Therefore, the harmonic contents of the output load waveform begin in the 15thorder. To this end, Fourier transforms for the well-known stepped waveform shown in Fig. 2(b) can be calculated in Equ. (5) as

$$V(\omega t) = \frac{4k}{\pi}\sum_{n=1,3,5,7,\ldots}[\cos(m\theta_1) + \cos(m\theta_2) + \cdots + \cos(m\theta_l)]\frac{\sin(m\omega t)}{m} \quad (5)$$

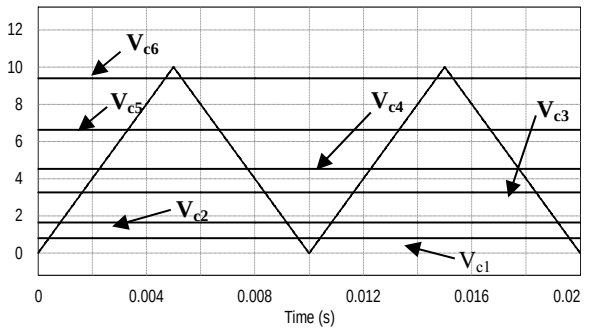
where$k$is the value of the stepped voltage or the lowest DC inverter voltage shown in Fig. 2 and l' is the number of steps. Based on(5), the normalized magnitudes of the Fourier coefficients are given in Equ. (6).

$$H(m) = \frac{1}{m}[\cos(m\theta_1) + \cos(m\theta_2) + \cdots + \cos(m\theta_l)],\ m = 1, 3, 5, 7, \ldots \quad (6)$$

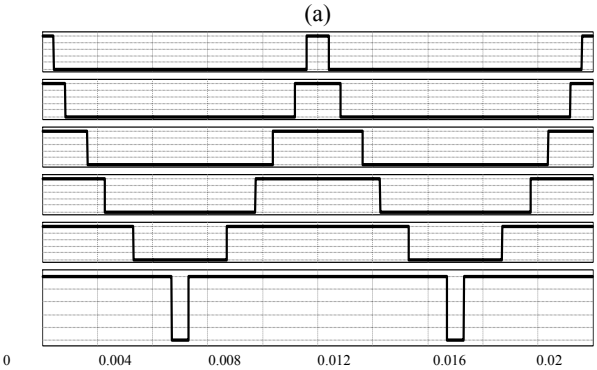
The studied case of the proposed topology shown in Fig. 2 comprises six steps $l = 6.\mathrm{T}$ therefore, with the application of the SHE control technique, each step can cancel one harmonic order. Thus, the 3rd, 5th, 7th, 9th, 11th, and 13th harmonic orders can be cancelled. This can be realized by equating the normalized values calculated from (6) to 0. Then, the solution of the resultant set of nonlinear transcendental equations provides the following values.

$$\theta_1 = 7.27^o,\ \theta_2 = 14.94^o,\quad \theta_3 = 29.44^o,$$
$$\theta_4 = 40.86^o,$$
$$\theta_5 = 59.61^o,\ \theta_6 = 87.55^o,$$

Generating the switch pulses of SW1–SW7 involves six voltages V_1–V_6, which are compared with a single triangle waveform V_{tr1}, as shown in Fig. 3(a). Six signals c_0 -– c_5.are generated for this comparison. These six signals are utilized to generate the pulses of the switches. The voltages



(a)



(b)

Fig. 3. Generating of switch pulses using the SHE technique (two periods from 0 ms to 20ms). (a) Carrier and six constant voltages.(b) ON/OFF signals from top to bottom c0, c1, c2, c3, c4, c5.

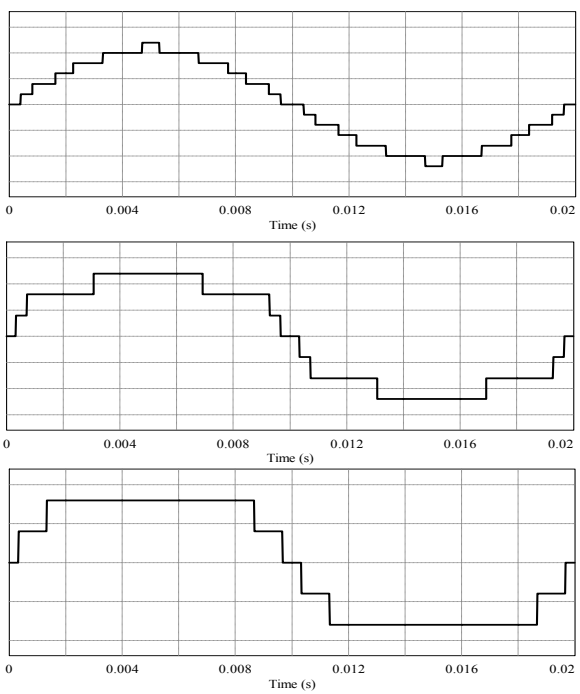
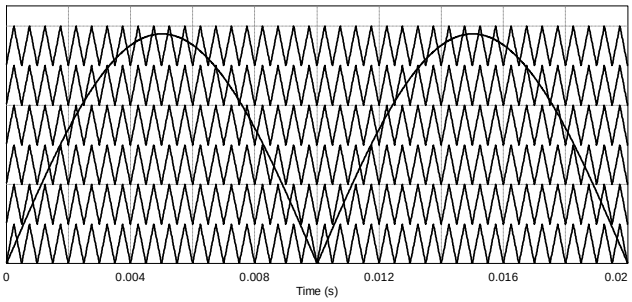


Fig. 4. Simulated waveforms of V_{ab} at different modulation indexes for the proposed inverter (voltage step of V_{ab} = k).

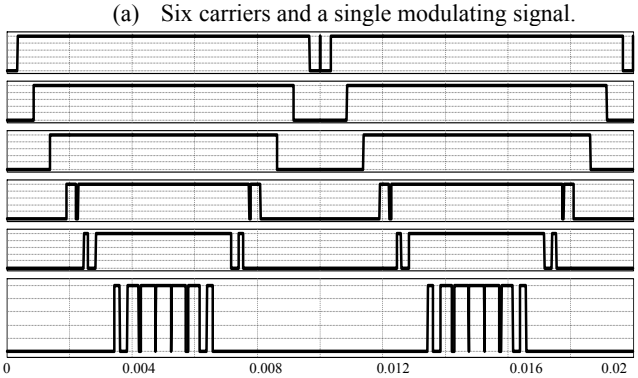
V_1–V_6 are related to the above six angles θ_1–θ_6 as follows:

$$V_i = \frac{1000\,\theta_i}{2\pi f} \quad , \qquad i = 1,2,\dots,6$$

where θ_i is in radian and f is the load line frequency (Hz).



(a) Six carriers and a single modulating signal.



(b) Signals from top to bottom: cm1, cm2, cm3, cm4, cm5, cm6.

Fig. 5. Generation of switch pulses using the SPWM technique.

The triangle carrier has a frequency of$2f$ and an amplitude of 10, as shown in Fig. 3(a). The pulses of the switches are calculated as follows:

$$SW_1 = c_2 - c_1 + c_5 - c_4 + \bar{c_5}$$
$$SW_2 = c_1 + c_4$$
$$SW_3 = c_1 - c_0 + c_3 - c_2 + c_5 - c_4$$
$$SW_4 = c_1 - c_0 + c_4 - c_3 + \bar{c_5}$$
$$SW_5 = c_1 - c_2 + c_4$$
$$SW_6 = c_2$$
$$SW_7 = c_0 - c_1 + c_3 + c_5 - c_4 \qquad (7)$$

where (+) denotes the logic OR and (−) is generated using the exclusive OR and normal AND gates. Therefore, this method generates switching signals in the same manner as that of the PWM technique without the need to use a lookup table, which requires data storage and extra memory. Fig. 4 shows the load output voltage for different modulation indexes.

B. PWM Technique

This type of modulation technique is implemented by comparing sinusoidal and triangular waveform signals. The comparison produces the Boolean signals required to generate switch control pulses. Thus, the SPWM technique is applied for the proposed topology. It uses six carrier signals with equal amplitudes (A_{cr}) but is shifted by a DC level that is equal to the carrier amplitude. These six carrier signals are compared with one rectified sinusoidal waveform with a peak value (A_m) given by Equ. (8). The comparison is shown in Fig. 5(a), and the resulting Boolean output produces the main pulse signals cm1–cm6 shown in Fig. 5(b). After logical

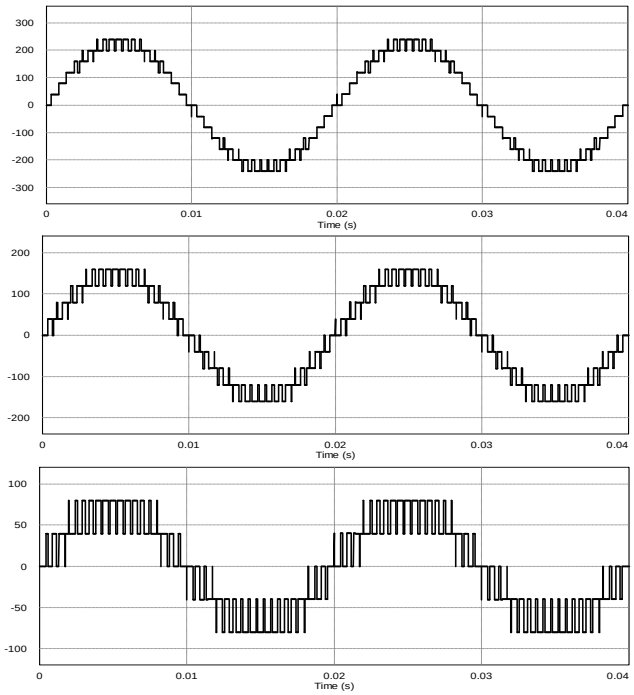


Fig. 6. Simulated waveforms of V_{ab} at different modulation indexes for the proposed inverter (voltage step of V_{ab} = k).

processing on cm1–cm6, the switch pulses SW_1–SW_7 can be generated as specified in (9).

$$A_m = MI * 6 * A_{cr} \tag{8}$$

$$SW_1 = (cm_2 \cdot \overline{cm_3}) + cm_5$$
$$SW_2 = (cm_2 \cdot \overline{cm_5})$$
$$SW_3 = (cm_1 \cdot \overline{cm_2}) + (cm_3 \cdot \overline{cm_4}) + (cm_5 \cdot \overline{cm_6})$$
$$SW_4 = (cm_1 \cdot \overline{cm_2}) + (cm_4 \cdot \overline{cm_5}) + cm_6$$
$$SW_5 = (cm_3 \cdot \overline{cm_5}) + \overline{cm_2}$$
$$SW_6 = \overline{cm_3}$$
$$SW_7 = \overline{cm_1} + (cm_2 \cdot \overline{cm_4}) + (cm_5 \cdot \overline{cm_6}) \tag{9}$$

where (+) and (·) stand for the logic OR and logic AND, respectively. Fig. 6 shows the output voltage waveforms for different modulation indexes. The output voltage levels for this inverter with three cells can vary from 3 levels to 13levels, as shown in Fig. 6.

IV. Simulation and Experimental Results

The proposed topology is simulated using the PSIM software package tools. A three-cell arm (n=3) shown in Fig. 2(a) is tested to validate the proposed system. However, the proposed topology can be extended to *n* cells. Power supplies with 40, 80, and 120 V are selected to follow the ratio of 1:2:3. A 2 kHz switching frequency is used in the case of the PWM control method. A single-phase RL load with 370Ω resistance and 0.6H inductor is used.

A small-scale single-phase inverter with the same simulation parameters is built, tested experimentally, and then compared with the simulation results. The inexpensive

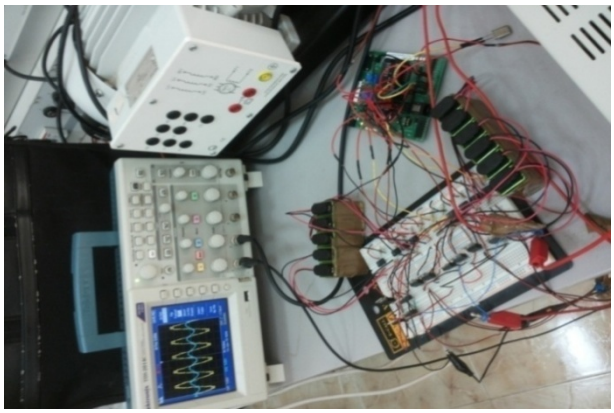


Fig. 7. Experimental setup of the proposed prototype.

dspic30F2010 microcontroller is utilized to generate the switching signals. The prototype setup of the proposed MLI is shown in Fig. 7. It includes three DC power supplies, switching devices, measurement tools, the dspic30F2010 controller, and the RL load.

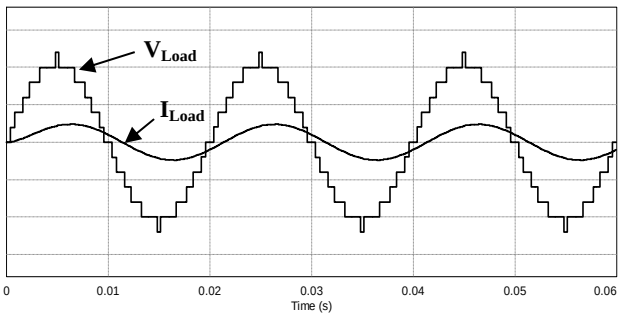
First, the system is simulated with the low switching control technique with A_m = 5.8. The SHE technique is subsequently employed to cancel lowest-order harmonics (i.e., 3rd-, 5th-, 7th-, 9th-, 11th-,and13th-order harmonics). The output voltage and load current waveforms of the simulation and experimental results are shown in Figs. 8(a) and (b), respectively. The peak voltage is 240V, and the peak current is approximately 0.5A.

The harmonic contents start from the 15thharmonic, as shown in Figs. 8(c) and (d), which provide the harmonic spectra of the output load voltages in the simulated and real-time implementation using DSPACE 1007. The THD of the load voltage is approximately 8.27%, which meets the recently published results [3]. Fig. 9 shows the experimental results of the switch pulses for SW_1–SW_7, in addition to the switches of the H-bridge inverter.

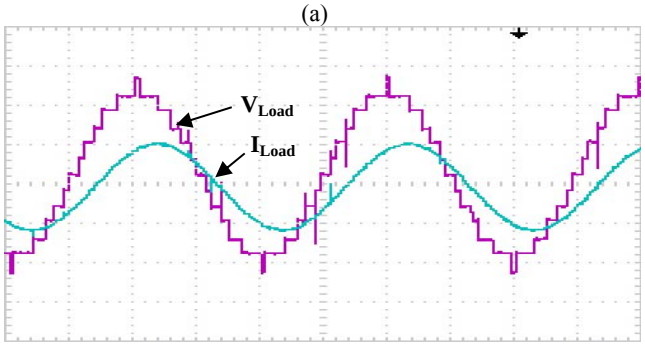
The performance of the proposed single-phase MLI topology is tested using PWM for MI=0.95. Figs. 10(a) and (b) show the simulation and experimental results of the load voltage and load current, respectively, for the same system parameters. The peak voltage is 240V, and the peak current ≅ 0.5A in the simulation and experiment. The load voltage THD is shown in Fig. 10(c) using DSPACE 1007; the harmonics are centered on the switching frequency and its multiples. Fig. 11 shows the switching pulses for SW_1–SW_7switches and the switches of the full-bridge inverter. The simulation and experimental results show a good agreement.

The proposed three-cell topology is simulated using PWM to estimate the THD of the load voltage for a wide range of modulation indexes. The result is plotted in Fig. 12. The THD is reduced to approximately less than 10% of the modulation index near unity.

Table II compares the proposed system with other designs and control methods for the same number of cells per arm.



(a)



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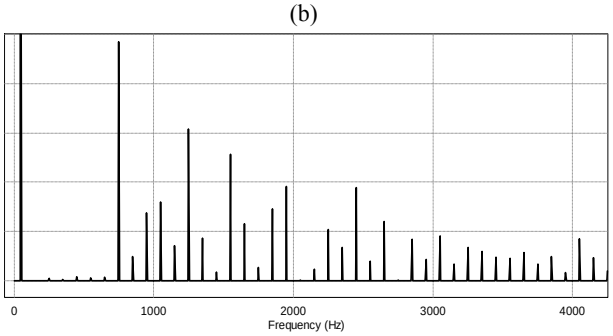
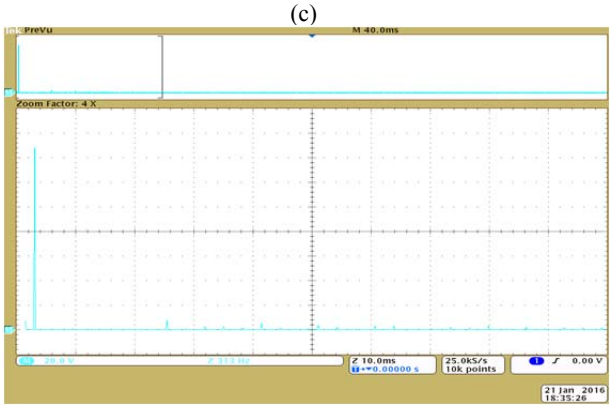


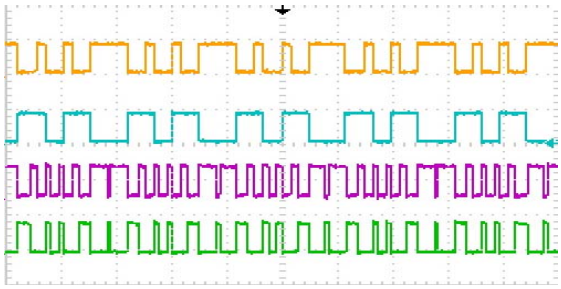
(c)



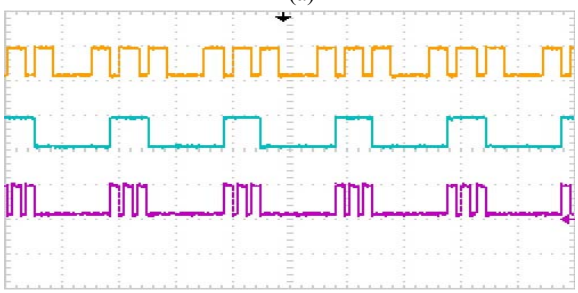
(d)

Fig. 8. (a) Simulation: load voltage, 100V/div; load current, 1A/div, time, 10ms/div. (b) Experimental: load voltage, 100V/div; load current, 0.5 A/div; time 5, ms/div. (c) Harmonic spectrum of the simulated load voltage. (d) Real-time implementation of the harmonic spectrum of the load voltage.

The comparison involves the number of switching devices, main power diodes, inverter levels, and LSR. The proposed topology shows the second highest level/switch (LSR) ratio among all the other designs. In addition, the proposed topology exhibits a significant advantage because of its fixed neutral point.



(a)



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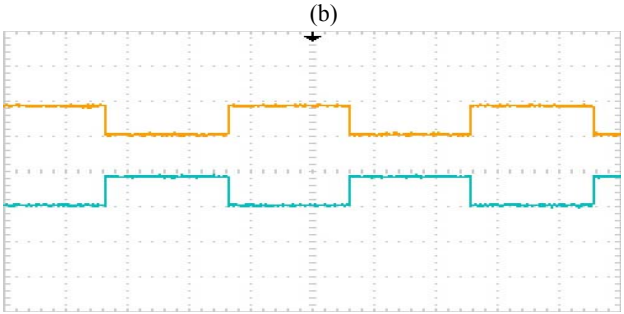
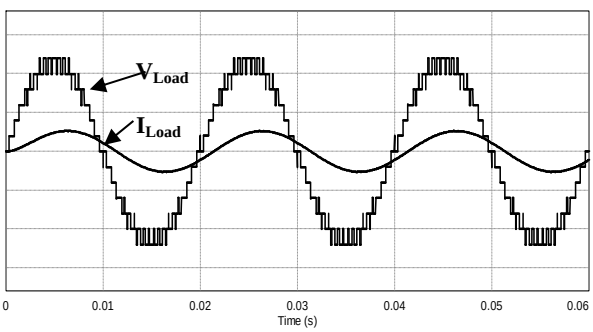
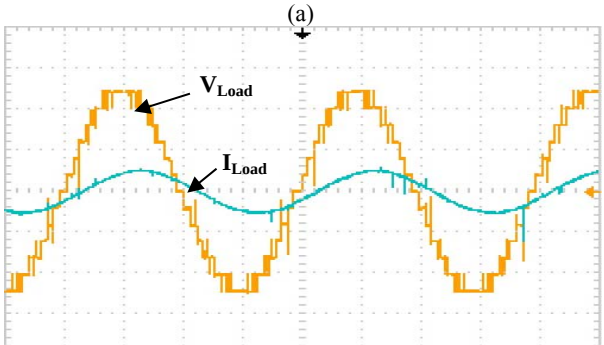


(c)

Fig. 9. Experimental results of switch pulses using the SHE control scheme (5ms/ div), (a) switch pulses SW_1–SW_4, (b) switch pulses SW_5–SW_7, (c) switch pulses Q_1 and Q_3.



(a)



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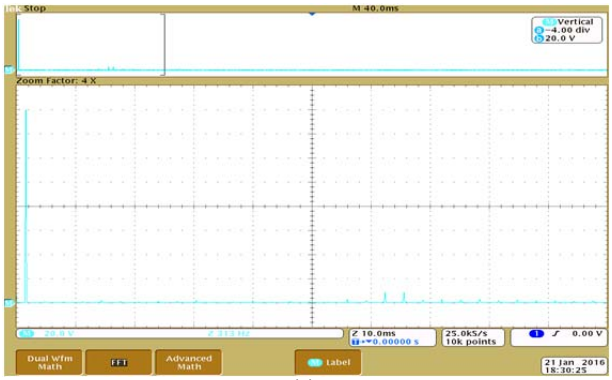
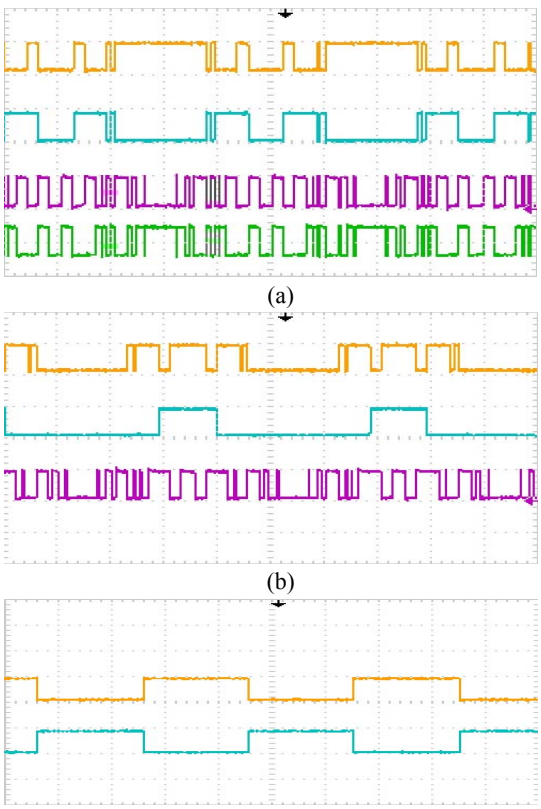


(c)

Fig. 10. (a) Simulation: load output voltage and current for SPWM at MI=0.95 (1A/div, 100V/div, 10ms/div), (b) Experimental: load output voltage and current for SPWM at MI=0.95 (1A/div, 100V/div, 5 ms/div), and (c) Real-time implementation of the harmonic spectrum of the load voltage.



(a)

(b)

(c)

Fig. 11. Experimental results of switch pulses using(b) switch pulses SW_5-SW_7, 2.5ms/div; and(c) switch pulses Q_1-Q_3, 5ms/div.

V. Power Loss Analysis

Power losses and inverter efficiency are approximately evaluated. The conduction and switching losses for the switches, including their freewheeling diodes, are considered, whereas the losses of the gate drives and snubber circuits are neglected. The MOSFET IRF9640PBF is used as a power switch. On the basis of the MOSFET data sheet, the following equations are utilized to approximate the proposed inverter losses:

Switch conduction losses, $P_{cond.,M} = \frac{1}{T}\int_0^T I_M^2 R_{ds,on}\, dt$

Diode conduction losses, $P_{cond,D} = \frac{1}{T}\int_0^T I_D V_{DF} dt$

Switch switching losses, $P_{SW,M} = \frac{1}{8T}\int_0^T I_M V_{M,off}\, dt$

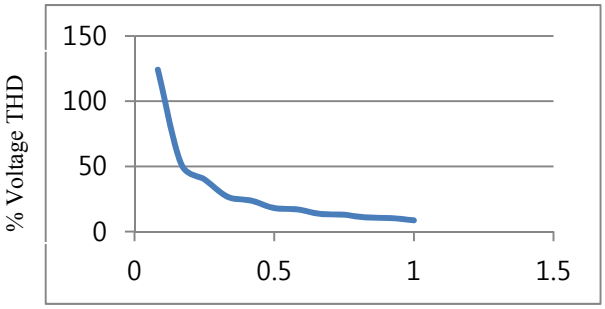
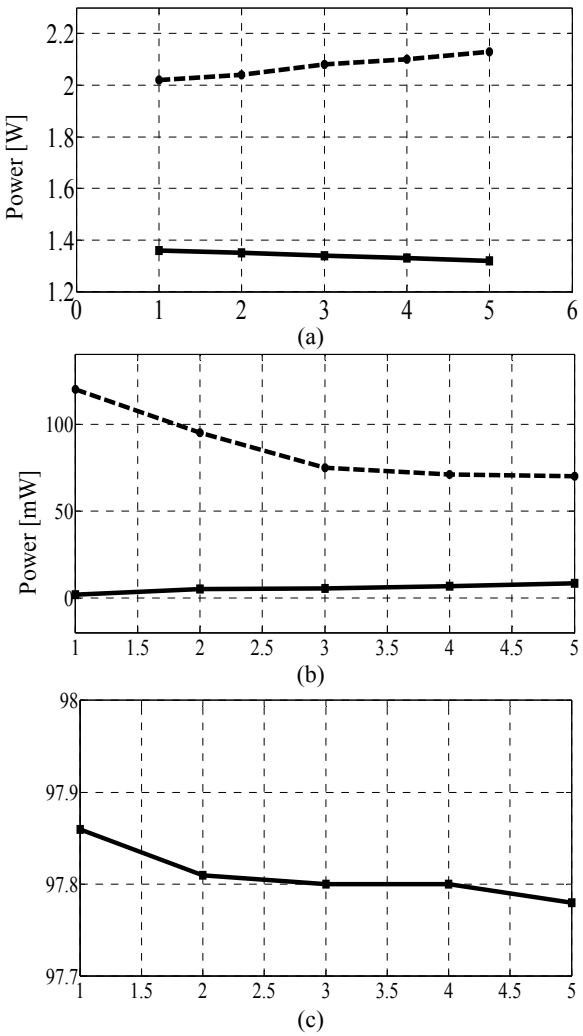


Fig. 12. Modulation index versus load voltage THD.



(a)

(b)

(c)

Fig. 13. (a) Total conduction losses (dashed line for diodes and solid line for switches), (b) Total switching losses (dashed line for diodes and solid line for switches), and (c) percentage efficiency.

TABLE II
COMPARISON BETWEEN THE PROPOSED MLI TOPOLOGY AND OTHER SYSTEMS FOR THE SAME NUMBER OF CELLS PER ARM

	Proposed MLI inverter Topology	MLDC link inverter		Ref[26]	Ref[15]	Ref[20]	Ref[3]
		Symmetric [7], [14]	Asymmetric [8]				
No. of switching devices(Single phase)	11	10	10	15	10	7	15
Main power diodes	0	0	0	12	0	0	12
Phase-to-neutral voltage levels	7	4	8	7	4	4	7
Level/switch ratio	0.636	0.4	0.8	0.466	0.466	0.57	0.47
No. of DC voltage sources (single phase)	3	3	3	3	3	3	3
DC sources	Not isolated	Isolated	Isolated	Isolated	Not isolated	Not isolated	Isolated

Diode switching losses, $P_{SW,M} = \frac{1}{4T}\int_0^T Q_{rr} V_{D,off}\, dt$

where

I_M = Switch conduction current

I_D = Freewheeling diode forward current

$R_{ds,on}$ = switch ON resistance calculated from the data sheet, 0.75 Ω at 80°

V_{DF} = Diode forward voltage calculated from the data sheet, 1.7V

V_{MF} = Switch blocking voltage

V_{DF} = Diode blocking voltage

Q_{rr} = Body diode reverse recovery charge from the data sheet, 3.6 μC

After calculating the total losses of the inverter, the efficiency is then calculated as follows:

$$\%\,\eta = \frac{P_{out}}{P_{out} + P_{loss}}$$

The losses and efficiency of the proposed MLI are evaluated at about 150 W output power and a switching frequency ranging from 1 kHz to 5 kHz. Fig. 13(a) depicts the total conduction losses of both switches and their freewheeling diodes, which represent the dominant losses. Fig. 13(b) shows the total switching losses of both switches and their freewheeling diodes, which are very low in comparison with the conduction losses. This result is attributed to two main factors.(1) In an MLI, the switching of an individual switch or diode is lower than the switching frequency of the whole system.(2) The MOSFET used exhibits extremely low rise and fall times during switching. Fig. 13(c) provides the MLI efficiency under the considered light load. This efficiency changes slightly as the switching frequency varies.

VI. CONCLUSION

A new single-phase asymmetrical MLI with non-isolated DC sources is proposed. The proposed inverter is composed of a level generation circuit and a folded cascaded H-bridge circuit. The operational principles of the proposed inverter are explained in detail. Low switching and PWM control schemes are employed successfully. A generation of pulses and their equations are also provided along with the details of the two control schemes. The LSR of the proposed topology with up to three cells is approximately close to that of existing systems. In addition, the DC sources exhibit a fixed neutral point. The analysis, simulation, and experimental results are provided to validate the proposed system. A dspic30F2010 microcontroller is used to implement the control system and generate MLI switch signals.

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