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A Novel Controller for Electric Springs Based on Bode Diagram Optimization

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Abstract

A novel controller design is presented for the recently proposed electric springs (ESs). The dynamic modeling is analyzed first, and the initial Bode diagram is derived from the s-domain transfer function in the open loop. The design objective is set according to the characteristics of a minimum phase system. Step-by-step optimizations of the Bode diagram are provided to illustrate the proposed controller, the design of which is different from the classical multistage leading/lagging design. The final controller is the accumulation of the transfer function at each step. With the controller and the recently proposed δ control, the critical load voltage can be regulated to follow the desired waveform precisely while the fluctuations and distortions of the input voltage are passed to the non-critical loads. Frequency responses at any point can be modified in the Bode diagram. The results of the modeling and controller design are validated via simulations. Hardware and software designs are provided. A digital phase locked loop is realized with the platform of a digital signal processor. The effectiveness of the proposed control is also validated by experimental results.

Key words: Bode diagram, Controller design, Electric spring, Minimum phase system, Modeling, Phase control, Renewable energy systems

I. INTRODUCTION

The use of renewable energy sources (RESs) is encouraged and promoted all over the world. The intermittent nature of RESs, such as wind and solar energy, is regarded as their common flaw, which leads to stability issues and mismatch problems between the power generation and the load demand of future smart grids [1]-[3]. For instance, the power generated by synchronous generators changes as the load varies because they keep the system stable by compensating for the power difference from the energy stored in high rotor inertia. However, for future smart grids with low inertia, the aforementioned issue could be problematic. Although static var compensators (SVCs) and static var generators (SVGs) can act as reactive power compensators to stabilize ac mains voltages [4]-[9], neither can realize the function in which the load demand matches the power generation dynamically. Moreover, SVCs and SVGs can only provide pure reactive power compensation. Electric springs (ESs) have recently been proposed as a new smart grid technology for regulating ac mains in distributed power grids and achieving a new control paradigm of load demand following power generation [10]. ESs are embedded into non-critical loads to form smart loads for absorbing wide voltage fluctuations. Fluctuations introduced by RESs can be passed to non-critical loads when ESs are equipped massively over distributed power systems.

The use of ESs is described in [11]-[14], and hardware and control implementations are demonstrated in [15]. The load characteristic of ESs is analyzed in [16]. The general steady-state analysis and control principle with different types of compensations are described in [17]. The dynamic modeling of ESs is presented in [18], which provides differential formulas but does not establish a unified form of the transfer function from the reference to the output. The δ control algorithm with a proportional resonant (PR) controller is proposed in [19], which defines δ as the phase angle at which the critical load voltage lags behind the line voltage. By calculating δ dynamically, the critical load voltage can be regulated to a predefined value, and ESs can operate in a related compensation mode. However, a single PR controller can only change the gain at a certain frequency and can only regulate ac signals. Compared with traditional frequency domain designs using gain and phase margins, the proposed

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method is easier and more convenient to use, although their final results may be similar. In the present work, i) s-domain transfer functions are obtained from system modeling, ii) Bode diagrams are used for controller design, iii) hardware diagrams and software flow charts are given to realize a digital phase locked loop (PLL), and iv) the system modeling and controller design are verified via simulation and experiments.

II. Operating Principles and Modeling of ESs

A. Existing δ Control of ESs

The topology of a single ES is shown in the dashed box in Fig. 1(a), which consists of a single-phase inverter and a low pass filter consisting of an inductor L and a capacitor C. v_G represents the unstable ac source; R_1 and L_1 are the line and source resistor and inductor, respectively; Z_2 is the critical load; and Z_3 is the non-critical load, which is designed with a large operating voltage range. A smart load is formed by an ES in series with Z_3.

The main principle of a single ES is to act as a power compensator that regulates the voltage of ac mains while passing fluctuations from unstable sources to non-critical loads [10].

The double loop control, as shown in Fig. 1(b), is used in [19], in which the outer loop is controlled with a PR controller with a sinusoidal signal as its reference. Although the frequency and amplitude can be set manually, the phase is not easy to be determined. The algorithm for controlling the phase is described in [19].

With the existing control, the critical load voltage can be regulated to match the predefined value while the ES operates in pure reactive compensation mode.

Although the waveforms of the critical load voltage appear sinusoidal, the values of the total harmonic distortion (THD) remain high when the input voltages become distorted to some extent. An example is shown in Fig. 1(c), in which the THD of the critical load voltage is 4.86% when the THD of the line voltage is 20%, which may still be improved. In addition, a single PR controller can only change the gain at a certain frequency. If other singular points exist within the system, additional PR controllers are needed to compensate for those points at different frequencies. Consequently, the amount of resources needed for the calculation in the digital signal processor (DSP) increases. Take for example the existing δ control, the switching frequency (f_s) is set to 5 kHz, and the algorithm consumes 90% of each switching period. An additional calculation of the added algorithm leads to a low f_s, which in turn reduces the quality of the output waveforms further.

B. Proposed Control of ESs

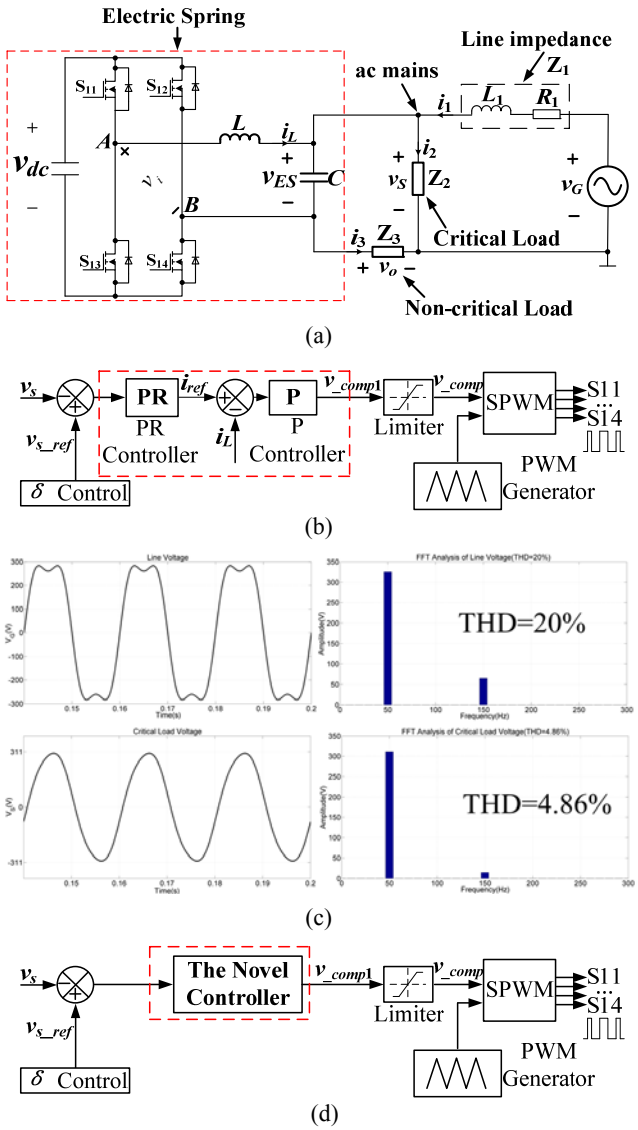


Fig. 1. Application and control of an ES in a single-phase power system. (a) Application of the ES. (b) Existing control. (c) THD analysis of the existing control. (d) Proposed control.

A new control diagram is depicted in Fig. 1(d). The new control is also based on δ control, as described in [19]. Figs. 1(b) and (d) differ because of the presence of the different controllers in the dashed lines. PR and P controllers used in the existing δ control are replaced with a novel controller, which can be regarded as a transfer function, in the proposed control. As explained later, the proposed controller is a common controller that can be used in ES systems and in other linear systems. Given that the proposed controller is designed by optimizing the frequency responses of systems, system modeling should be implemented first.

C. Modeling of ESs

As explained in [18], if dc bus dynamics are neglected, then linear time-invariant equations can be obtained as follows.

Applying KCL in Fig. 1(a) yields

$$i_3 = C\frac{dv_{ES}}{dt} - i_L \tag{1}$$

$$\frac{i_3 R_3 + v_{ES}}{R_2} + i_3 = i_1 \tag{2}$$

Applying KVL in Fig. 1(a) yields

$$L\frac{di_L}{dt} + v_{ES} = v_i \tag{3}$$

$$L_1\frac{di_1}{dt} + i_1 R_1 + v_{ES} + i_3 R_3 = v_G \tag{4}$$

where i_3 is the current flowing through the non-critical load, v_{ES} denotes the ES voltage, i_L is the current flowing through the filter L, i_{L1} is the input current on the ac side, v_G is the voltage of the ac source, v_i is the output voltage of the single-phase inverter, and v_S is the critical load voltage.

Solving (1) to (4) yields

$$\begin{cases} \dfrac{di_L}{dt} = -\dfrac{v_{ES}}{L} + \dfrac{v_i}{L} \\ \dfrac{dv_{ES}}{dt} = \dfrac{i_L}{C} - \dfrac{v_{ES}}{C(R_2+R_3)} + \dfrac{R_2 i_1}{C(R_2+R_3)} \\ \dfrac{di_1}{dt} = -\dfrac{R_2 v_{ES}}{L_1(R_2+R_3)} - \dfrac{(R_1R_2+R_2R_3+R_3R_1)i_1}{L_1(R_2+R_3)} + \dfrac{v_G}{L_1} \end{cases} \tag{5}$$

The dynamics of the ES system can be described by

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \tag{6}$$

where $x = \begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} = \begin{pmatrix} i_L \\ v_{ES} \\ i_1 \end{pmatrix}$, $u = \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} = \begin{pmatrix} v_G \\ v_i \end{pmatrix}$, $y = v_S$,

$$A = \begin{pmatrix} 0 & -\dfrac{1}{L} & 0 \\ \dfrac{1}{C} & -\dfrac{1}{C(R_2+R_3)} & -\dfrac{R_2}{C(R_2+R_3)} \\ 0 & -\dfrac{R_2}{L_1(R_2+R_3)} & -\dfrac{R_1R_2+R_2R_3+R_3R_1}{L_1(R_2+R_3)} \end{pmatrix},$$

$$B = \begin{pmatrix} 0 & \dfrac{1}{L} \\ 0 & 0 \\ \dfrac{1}{L_1} & 0 \end{pmatrix}, C = \begin{pmatrix} 0 & \dfrac{R_2}{R_2+R_3} & \dfrac{R_2R_3}{R_2+R_3} \end{pmatrix}, D = \begin{pmatrix} 0 & 0 \end{pmatrix}.$$

Control theory states that the open loop transfer function can be obtained through a matrix calculation.

$$G_{o1}(s) = \frac{Y(s)}{V_i(s)} = C(sI - A)^{-1}B + D \tag{7}$$

where $V_i(s)$ is the s-domain form of v_i and $Y(s)$ is the s-domain form of y, which is the same as the critical load voltage v_S.

TABLE I
PARAMETERS OF ES SYSTEM

Items	Values
Regulated mains voltage (V_S)	22 V
DC bus voltage (V_{dc})	36 V
Carrier amplitude(V_{tri})	1 V
Line resistance (R_1)	4 Ω
Line inductance (L_1)	52 mH
Critical load (R_2)	2,000 Ω
Non-critical load (R_3)	101.4 Ω
Inductance of low-pass filter (L)	3 mH
Capacitance of low-pass filter (C)	50 μF
Switching frequency (f_s)	5 kHz

As explained in [18], if the dc bus dynamics and inverter loss are disregarded, then the ES system can be regarded as a linear system. Therefore, the transfer function from $V_i(s)$ to the reference is linear, with the dc bus voltage defined as follows:

$$K_{PWM} = \frac{V_i(s)}{V_{ref}(s)} = \frac{V_{dc}}{V_{tri}} \tag{8}$$

where V_{dc} denotes the dc bus voltage of the inverter and V_{tri} is the carrier amplitude. Thus, the open loop transfer function from the reference to the output is expressed as

$$G_o(s) = K_{PWM}G_{o1}(s) \tag{9}$$

To ease the implementation of the system shown in Fig. 1 using the facilities available in the lab, we utilize three batteries with a rated voltage of 12 V in series and set V_S to 22 V. The parameters in Table I are chosen as examples for modeling and controller design, in which the critical load and non-critical load are pure resistors. Substituting the parameters in Table I into (9) yields

$$G_o(s) = \frac{2.284\times10^8 s + 1.757\times10^{10}}{s^3 + 1942s^2 + 7.033\times10^6 s + 1.289\times10^9} \tag{10}$$

III. CONTROLLER DESIGN

With the open loop transfer function obtained from dynamic modeling, the controller can be designed by optimizing $G_o(s)$ step by step. The control diagram of the closed loop is shown in Fig. 2, in which the proposed controller is defined as $G_x(s)$.

A. Modifications of Bode Diagrams

The Bode diagram of $G_o(s)$ is plotted first, as shown in Fig. 3(a). The phase margin (PM) of $G_o(s)$ is only 6.96°, leaving almost no margin for stability consideration.

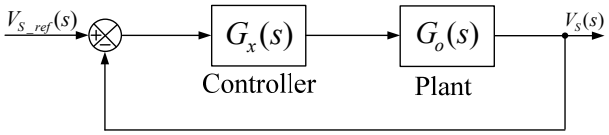


Fig. 2. Control loop of the critical load voltage.

Moreover, the maximum gain point is not at the fundamental frequency (e.g., 314 rad/s) but at 2,630 rad/s. The PM could be increased by employing several compensators. The design goals include increasing the PM of the compensated transfer function and raising the gain at 314 rad/s. In the present work, the characteristics of a minimum phase system are explored [20], and the desired PM is set to 90°, which indicates that the slope of the gain curve at the crossover frequency should be −20 dB/dec according to the theory of minimum phase system.

The next step is to compensate the resonant point at 2,630 rad/s and to increase the PM. Thus, $G_o(s)$ is multiplied by a compensator $G_{x1}(s)$, and the compensated transfer function is defined as $G_1(s)$, the Bode diagram of which is shown in Fig. 3(b). Two methods may be used to obtain $G_{x1}(s)$. One method is to find the poles and zeros of $G_o(s)$ and then try to compensate them. This method is adopted in this work. Another method is to use a trap filter to eliminate unexpected resonant points and then use lead links to achieve the characteristics of a minimum phase system.

$G_1(s)$ is expressed as

$$G_1(s) = G_{x1}(s)G_o(s) \tag{11}$$

where

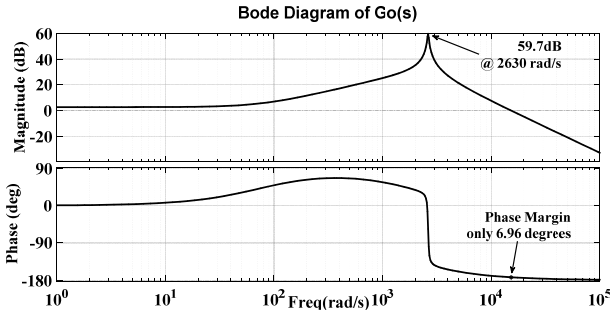
$$\begin{cases} G_{x1}(s) = k_{x1} \times \dfrac{500s^2 + 3.648\times10^4 s + 3.448\times10^9}{6.897\times10^6 s + 5.305\times10^8} \times G_d(s) \\ G_d(s) = \dfrac{1}{1\times10^{-6}s + 1} \\ k_{x1} = 1 \end{cases} \tag{12}$$

Fig. 3(b) shows that the PM of $G_1(s)$ reaches 95.5°. With the ES circuit operating at 314 rad/s, the next step is to raise the gain at 314 rad/s using a PR controller as one option. The compensated transfer function is defined as $G_2(s)$ and expressed as

$$G_2(s) = G_{x2}(s)G_1(s) \tag{13}$$

where $G_{x2}(s)$ is the s-domain transfer function of the PR controller, in which ω_0 is 100 π rad/s, ω_c is defined as $0.01\omega_0$, and k_p and k_r are 5 and 50, respectively. $G_{x2}(s)$ is expressed as

$$G_{x2}(s) = k_p + k_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{14}$$



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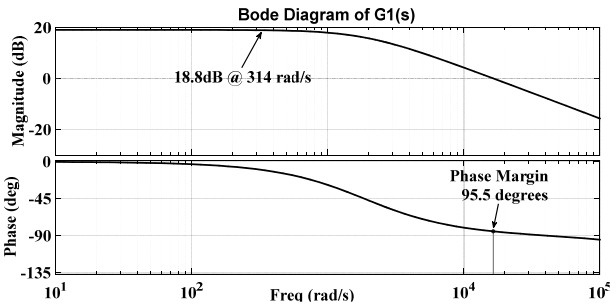

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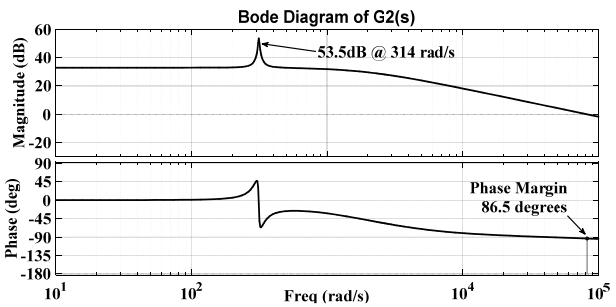

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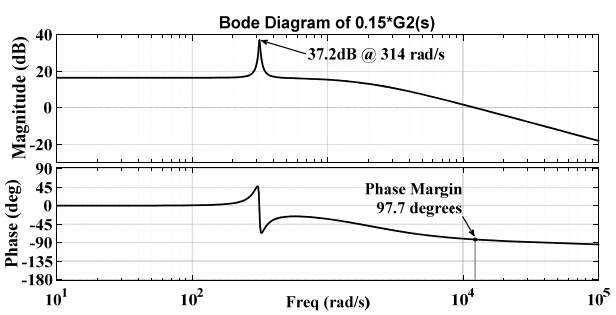


(d)

Fig. 3. Bode diagrams for controller design. (a) Bode diagram of G_o(s). (b) Bode diagram of G_1(s). (c) Bode diagram of G_2(s). (d) Bode diagram of 0.15 G_2(s).

With the design above, the final controller can be expressed as

$$\begin{aligned} G_x(s) &= G_{x1}(s)G_{x2}(s) \\ &= \frac{2500s^4 + 3.55\times10^5 s^3 + 1.75\times10^{10}s^2 + a_1 s + a_0}{6.897s^4 + 6.897\times10^6 s^3 + 5.746\times10^8 s^2 + b_1 s + b_0} \end{aligned} \tag{15}$$

$$\text{where } \begin{cases} a_1 = 1.21\times10^{12} \\ a_0 = 1.702\times10^{15} \\ b_1 = 6.841\times10^{11} \\ b_0 = 5.236\times10^{13} \end{cases} \quad (16)$$

The Bode diagram of $G_2(s)$ is plotted in Fig. 3(c). The final PM is 86.5°, which is significantly greater than the initial value of 6.96°. In addition, the gain at 314 rad/s is 53.5 dB, which is large enough and greater than that at any other frequency. Fig. 3(c) shows almost no phase shift at 314 rad/s with the PR controller. However, the cross-over frequency in Fig. 3(c) is about 80000 rad/s, which is so large that the operating frequency must be raised according to control theory. Several methods may be used to reduce cross-over frequencies. One option is to multiply $G_2(s)$ by a coefficient and to find a proper value, as shown in Fig. 3(d). If no compromise value is set, the parameter of the PR controller can be used again for this adjustment.

B. Design Summary

The design procedures are summarized as follows.

Step 1

The Bode diagrams of $G_o(s)$ are plotted and analyzed.

Step 2

The PM is checked and corrected to about 90° according to the theory of minimum phase systems.

Step 3

The gain at the desired frequency is raised to the maximum and to a value greater than that at other frequencies.

Step 4

The cross-over frequency of the magnitude–frequency curve is checked and determined to be about one-fifth to one-third of the pulse width modulation (PWM) frequency.

Step 5

Phase correction is performed at the desired frequency if needed.

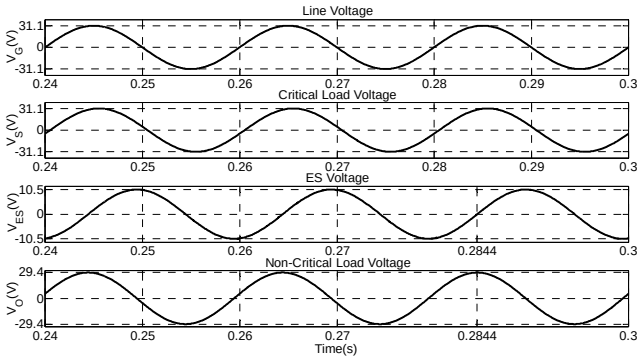
The proposed design can be likened to a tailor who sews clothes. Frequency responses at any point can be compensated by using the leading or lagging links of transfer functions. The design of the proposed controller is obviously different from the classical multistage leading/lagging design. With the proposed controller, the gains and phase angles at any frequency can be modified, and the final controller is the accumulation of the transfer function at each step. To optimize the control, three parameters, namely, k_{x1}, k_p, and k_r, can be adjusted. If the order of a certain numerator is greater that of the denominator in the controller, an additional pole far from the imaginary axis can be added (e.g., $G_d(s)$ in (12)). We must note that the design procedures can be exchanged during the practical design. For example, the total gain can be raised first, and the gain at the desired frequency can be raised to the maximum. The next step involves the stability consideration, and the final step may be phase correction and order adjustment of the final controller. As a result, the controllers designed may come in various forms, but the compensation directions and final effects are similar. The proposed control is based on system modeling and system parameters. Line impedance could be estimated according to [15].

C. Performance Studies

All the parameters in the simulations are the same as those in Table I. As shown in Fig. 4, the output voltages are regulated to match the predefined value regardless of the variation in V_G. Based on the parameters in Table I, the calculated V_G at which the ES operates in resistive mode is approximately 23.3 V. In addition, 22 and 24.2 V are set to show the results of the capacitive and inductive modes. As shown in Fig. 4(a), when V_G is 22 V, a zero-crossing point of the ES voltage is marked at 0.2844 s, which is also the moment when the non-critical load voltage reaches its maximum value and the ES operates in capacitive mode. The same analogy can be described for the inductive mode in Fig. 4(c). In Fig. 4(b), the ES voltage is nearly zero, and the non-critical load voltage is around 22 V, which indicates that the ES operates near resistive mode. To observe the effectiveness of the modeling, we also simulate the case at V_S = 220 V and V_G = 242 V, in which the dc bus is set to 360 V. The results are shown in Fig. 4(d). Two objectives are set for Fig. 4(d). One is to show that the output voltage can match the reference precisely, and the other is to show that the modeling and control algorithm developed for the scaled-down system are also valid for the standard system. The simulation results verify the effectiveness of the controller design. The phase control is also validated to ensure that the ES operates in pure reactive power compensation modes.

D. Harmonics Suppression Analysis

Harmonics suppression is also analyzed in this study. All the parameters in the simulation are the same as those in Part C. The simulation results are shown in Fig. 5. From 0.1 s to 0.7 s, the nominal value of V_G is set to 220 V. Harmonics are not added from 0.1 s to 0.3 s, the third-order harmonics with an amplitude of 44 V are added within 0.3 s to 0.5 s, and the third- and fifth-order harmonics with an amplitude of 44 V are added together within 0.5 s to 0.7 s. Fig. 5(a) shows that the critical load voltages remain sinusoidal from 0.1 s to 0.7 s regardless of line voltage distortion. The value of V_S in each period is equal to 220 V. The distortions in the line voltages are passed to the ES and the non-critical load. The fast Fourier transform (FFT) analysis of the line voltage and critical load voltage is shown in Fig. 5(b) and compared with that in Fig. 1(c). The THD of the critical load voltage is controlled to 0.13% when the THD of the line voltage is 20%.



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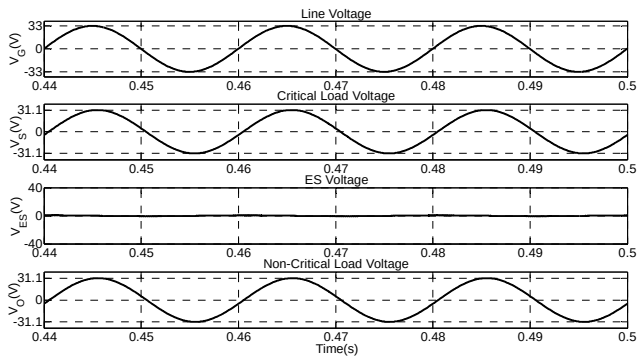

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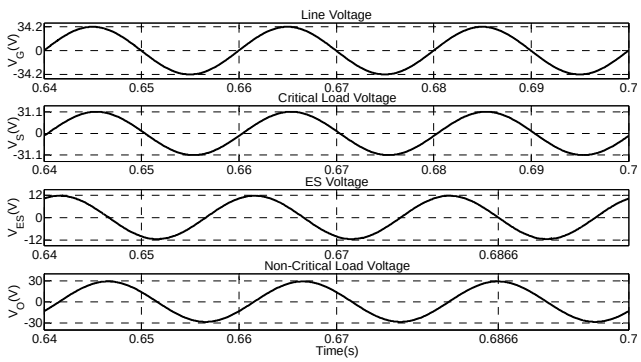

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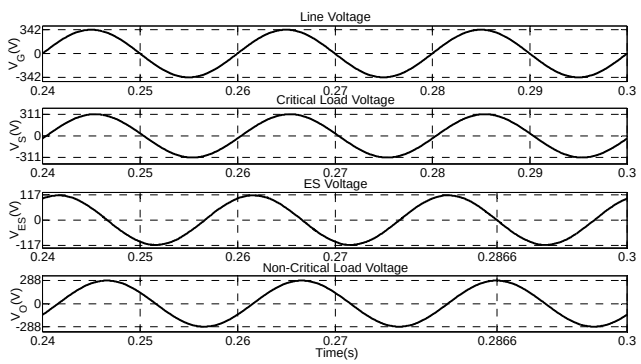
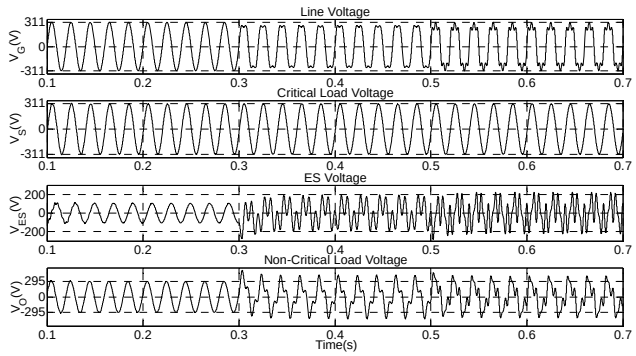
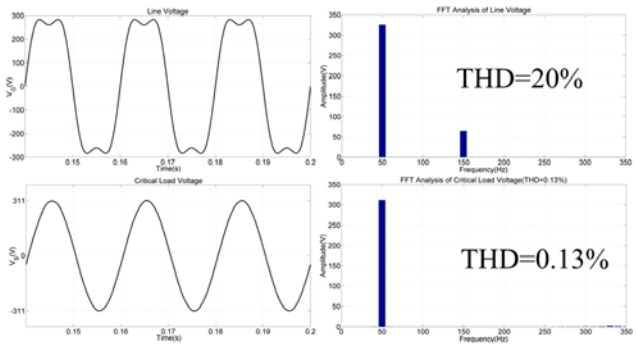


(d)

Fig. 4. Simulation results for reactive power compensations of the ES. Ch1 to Ch4: Line voltage, critical load voltage, ES voltage, and non-critical load voltage. (a) V_{S_ref} = 22 V and V_G = 22 V. (b) V_{S_ref} = 22 V and V_G = 23.3 V. (c) V_{S_ref} = 22 V and V_G = 24.2 V. (d) V_{S_ref} = 220 V and V_G = 242 V.



(a)



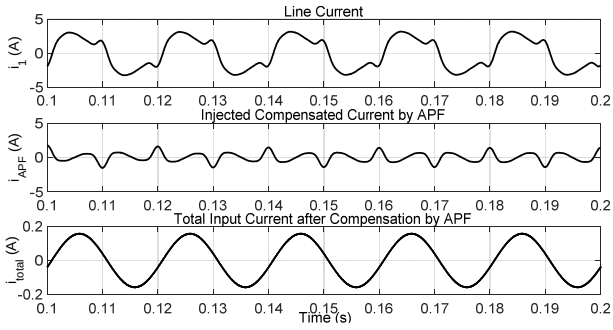
(b)

Fig. 5. Harmonics suppression of the proposed controller. (a) Simulation results for three different situations. (b) FFT analysis of line voltage and critical load voltage when third-order harmonics are introduced.

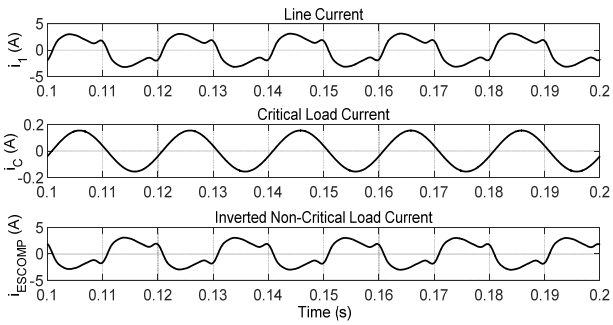
This result validates the superiority of the proposed controller over existing δ controllers in terms of harmonics suppression.

E. Comparison between Electric Spring and Active Power Filter

The difference between an ES and an active power filter (APF) can be summarized as follows. When harmonic components originate from the ac source, a typical APF detects a harmonic current and then tries to compensate for it to make the total input current clean (Fig. 6(a)). Generally, an ES can also take actions to compensate for such harmonic current and thereby ensure a clean current through the critical load while passing the harmonic components to the non-critical load (Fig. 6(b)). From this point of view, the ES and APF are similar. However, with the proposed controller, the ES no longer needs to detect and compensate for harmonic components like an APF. It simply needs to design the controller properly and set the cross-over frequency to a proper value. The ES also features unique functions that an APF does not have. For instance, when fluctuation occurs in an ac source, the ES can dynamically pass it to the non-critical load while ensuring a stable voltage on the critical load; this process is called input voltage control [10]. As shown in Fig. 5(a), when the value of the line voltage varies, the critical load voltage, which is the same as the point



(a)



(b)

Fig. 6. Comparison between an ES and an APF. (a) APF: Harmonics compensation. (b) ES: Harmonics compensation and voltage regulation for critical load.

of common coupling (PCC) voltage, is regulated to the predefined value (e.g., 220 V). On the contrary, an APF only deals with harmonic compensation [21] and does not focus on the regulation of PCC voltage and unpredictable power. With many ESs distributed, a micro-grid is laid out on many springs, and the PCC voltage is kept stable. ESs can be used in distributed applications, and their total performance is not influenced by a single failure.

IV. Experimental Setup Design

A. Hardware Design

To verify the proposed controller, we design the hardware setup on the platform of DSP28335, as shown in Fig. 7. As shown in Fig. 7, a single-phase full-bridge inverter is used to implement the ES. The output of the inverter is filtered with a low-pass LC filter to ensure that the ES voltage is sinusoidal.

A mechanical switch is added in the loop of the LC filter to observe the performance before and after the activation of the ES. Three batteries (12 V) in series are used as the dc source of the inverter. The dc bus capacitor C_1 is electrolytic. C_3 is ceramic and designed as a turn-off capacitor for switches. C_2 is added in parallel with the critical load to suppress high-frequency noises. In addition to the parameters in Table I, other parameters are provided in Table II. The critical load voltage, fluctuated ac voltage, and battery voltage are sensed through the sensor board, which also isolates the control circuit from the power circuit (Fig. 8(a)). The sensed signals

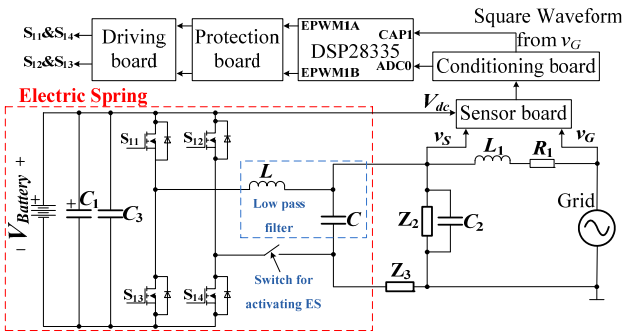
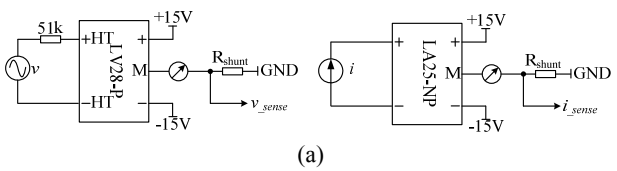


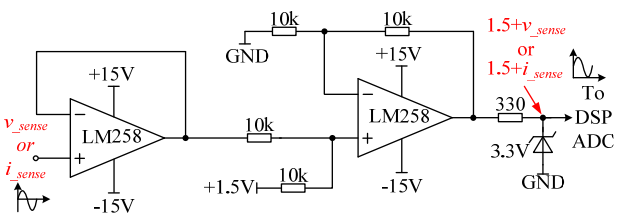
Fig. 7. Hardware implementation diagram of the ES.

TABLE II
Additional Parameters for the ES Experiments

Items	Values
DC bus capacitor (C_1)	2,200 μF/450 V
Decoupling capacitor (C_3)	10 nF/630 V
High-frequency filter capacitor (C_2)	10 nF/630 V
Current sensor	LV28-P
Voltage sensor	LA25-NP
Comparator	LM311
Amplifier	LM258
DC bus capacitor (C_1)	2,200 μF/450 V



(a)



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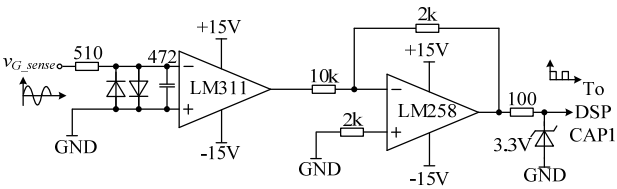
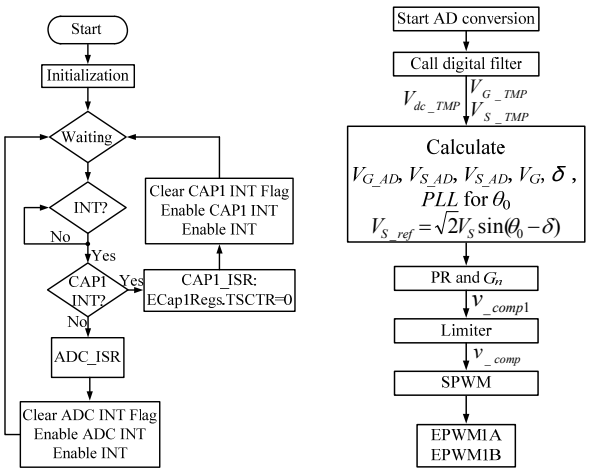
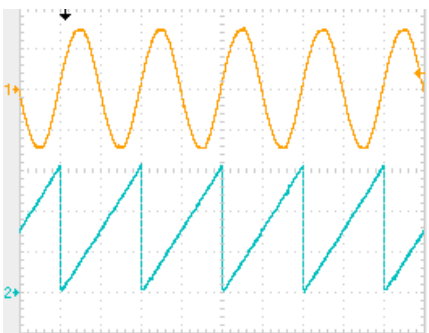


(c)

Fig. 8. Detailed hardware circuits. (a) Sensor circuits. (b) Conditioning circuit for AD conversion. (c) Circuit for generating square waveform.

are sent to the conditioning board, as shown in Fig. 8(b), in which all the three signals are converted to be positive so as to comply with the requirement of the DSP. As mentioned previously, a PLL function is realized by both hardware and





(c)

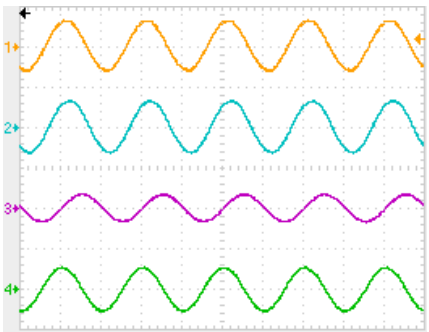
Fig. 9. Software flow charts and result of PLL. (a) Flow chart of the main program. (b) Flow chart of ADC_ISR. (c) Result of PLL, Ch1: line voltage 20 V/div, Ch2: phase of line voltage 2 rad/div.

software. The purpose of the hardware circuit for the PLL function is to generate a square waveform that synchronizes the line voltage and sends it to the CAP1 port of the DSP, as shown in Fig. 8(c).

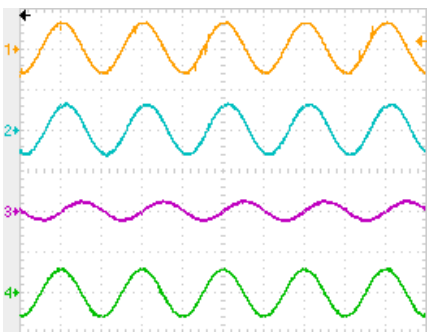
B. Software Design

The flow charts of the programs and the result of the PLL are shown in Fig. 9. The definition and initialization of the global parameters and subprograms are completed before the main function. Two types of interrupts are used. The CAP1 interrupt is used to capture the rising edge of the square waveform generated by the hardware shown in Fig. 8(c). The other interrupt is the ADC interrupt triggered by the enhanced PWM (EPWM) every 200 μs. All the algorithms, including that for the δ calculation, the digital controller, and sinusoidal PWM (SPWM), are realized in the subprogram named ADC_ISR.

In ADC_ISR, AD conversion is first initiated. The received signals are filtered with a digital filter and then transformed to their original values. The δ calculation function is initiated after the RMS voltage of v_G is calculated. Once the phase angle of v_G is detected, the predefined sinusoidal reference is generated.

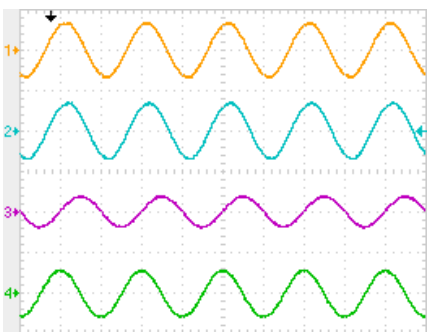


(a)

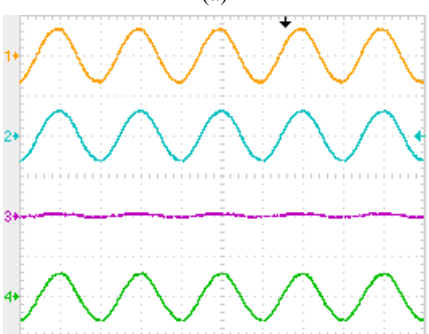


(b)

Fig. 10. Measured voltage waveforms @ V_G=22V. Ch1: line voltage, Ch2: critical load voltage, Ch3: ES voltage, Ch4: non-critical load voltage. (a) ES is not activated. (b) ES is activated and in capacitive mode. All the channels are 50 V/div, and the time base is 10 ms/div.

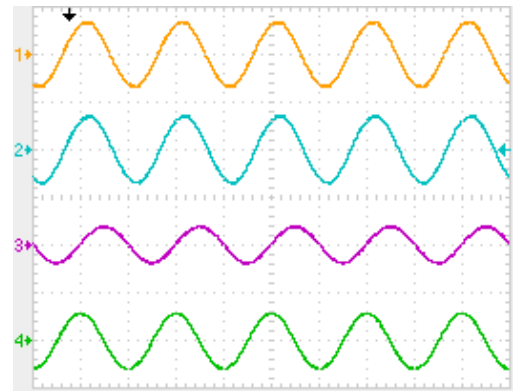


(a)

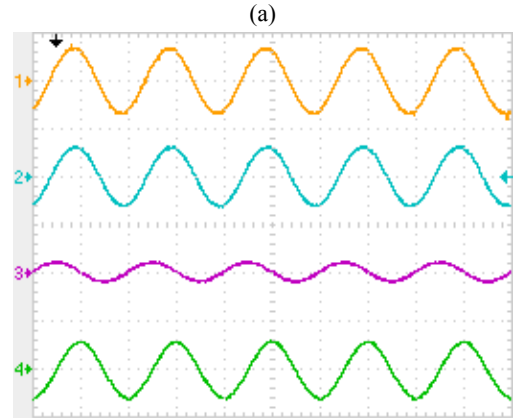


(b)

Fig. 11. Measured voltage waveforms @ V_G=23.3V. Ch1: line voltage, Ch2: critical load voltage, Ch3: ES voltage, Ch4: non-critical load voltage. (a) ES is not activated. (b) ES is activated and in resistive mode. All the channels are 50 V/div, and the time base is 10 ms/div.



(a)



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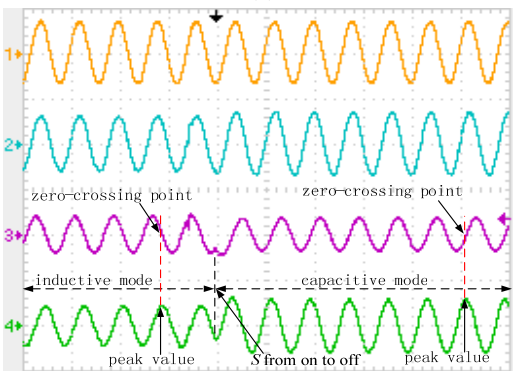

(c)

Fig. 12. Measured voltage waveforms @ V_G=24.2V. Ch1: line voltage, Ch2: critical load voltage, Ch3: ES voltage, Ch4: non-critical load voltage. (a) ES is not activated. (b) ES is activated and in inductive mode. (c) Transient response @ S from on to off. All the channels are 50 V/div. The time bases are 10 ms/div for (a) and (b) and 25 ms/div for (c).

Two complementary drive signals of EPWM1A and EPWM1B are generated with the algorithm of the proposed controller through a limiter and SPWM.

The PLL function in the software is realized as follows. Once the zero-crossing point of v_G occurs, the CAP1 interrupt is triggered, and the timer in the DSP is set to zero, which is read in every subprogram named ADC_ISR. The value is proportional to the phase angle of v_G, and the final value is defined as θ_0. Fig. 9(c) shows that θ_0 ranges from 0 to 2π and is thus consistent with the real-time waveform of v_G.

V. Results and Discussions

Experiments are conducted on the basis of the i) parameters in Tables I and II, ii) the hardware setup shown in Fig. 7, and iii) the software flow charts shown in Fig. 9. V_S is set to 22 V, and the calculated voltage at which the ES operates in resistive mode is about 23.3 V.

Fig. 10(a) shows the results when the switch in Fig. 7 is off while V_G is 21.9 V; the RMS values of the critical load, ES, and non-critical load voltages are 22.7, 12, and 18.9 V, respectively. With the introduction of the ES, the critical load voltage is regulated to 21.9 V. The ES and non-critical load voltages change to 7.15 and 20.8 V, respectively, as shown in Fig. 10(b), in which the ES voltage lags behind the current by 90° and the ES operates in capacitive mode. Such outcome is consistent with the simulation results shown in Fig. 4(a).

Fig. 11 presents the results when V_G=23.3 V and clearly shows significant changes. When the switch is off, the circuit operates under the sinusoidal steady state, and the current of the capacitor leads its voltage by 90°, as shown in Fig. 11(a). However, with the activation of the ES, the calculated θ at 23.3 V is around 0, and the ES voltage is also nearly 0; hence, the ES operates in resistive mode. As shown in Fig. 11(b), the RMS voltage values of the critical load, ES, and non-critical load voltages are 22, 1.41, and 20.7 V, respectively, and thus meet (20) in [19]. The ES voltage is not strictly 0 because the input voltage is coupled from the grid and its precise value is difficult to obtain, with its tolerance ranging from 0.1 V to 0.2 V. The results in Fig. 11(b) are also consistent with those in Fig. 4(b).

Figs. 12(a) and (b) show the results at V_G=24.2 V when the switch is off and on, respectively. The critical load voltage is regulated to about 21.8 V with the ES and to 25.1 V without the ES. The effectiveness of the ES can be obviously observed by comparing channels 3 and 4 in Fig. 12(a), in which the switch is off and the ES operates under the theory of the circuit at a sinusoidal steady state, and in Fig. 12(b), in which the switch is on and the ES operates in inductive mode. A transient response is also captured, as shown in Fig. 12(c). The ES current lags behind the ES voltage by 90° when the switch is on. Hence, the ES is activated and operates in inductive mode. However, when the switch is off, the ES current leads its voltage by 90°. Hence, the ES is deactivated and operates under the sinusoidal steady state.

VI. Conclusion

The modeling and controller design of a single-phase power system using a single-phase ES are analyzed. Mathematical derivations and equations supporting the dynamic modeling are given first. The open loop transfer function in the s-domain from the reference to the output is hence deduced. A novel controller is proposed through modifications on the Bode diagrams obtained from the

voltage loop to regulate the critical load voltage; the phase angle is based on a recently proposed δ control. Frequency responses at any point can be modified by using the leading or lagging links. Such modification is a new control strategy for ESs and other linear systems. The performance and harmonics suppression of the proposed controller at steady state are analyzed and simulated. The critical load voltage can be regulated to match the predefined value precisely even with input voltage distortion. The hardware design with detailed circuits and the flow charts of the software are presented. The critical technology of digital PLL is realized through the combined use of hardware and software. The ES system is implemented on the DSP platform. Simulations are conducted, and the results are in good agreement with the theoretical analysis. Moreover, experiments on the prototype are carried out, and the results confirm the effectiveness of the controller design of the ES system.

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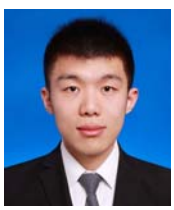

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