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A Level Dependent Source Concoction Multilevel Inverter Topology with a Reduced Number of Power Switches

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Abstract

Multilevel inverters (MLIs) have been preferred over conventional two-level inverters due to their inherent properties such as reduced harmonic distortion, lower electromagnetic interference, minimal common mode voltage, ability to synthesize medium/high voltage from low voltage sources, etc. On the other hand, they suffer from an increased number of switching devices, complex gate pulse generation, etc. This paper develops an ingenious symmetrical MLI topology, which consumes lesser component count. The proposed level dependent sources concoction multilevel inverter (LDSCMLI) is basically a multilevel dc link MLI (MLDCMLI), which first synthesizes a stepped dc link voltage using a sources concoction module and then realizes the ac waveform through a conventional H-bridge. Seven level and eleven level versions of the proposed topology are simulated in MATLAB r2010b and prototypes are constructed to validate the performance. The proposed topology requires lesser components compared to recent component reduced MLI topologies and the classical topologies. In addition, it requires fewer carrier signals and gate driver circuits.

Key words: Component count, Level dependent sources concoction multilevel inverter (LDSCMLI), Phase disposition pulse width modulation

I. INTRODUCTION

Multilevel inverters (MLIs) are recommended for high power, medium voltage applications due to their ability to synthesize a staircase waveform from several isolated dc sources, capacitor banks or renewable energy sources. The primary features of a typical MLI include a high quality output voltage (near to a sinusoid wave), low harmonic distortion, lower electromagnetic interference and low voltage stress across the switches [1], [2]. The classical MLI topologies are the cascaded H-Bridge (CHB), diode clamped and flying capacitor types [3]-[5]. The CHB is composed of a series connection of several isolated H-Bridge inverters to generate a stepped output voltage with a desired amplitude and frequency. The diode clamped and flying capacitor MLIs make use of a single dc source with capacitor banks to synthesize an output voltage through clamping diodes and flying capacitors. However, these topologies need more number of power components with different blocking voltages and at an increased number of levels. In addition, they suffer due to higher implementation costs and control complexity. Topologies with a higher component count not only increases the size, but also increases the complexity through larger gate drives and tough timing/sequence management. This is the motivation to focus on developing converter topologies with reduced component counts and suitable modulation strategies [6]-[9]. Depending on the voltage magnitudes of separate dc sources (SDCs), the MLIs are classified into symmetric and asymmetric topologies [10]-[12]. The magnitudes of the SDCs are equal in symmetric topologies while in the asymmetric topologies they are unequal. The symmetric topologies have modularity and other related merits. On the other hand, the asymmetric topologies require devices with different blocking voltages and do not have modularity in their structure.

A class of MLIs based on a multilevel dc link (MLDCL)

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together with an H-bridge inverter has been suggested to reduce the number of switches, clamping diodes and capacitors [11]. The MLDCL has been endowed utilized to acquire a dc voltage with the shape of a staircase, approximating the rectified shape of the desired wave. MLDCL converters have been seen to significantly reduce the switch count and the number of gate drivers as the number of voltage levels increases. Another variety of multilevel dc-link inverter (MLDCLI), referred to as the series parallel switched multilevel dc-link inverter (SPSMLDCLI), has been developed with the primary objective of arriving at a reduced component count [12]. It has been developed to produce the shape of a staircase output voltage approximating the rectified shape of a desired sinusoidal wave, either with or without pulse width modulation (PWM) by switching the dc sources in series/parallel. A few more symmetric MLI structures have been recommended, which reduce the number of switches for higher voltage levels [13], [14]. The topology mentioned in [13] is based on a mixture of cascaded basic cells and the one presented in [14] is derived from non-isolated dc sources with a reduced number of power switches. On the other hand, these topologies offer marginal improvements in the reduction of switches. A modular MLI topology has been introduced with advantages such as simplicity, modularity and redundancy with respect to the CHB-based inverter [15]. However, this topology offers a higher number of components and gate driver circuits. A MLI topology comprised of a cascaded connection of cells containing two voltage sources with six switches and a H-bridge inverter has been developed [16]. The presented topology maximizes the number of levels using a few cells. Numerous topologies have been introduced with the primary characteristic of lowering the number of switches [17], [18]. The switch peak inverse voltages (PIVs) of the switches in the presented topologies are greater than that of the basic CHB MLI.

Having selected a topology for user convenience, the next step is developing a PWM strategy and pulse separation logic. A discussion of the MLI topology will only be complete when a suitable switching strategy is devised. Generally the PWM strategies of a MLI are logical extensions of the strategies available for two level voltage source inverters (VSIs). In 1983, P. M. Bhagwat and V. R. Stefanovi presented a generalized control structure for multilevel PWM inverter, which stands as the foundation of the PWM techniques for MLIs [19]. In 1992, G. Carrara et al. proposed a multilevel PWM method and proved its superiority by the lowest harmonic distortion when compared with the other PWM methods [20]. In 1999, L. M. Tolbert et al. found that the implementation of the existing control strategies for a diode-clamped inverter affects the switch utilization, which in turn increases the losses. In 2000, B. P. Mcgrath and D. G. Holmes demonstrated an analytical solution for PWM techniques and also determined that the harmonic components produced by the alternative phase opposition disposition (APOD) technique in diode clamped inverters is the same as that of the phase shifted carrier (PSC) technique in cascaded inverters [21]. In 2001, Calais. M. et al. confirmed a number of multi-carrier PWM methods [22]. A MLI modulation strategy suitable for stand-alone PV applications has been suggested, which produces a much higher fundamental output compared to conventional SPWM without any pulse dropping [23]. The employed phase-shifted carriers produce a harmonically superior SPWM signal, reduce THD and improve conversion efficiency. A MLDCL-based topology along with the natural sampled PWM scheme has been presented [24]. A boost switched capacitor MLI has been tested for different multi carrier based PWM techniques [25]. Single carrier-based PWM strategies have been tried for nine level inverters [26]-[27]. A detailed study has revealed the presence of even harmonics in the output of a few of the multi-carrier options because of the absence of half wave symmetry in the phase switching function [28].

This paper proposes a new level dependent sources concoction MLI (LDSCMLI) with a view to reduce the number of switching devices and gate drivers. It is basically a symmetrical multilevel dc link MLI (MLDCMLI) topology, which has modules viz. a sources concoction module and a H-bridge module. The presented simulation and experimental results confirm the validity of the proposed inverter. Phase disposition pulse width modulation (PD-PWM) is employed both in the MATLAB simulation and in the laboratory corroboration.

II. PROPOSED LDSCMLI TOPOLOGY

The LDSCMLI topology facilitates the connection of voltage sources in series/parallel combination by switching the appropriate devices to produce a desired level of output voltage. The sources to be included as well as their concoction fashion (either series or parallel) are dependent on the present level of the output. It uses the same number of voltage sources as that of CHBMLI for any number of voltage levels but at a reduced switch count. Fig. 1 shows the generalized LDSCMLI topology along with isolated dc voltage sources (V_1-V_n) integrated with a H-Bridge inverter. The two integral modules of the LDSCMLI are clearly indicated in the figure. The dc sources are available both in the vertical and horizontal arms of the LDSCMLI, and there is a series switch with every one of them. The source paralleling switches S_1, S_3, S_5, S_7 etc., help in paralleling the sources in the adjoining vertical arms V_2-V_4, V_4-V_6, V_6-V_8, etc. The arm bridging switches S_2', S_4', S_6', etc., cascade the sources in the adjoining vertical arms and help in making higher voltage levels. The source cascading switches S_2, S_4,

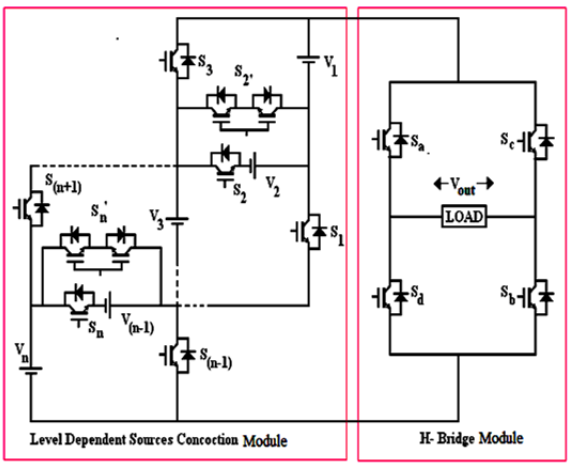

Fig. 1. Proposed LDSCMLI Topology.

S_6, etc., connect the horizontal arm sources with the vertical arm sources to synthesize highest levels. The switches S_a and S_c are complementary to the switches S_d and S_b, and they perform polarity reversal in the H-bridge inverter.

Figs 2 to 4 illustrate the operating modes of a seven level LDSCMLI for producing the positive/negative cycles of the output voltage on the load side. As seen in Fig. 2, the switches (S_1 and S_3) are fired to connect the voltage sources, V_1 and V_3 in parallel to produce the first level V_{dc} (V_1=V_2=V_{dc}) in the output voltage. Source V_2 is not included in this mode. In the next mode, shown in Fig. 3, sources V_1 and V_3 are made in series to have an output of $2V_{dc}$. V_2 is not used in this mode either. In Fig. 4, the switch S_2 connects all three of the voltage sources V_1, V_2 and V_3 in series to produce an additive level $3V_{dc}$ in the output voltage. The switches used in a typical LDSCMLI have to withstand different voltages. For the seventh level inverter, the switches (S_1 and S_3) have to block V_{dc} and the switch (S_2) has to block $2V_{dc}$. Meanwhile the switches (S_a, S_b, S_c and S_d) in the H-bridge inverter have to block $3V_{dc}$. In addition, the devices in the H-bridge inverter have to block the full dc-link voltages. Therefore, devices with higher blocking voltages need to be selected. The proposed MLI requires a reduced number of switching components in the active current conduction path k_c and just half the number of carrier waves in the PWM generation when compared to the cascaded H-bridge inverter. It is worthwhile to note that an increased number of active devices in the conduction path leads to a larger voltage drop (hence a reduced output voltage) and increased conduction losses (the domination category of losses in power devices).

Being a symmetrical MLI topology, all the magnitudes of all the dc sources are equal to V_{dc}. The maximum output voltage and the number of levels are equal to 'nV_{dc}' and (2n+1) respectively, where 'n' is the number of dc sources. The entries in Table I represent the requirements of the switches, dc sources, gate drive drivers, etc. in the proposed

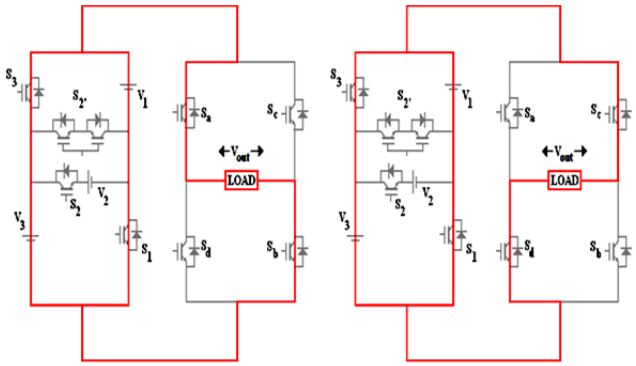

Fig. 2. Mode 1 Voltage sources ($V_1$and V_3) operating in Parallel.

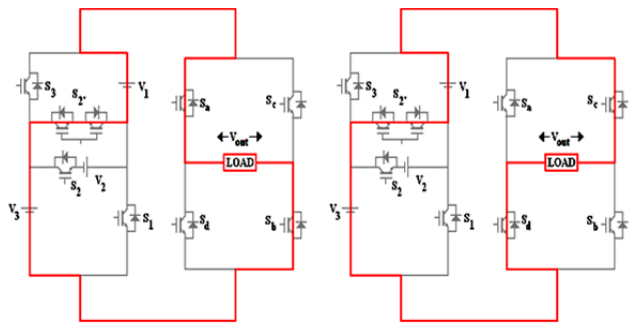

Fig. 3. Mode 2 Voltage sources ($V_1$and V_3) operating in series.

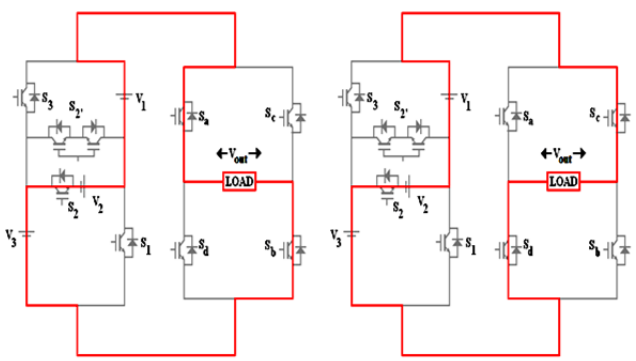

Fig. 4. Mode 3-voltage sources (V1, V_2 and V_3) operating in series.

topology and in other competing topologies (for 'm' levels). The superiority of the proposed topology is demonstrated in terms of the component count. In an identical condition, the proposed symmetric topology is compared with the symmetric CHBMLI, the MLDCLI and the SPSMLDCLI. The SPSMLDCLI uses series and parallel connections of the dc voltage sources.

At a seven level output, the three classical topologies (CHBMLI, diode clamped MLI and flying capacitor MLI) and the SPSMLDCLI require 12 and 10 devices respectively. Meanwhile the proposed LDSCMLI topology requires only 8 devices. The proposed symmetric MLI uses a much lower number of switches in comparison with the other topologies.

From the previous discussions, the benefits of the proposed configuration can be easily understood. Fig. 5

TABLE I
COMPONENT COMPARISON OF MLI TOPOLOGIES

Topology	Main switches	Main diodes	Gate drivers	Clamping diodes	Flying capacitors	Dc-link capacitors	Total Component Count
CHBMLI	2(m-1)	2(m-1)	2(m-1)	-	-	(m-1)2	13(m-1)/2
Diode clamped	2(m-1)	2(m-1)	2(m-1)	2(m-3)	-	(m-1/)2	(17m-25)/2
Capacitor clamped	2(m-1)	2(m-1)	2(m-1)	-	(m-3)	(m-1/)2	(15m-19)/2
Cascaded Half-Bridge MLDCLI	(m-1)+4	(m-1)+4	(m-1)+4	-	-	(m-1)2	(7(m-1)+24)/2
Diode Clamped MLDCLI	(m-1)+4	(m-1)+4	(m-1)+4	(m-3)	-	(m-1/)2	9(m+1)/2
Capacitor Clamped MLDCLI	(m-1)+4	(m-1)+4	(m-1)+4	-	(m-3)/2	(m-1/)2	(8m+14)/2
SPSMLDCLI	(3m-1)/2	(3m-1)/2	(3m-1)/2	1	-	(m-1/)2	(5m-1)
Proposed	(m+1)	(m+1)	(m+1)	-	-	(m-1/)2	(7m+5)/2

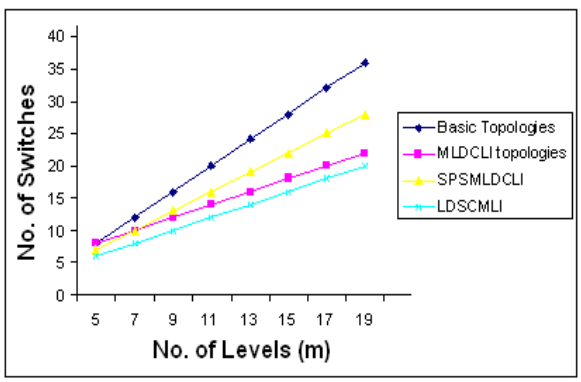

Fig. 5 Comparison of required number of switches.

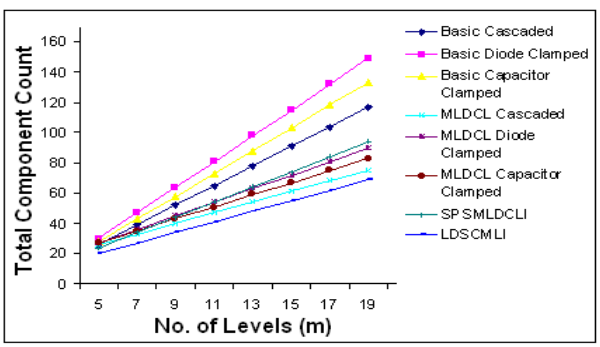

Fig. 6. Comparison of total component count.

compares the number of active switches required for the basic configurations (cascaded, diode-clamped and capacitor clamped), the MLDCL and the proposed LDSCMLI inverters. All three of the classical topologies require the same number of main power switches. Similarly, all of the MLDCL configurations do not differ in this count. When the number of levels (m) increases, the number of active switches also increases as 2(m-1) and ((m-1) +4) for the basic configurations and the MLDCL configurations while the LDSMLI follows the expression (m+1). Fig. 6 summarizes the total component count. The proposed LDSCMLI configuration reduces the total component count by 42% from the monster configuration (basic diode clamped) and

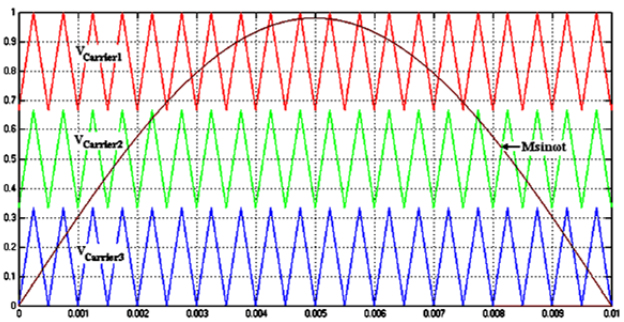

Fig. 7. PD-PWM technique.

18% from the diminutive circuit (cascaded-MLDCL) at a seven level output.

III. APPROPRIATE SWITCHING SCHEME

To implement any single variant of the sub-harmonic/multicarrier PWM (SHPWM/MCPWM), the proposed topology at a 'm' level output requires (m-1) triangular carriers of the same amplitude and frequency. In addition, they are disposed vertically in phase with each other. The switching signals required to fire the switching devices are obtained by direct comparisons between the triangular carriers (V_{cr1}, V_{cr2} and V_{cr3}) and the modulating reference sine signal ($(M \times \sin wt)$, as depicted in Fig. 7, where 'M' is the modulation index. Fig. 8 illustrates the analog circuitry for implementing the PD-PWM for a seven level output. Table II shows the logical functions to tailor exact gate pulses to the devices in the sources concoction module while the gate pulses of the H-bridge devices are basic square wave pulses (fundamental switching).

IV. SIMULATION RESULTS

MATLAB-Simulink r2010b software is used for the simulations in this paper. The simulation parameters are: $V_1=V_2=V_3= V_{dc}=100V$ and the switching frequency is 2 kHz. An inductive load is considered with the values R= 150Ω and

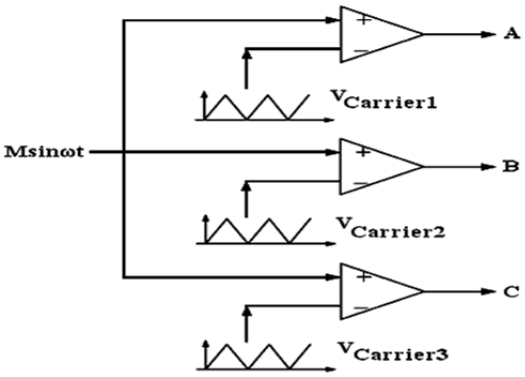

Fig. 8. PD-PWM scheme for single phase seven level inverter.

TABLE II
LOGICAL FUNCTIONS TO GENERATE GATES PULSES FROM BASIC DUTY CYCLE FUNCTIONS

Power switches	Logical function
S_1, S_3	A **xor** B
S_2	C
S_2'	B **xor** C

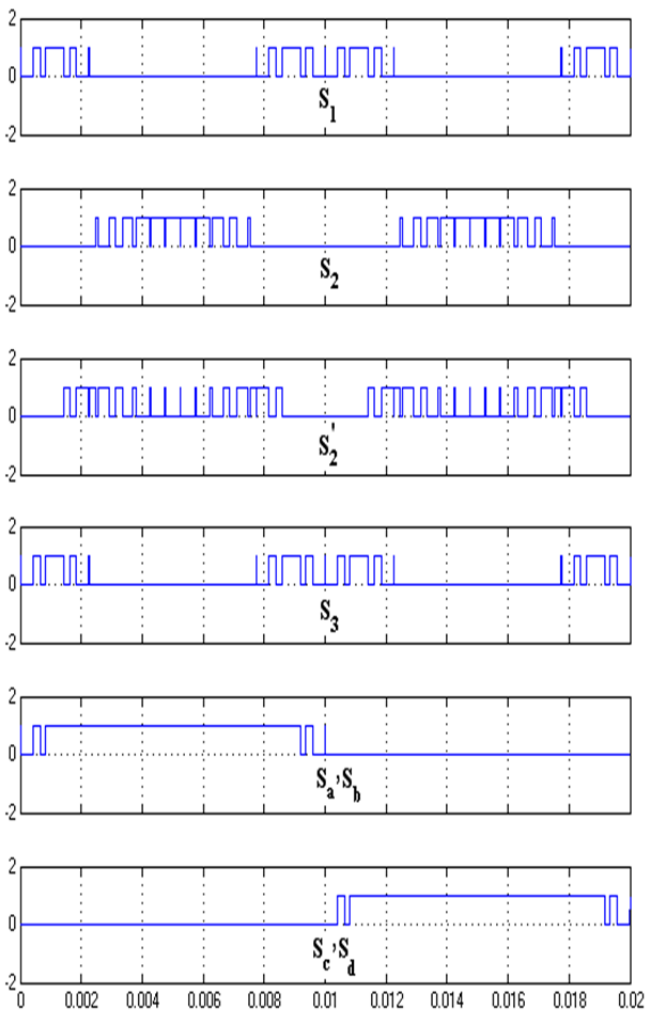

Fig. 9. Typical gate pulse patterns.

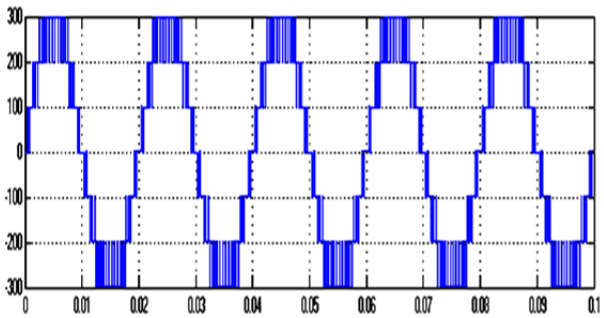

Fig. 10. Output voltage waveform.

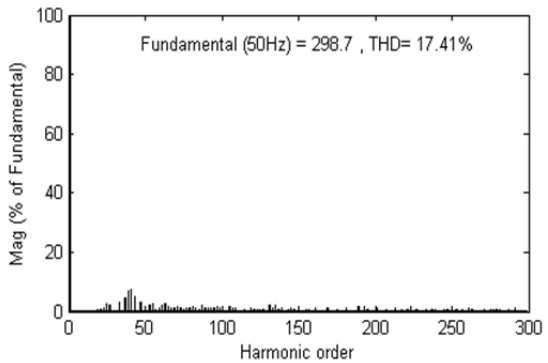

Fig. 11. Output voltage Spectrum.

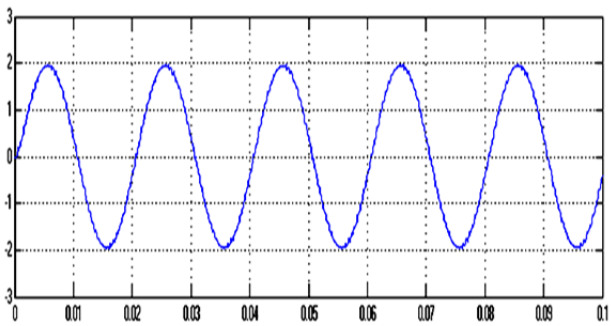

Fig. 12. Load current.

L= 100mH. Typical gate pulses obtained in the simulation are portrayed in Fig. 9. Meanwhile, Fig. 10 and Fig. 11 depict the output voltage waveform and its harmonic spectrum respectively for M=1. The inductive load current for a single phase seven level inverter is portrayed in Fig. 12, and it traces a nearly sinusoidal shape due to the filtering action of the inductive load and the supportive carrier frequency. Fig. 13 and Fig. 14 depict the chart for variations of the fundamental component of the output voltage (V_{o1}) with M and for variations of the THD with V_{o1}. It is seen that V_{o1} increases linearly with M (the THD decreases).

V. EXPERIMENTAL INVESTIGATION

The prototype LDSCMLI shown in Fig. 15 is constituted using a power IGBT (BUP306D) and tested for the load specifications used in simulation study to validate the simulated performance. The PD-PWM is implemented in a

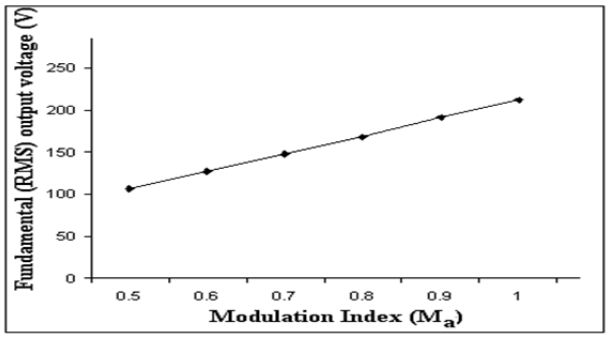

Fig. 13. Variation of V_{o1} with M.

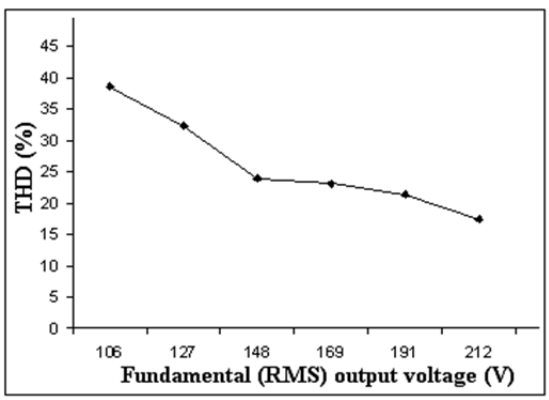

Fig. 14. V_{o1} Versus THD.

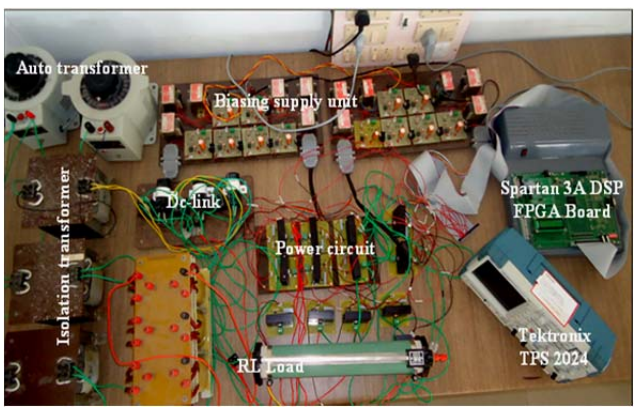

Fig. 15. Prototype of proposed single phase seven level inverter.

Xilinx Spartan 3E-500 FG320 FPGA board. The PD-PWM architecture is designed using the VHDL language. The functional simulation of the architecture is carried out using the Modelsim 6.3 tool. A Xilinx ISE 13.2 synthesize tool is employed for the Register Transfer Level (RTL) verification and implementation. Then, the designed architecture is configured to the Xilinx Spartan 3E-500 FG320 FPGA device. The output voltage waveform, the harmonic spectrum and the load current waveform for a seven level output (at M=1) are shown in Fig. 16, Fig. 17 and Fig. 18, respectively. The experimental results are in agreement with the simulation results and highlight the practical applicability of the proposed MLI topology. The experimental investigation is

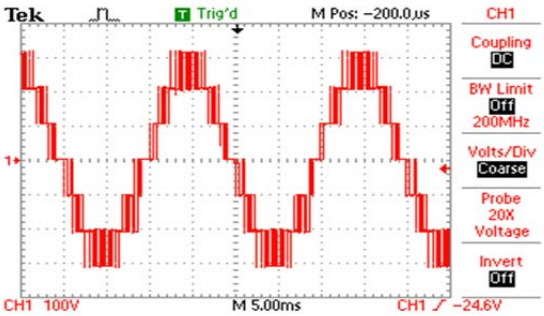

Fig. 16. Output voltage waveform-experimental.

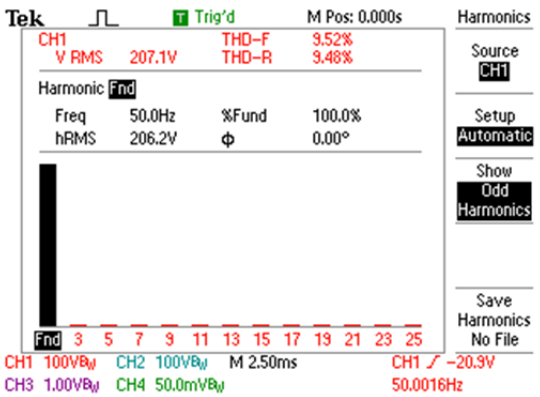

Fig. 17. Output voltage harmonic spectrum – experimental.

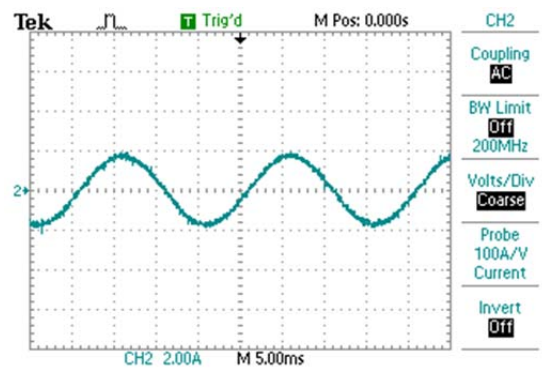

Fig. 18. Inductive load current waveform – experimental.

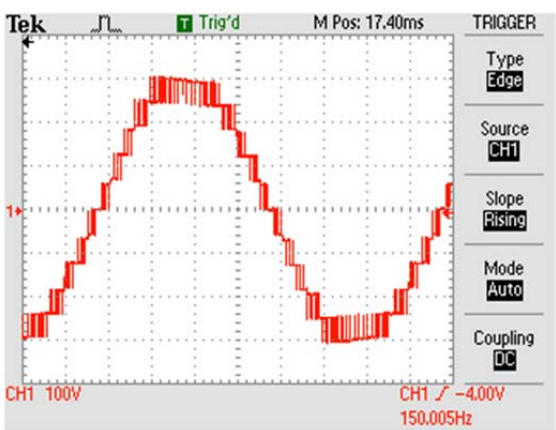

Fig. 19. Output voltage waveform- 11 level.

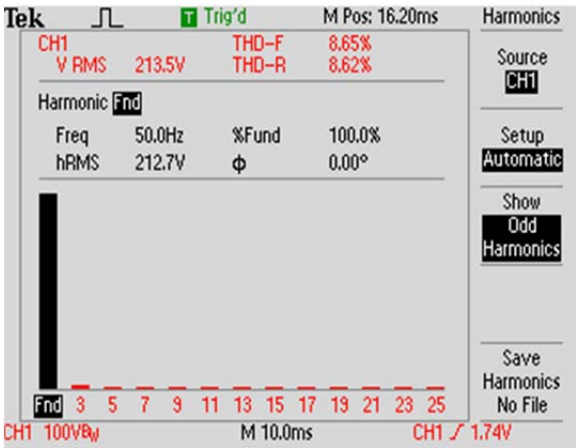

Fig. 20. Output voltage harmonic spectrum - 11 level.

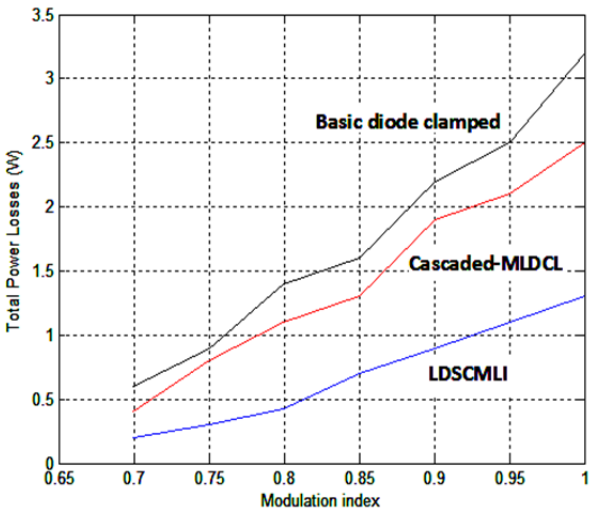

Fig. 21. Total power losses (W) versus M for proposed, monster and diminutive topologies- for seven level.

extended for higher level outputs as well. The output voltage waveform and harmonic spectrum for an 11 level output are shown in Fig. 19 and Fig. 20, respectively. The losses are estimated for the proposed topology and others at different M values and compared in Fig. 21.

VI. Conclusions

A new symmetrical MLI structure using isolated voltage sources has been developed. The topology has been constituted using a relatively small number of semiconductor devices compared to the existing MLI topologies. The proposed configuration has been designed to obtain a desired number of voltage levels from the same number of voltage sources and achieve a higher quality output voltage spectrum. The number of operating switches in each conduction sequence has been drastically reduced to minimize conduction losses and to obtain a higher efficiency. MATLAB simulation and Xilinx Spartan 3E-500 FG320 FPGA supported testing have also been provided. The proposed topology is suitable for photovoltaic, FACTS and UPS applications.

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