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Short-circuit Protection for the Series-Connected Switches in High Voltage Applications

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Abstract

This paper presents the development of a short-circuit protection mechanism on a high voltage switch (HVS) board which is built by a series connection of semiconductor switches. The HVS board is able to quickly detect and limit the peak fault current before the signal board triggers off a gate signal. Voltage clamping techniques are used to safely turn off the short-circuit current and to prevent overvoltage of the series-connected switches. The selection method of the main devices and the development of the HVS board are described in detail. Experimental results have demonstrated that the HVS board is capable of withstanding a short-circuit current at a rated voltage of 10kV without a di/dt slowing down inductor. The corresponding short-circuit current is restricted to 125 A within 100 ns and can safely turn off within 120 ns.

Key words: Arc current limiting, HVS board, Series-connected switches, Short-circuit current, Transient voltage

I. INTRODUCTION

Recently, the utilization of series-connected semiconductor switches has rapidly increased for pulsed power modulators which produces a high voltage (HV) dc pulse to accelerate electron or ion to high energy for water treatment or medical accelerators [1]-[6]. Various drive systems have been developed and applied to drive the semiconductor switches with a high repetitive rate as well as a high voltage condition. A problem commonly encountered during the operation of a modulator is the occurrence of an arc which requires the rapid removal of the storage energy from a load by turning off the HVS. Existing drive systems are generally equipped with a protection circuit on a signal board to detect short-circuits by Pearson CT and Hall CT [2], [3]. However, there is an unavoidable delay time of several hundred nanoseconds caused by the detection, comparison and logic control circuits. Due to the high voltage and low inductance characteristics of pulse power modulators, short-circuit faults result in a steep rise and an extremely high peak value of the fault current, which can exceed 15 kA with a rate of rise that is greater than 10 kA/μs during an arc [5]. These unique conditions cause IGBTs to burst into oscillation with an uncontrollable high peak current and eventually destroy the gate [6]. The fundamental reasons for IGBT failures in short-circuits, which are an excess of the thermal limit and/or breakdown voltage, static and dynamic latch-up, are presented in [7].

A lot of effort has already been spent on the investigation of short-circuit protection schemes for semiconductor switches. In [2], an inductor is connected in series to a load to slow down the di/dt rate of a fault current. Hence, the peak value can be limited to a safe value before the reaction of the signal board. However, the use of a HV inductor, a HV diode and a HV resistor for discharging results in a bulky and costly HVS tank. In [8], a desaturation technique uses a sense diode to detect collector-emitter voltage under short-circuit faults. When the current rises above the knee of the output characteristics, the device pulls out of the saturation and the increased collector-emitter voltage can trigger a protection circuit. A fast protection function for IGBT modules was recently proposed by an evaluation of the fault current value through the di/dt feedback signal which is based on the voltage across the parasitic inductance between the Kelvin emitter and the power emitter of an IGBT module [9], [10]. In [11], a fault current detection using a printed circuit board Rogowski coil is used in a gate driver to protect 4.5 kV press-pack IGBTs operated at 4 kA of pulse current. Detection circuits using the turn-on switching characteristic to protect IGBTs under short-circuit failures are represented in [12]-[15]. These scheme are based on the gate voltage

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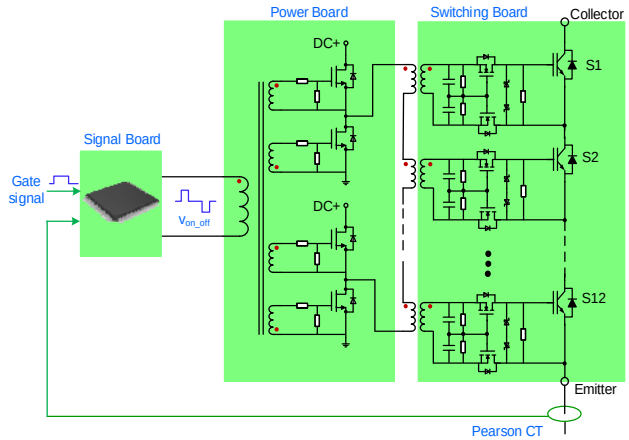


Fig. 1. A block diagram of a HVS system.

TABLE I
FAULT DETECTION METHODS AND ASSOCIATED FAILURE DETECTION TIME

Fault Detection Technique	Fault Detection Time
Using an additional inductor [2]	< 1.5 [μs]
Measurement of IGBT's voltage [8]	< 2 [μs]
Measurement of di/dt feedback [9]	< 1.1 [μs]
Using PCB Rogowski [11]	< 13.5 [μs]
Using turn-on characteristic [14]	< 3 [μs]

behavior at the turn-on transient of IGBTs, and to obtain an early detection failure. Table I summarizes these fault detection methods and their associated failure detection times. Voltage transients during a short-circuit turn-off are protected by an active clamping circuit in [16]. In [17], the effects of a self-turn-off mechanism, asymmetrical gate wiring between paralleled IGBT chips and semiconductor physics are considered to enhance the short-circuit capability of high-voltage IGBTs rated at 4.5 kV.

In this paper, a short-circuit protection mechanism using arc current limiting and a safe turn-off circuit is developed to protect series-connected switches against short-circuit faults. The arc current limiting circuit is designed to make a gate voltage drop when a high di/dt of fault current flows through the sensing resistors. Hence, the switching board can limit the fault current before the controller turns the gate off. In addition, voltage clamping techniques are also applied to prevent overvoltage at a short-circuit turn-off. Firstly, the principle operation of a typical HVS drive system is introduced in section II. Secondly, short-circuit protection schemes for a HVS board are analyzed in section III. Then, a test setup and a development process are described in sections IV and V, respectively. Finally, experimental results are illustrated in section VI.

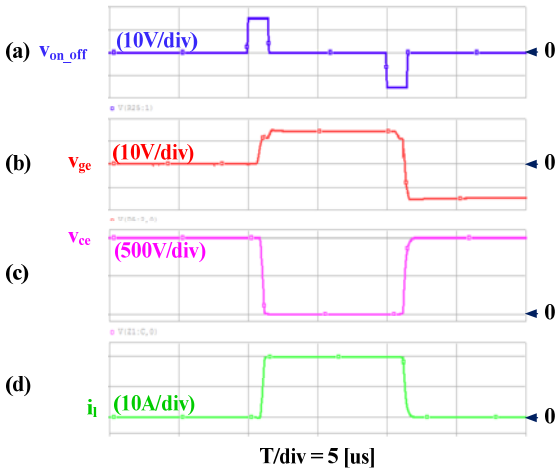


Fig. 2. Simulation results of HVS driver system (a) signal board output v_{on_off}. (b) Gate voltage v_{ge}, (c) Switch voltage v_{ce}, (d) Load current i_l.

II. PRINCIPLE OPERATION OF A HVS DRIVER

A block diagram of a typical HVS system which consists of a signal board, a power board and a switching board, is shown in Fig. 1. The signal board is a gate control unit which generates on/off signals and protects the system under fault conditions. The power board has a full bridge converter connected to the primary side of the high frequency transformers on the switching board. The switching board, which is composed of 12 switches in series connection, is triggered by their floating gate drive circuits. The floating gate driver includes a *1:n* toroidal transformer and a pulse shaping circuit [3],[4].

The operation of the HVS system can be illustrated by the simulation results in Fig. 2, where a gate signal of 10 μs turns on an IGBT at a dc voltage of 1000 V and a resistor load of 50 Ω. Fig. 2(a) shows a bipolar waveform v_{on_off} of ±15 V generated by the signal board. It controls the full bridge converter to provide primary current through the transformers on the switching board. The induced current at the secondary side flows through the pulse shaping circuit generating a gate voltage v_{ge} as shown in Fig. 2 (b). The switch voltage v_{ce} and load current i_l are shown in Fig. 2 (c) and (d), respectively.

III. SHORT-CIRCUIT PROTECTION FOR A HVS

A short-circuit protection mechanism is added to the pulse shaping circuit on the switching board. The main objective is to make it capable of detecting and limiting fault currents earlier than the signal board of the HVS driver. In addition, the capability of a safe turn-off after a fault has to be guaranteed in order to protect the switches against voltage overshoot.

A. Arc Current Limit

The proposed arc current limiting circuit, which is added to

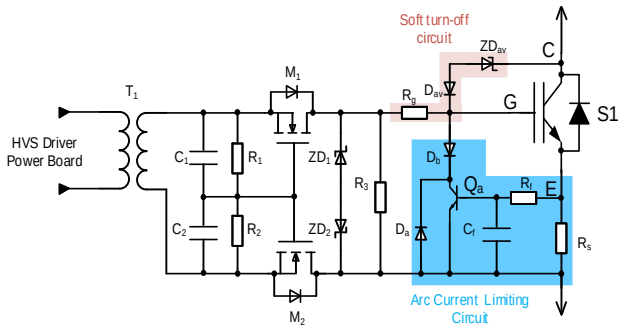


Fig. 3. Drive circuit with the addition of an arc current limit and a soft turn-off technique.

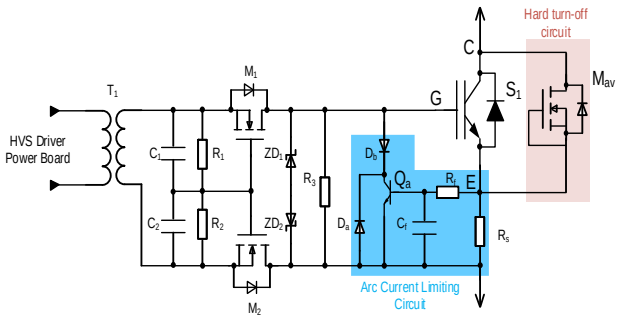


Fig. 4. Drive circuit with the addition of an arc current limit and a hard turn-off technique.

the pulse shaping circuit, is shown in Fig. 3. The circuitry consists of a sensing resistor R_s, an RC filter, a transistor Q_a and a negative off-stage block diode D_b. The sensing resistor R_s is connected in series with the emitter of an IGBT and serves as a fault sensing element. The circuit operates by sensing faults and subsequently lowering the gate voltage. The voltage across the sensing resistor is formed by the resistance R_s and the self-inductance L_s, which can be expressed as follows [9]:

$$V_s(s) = R_s I(s) + sL_s I(s) \quad (1)$$

where I is the current flowing through the sensing resistor, which is the sum of the gate current I_g and the load current I_l.

However, I_g can be neglected because I_l is much larger than I_g [9]. An RC filter connected in parallel with the sensing resistor distinguishes the fault current from any nuisance current spikes. The filter output voltage, V_f, can be described according to the sensing voltage V_s and the filter parameters R_f and C_f as follows:

$$V_f(s) = \frac{1}{\sqrt{1+(\omega R_f C_f)^2}} V_s(s) \quad (2)$$

Once V_f is higher than the turn-on voltage $V_{BE(on)}$ of the power transistor Q_a, the transistor Q_a is turned on which results in the gate voltage V_{ge} dropping below the gate threshold voltage. Thus, the magnitude of the fault current can be limited. From Eqs. (1) and (2), the proportion of the fault current to the filter output voltage can be derived as follows:

$$\mathrm{I(s)} = \frac{R_f C_f + \frac{1}{s}}{L_s + \frac{R_s}{s}} . V_f(s) \quad (3)$$

As can be seen in Eq. (3), under certain values of R_f and C_f, and the selected transistor Q_a, the detection value of fault currents can be adjusted by the experimental test with different sensing resistors.

B. Arc Current Turn-Off

Due to the existence of a stray inductance, the switch voltage can be expressed as follows:

$$v_{sw} = v_{dc} - L_p \frac{di_l}{dt} \quad (4)$$

where v_{sw} is the switch voltage, v_{dc} is the dc link voltage, and L_p is the stray inductance of the circuit.

During the turning off of the arc current, the negative *di/dt* of the high falling rate of the current results in a large spike in the switch voltage which causes failures of the switch. The soft and hard turn-off techniques, which are investigated to protect the switches against spike voltages, are shown in Fig. 3 and Fig. 4, respectively.

A soft turn-off circuit consists of a clamping diode ZD_{av} in series with a blocking diode D_{av} and a gate resistor R_g [16]. When the switch voltage exceeds the reverse breakdown voltage of ZD_{av}, the current $I_{ZD(av)}$ charges the IGBT's gate capacitance C_{ge} and results in an increase of the gate voltage above the gate threshold level. As a result, the switch is regained in the conduction state to clamp the switch voltage. This in turn leads to a drop in the switch voltage and consequently in the gate voltage, which turns the switch back off. This feedback mechanism clamps the switch voltage to a safe value. The rate of decay of the switch current is then equal to $(V_Z - V_{dc})/L_p$, where V_Z is the reverse breakdown voltage of ZD_{av}.

An arc fault at a high voltage causes an extremely high peak current which results in a high power pulse to the device. This transient power generates heat at the junction flowing through the chip to the case. The junction temperature T_J, which rose above the case temperature T_C , is proportional to this heat flow and the junction-to-case transient thermal impedance Z_{thJC}, expressed as [18]:

$$T_J = P_D Z_{thJC} + T_C \quad (5)$$

where P_D is the dissipated power of the switch during a short-circuit fault, which is the product of the fault current and the voltage across the device. The typical transient thermal impedance of voltage is across the device. The typical transient thermal impedance of a switch can be found in the device datasheet, and its variation depends on the pulse width. The longer the time of a high voltage and current applied simultaneously to the switch results in a higher power dissipation and transient thermal impedance. Hence, it results in a higher rise in the junction temperature according to Eq. (5). This in turn results in excessively maximum allowable

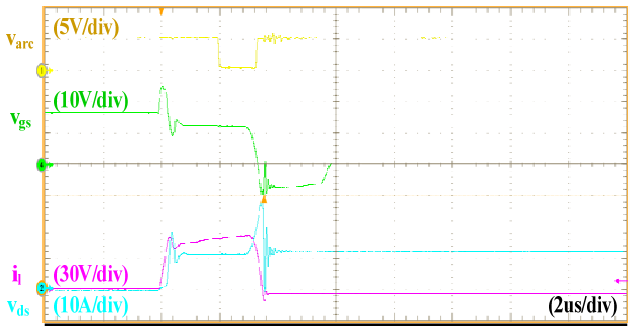


Fig. 5. Short-circuit test waveform with SiC MOSFET. Test condition: V_{dc}=250 V, soft turn-off.

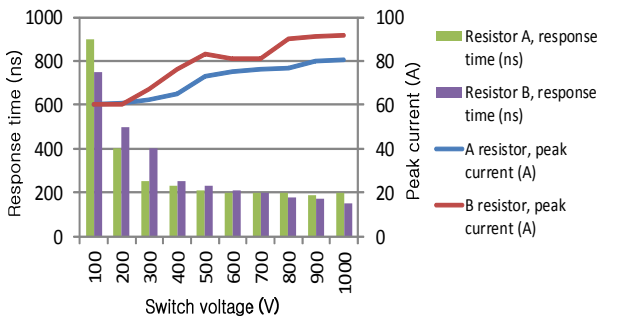


Fig. 6. Response time of arc current limiting circuit and peak current at different switch voltages.

value of 150 °C. In order to overcome this issue, a hard turn-off technique is proposed, as shown in Fig. 4. This technique uses a high avalanche energy device M_{av} in parallel with the main switch. During the arc current turn-off, an avalanche current flowing through M_{av} suppresses the overshoot voltage across the switch. Hence, the short-circuit conduction time of the switch S_1 can be reduced, which results in a smaller rise of the junction temperature. Consequently, the ability to withstand a short-circuit fault is improved at a high voltage. In addition, the gate resistor R_g is not used in the hard turn-off technique to reduce the turn-off time of the main switch.

IV. Development of the HVS Board

A. Selection of Switch S_1

The high switching speed and low power loss features of a SiC MOSFET are chosen to have an appropriate high voltage switch in pulse power applications. Hence, a 1200 V/ 60 A SiC MOSFET is selected for the switch S_1 to investigate short-circuit protection performance. Short-circuit test results with a v_{ds} of 250 V are shown in Fig. 5. The fault current is clamped at 80 A and turned off after approximately 3.3µs. However, a switch failure is found due to a short-circuit event at a v_{ds} of 300 V. The lack of a safe operating area in a SiC MOSFET causes this failure. A 1600 V/33 A IGBT with enhanced characteristics in terms of the safe operating area and transient thermal impedance is selected for short-circuit protection at higher voltages.

B. Selection of an Arc Current Limiting Circuit

According to Eq. (2), the selection of R_f and C_f should consider the time constant $\tau = R_f C_f$, which can produce a decrease of V_f and affect the filter delay time. As a rule of thumb, the time constant should be selected so that it is smaller than the turn-on switching time of the power transistor Q_a, which is rated at about 80 ns. Moreover, a low capacitance of C_f should be selected to present a high impedance filter which is capable of distinguishing fault current from normal switching. In that way, the selection of R_f and C_f are 100 Ω and 0.1 nF, respectively.

Under certain values of R_f and C_f and a selected transistor Q_a, various sensing resistors from different manufactures have been selected for a short-circuit test. Due to the high *di/dt* of the fault current, both the resistance and self-inductance have to be taken into consideration in the selection of a sensing resistor. The self-inductance of commercial sensing resistors varies in the range of 0.5 nH to 10 nH. Fig. 6 shows the response time of the arc current limiting circuit and the corresponding peak current of two resistors *A* and *B*. Resistor *A* is an open air sense-type of 10 mΩ. Resistor *B* is a series connection of two 3 mΩ resistors. As can be seen, a short-circuit event at a higher voltage leads a higher peak current and a faster response time. Sense resistor *A* is selected due to a lower peak fault current of 80 A at the 1 kV short-circuit test.

C. Selection of a Soft Turn-off Circuit

The clamping diode ZD_{av} should be selected so that its breakdown voltage is less than the maximum allowable voltage of the main switch of 1600 V. The avalanche diode type is preferred due to its high reserve voltage capability. Commercial avalanche diodes have reserve voltages up to 1500 V and an average forward current range from 1 A. An avalanche diode of 1500 V/ 2 A with a 20 mJ avalanche capability is selected as the clamping diode ZD_{av}. In addition, a 100 V/ 2 A Schottky diode is chosen as the blocking diode D_{av}.

D. Selection of a Hard Turn-off Circuit

An avalanche device in a parallel connection with a main switch has to be able to carry a large current when the voltage across the device exceeds its breakdown voltage. A power MOSFET with avalanche ruggedness features allows for a high reverse current flowing through itself in the avalanche mode. It will only fail when the temperature substantially exceeds the maximum junction temperature T_{jmax} [19]. Hence, the selected power MOSFET should have a high avalanche energy which can withstand a high current for a short time duration. A SiC rugged Power MOSFET rated at 1200 V with an avalanche energy of 1 J is selected for possibly carrying fault current during turn off.

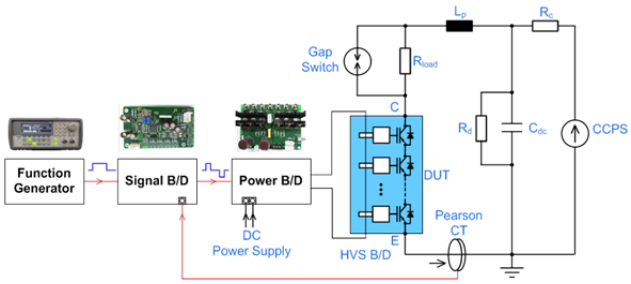


Fig. 7. Test circuit.

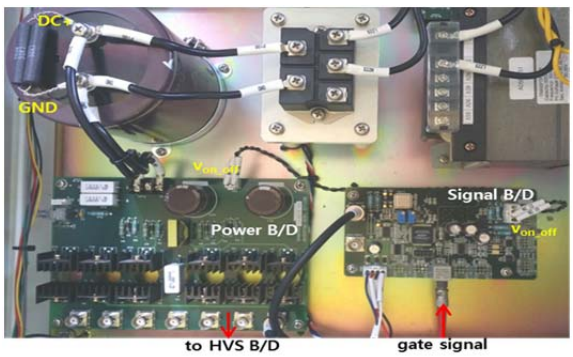


Fig. 8. Experimental setup of a drive system of a HVS board.

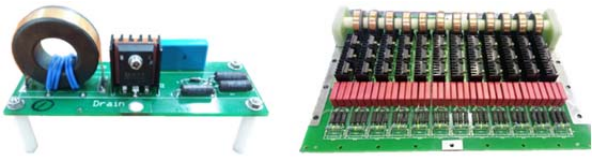
TABLE II
PARAMETERS OF TEST COMPONENTS

Devices	Description	Value
CCPS	Capacitor charging power supply	35[kJ]/50[kV]
R_c	Charging resistor	50[Ω]/100[kV]
R_d	Discharging resistor	20[MΩ]/100[kV]
C_{dc}	dc capacitor	4.7[uF]/50[kV]
L_p	Loop parasitic inductance	~10[uH]
R_{load}	Non-inductive load	200[Ω]/100[kV]
CT	Pearson current transformer	0.01[V]/[A]
Gap S/W	Manually S/W	100[kV]

V. TEST SETUP

Fig. 7 shows the testing circuit which includes a capacitor charging power supply (CCPS), a high voltage (HV) charging resistor R_c, a HV dc capacitor C_{dc}, a HV non-inductive load R_l, a gap switch and a device under test (DUT). The parameters of these devices are shown in Table II.

Their switching characteristics and short-circuit protection performances are investigated in a normal operation test and a short-circuit test, respectively. The normal operation test was conducted by firstly charging the dc capacitor to a predefined value. Then, a function generator is set in burst mode to provide a single pulse of 10 μs to the signal board. In the short-circuit test, the load resistor is replaced by a gap switch to make a short-circuit event. The gap switch includes two separate contacts. One contact is fixed and connected to the collector terminal of the switching board, and other contact is connected to the dc capacitor. The DUT is firstly turned on by a signal from the function generator. However there is no current flowing because the gap switch is manually kept in the open status. A fast touch between two contacts results in the occurrence of a short-circuit. Fig. 8 shows the experimental setup of the signal board, the power board and its dc power supply. A MAX7000 programmable logic device family EPM7128STC100-10 is used in the signal board for generating gate signals as well as for monitoring and protecting the HV switch. There are two detection circuits equipped on the signal board to individually detect overload currents and arc currents. Typically, an overload current is detected at a value of 1.1~1.3 times the load current I_L. As a result, a predefined value of the arc current is set at 1.5 times I_L to distinguish between the arc current and the overload current. Moreover, a higher preset value may cause a higher peak fault current due to a delay in the detection. When the fault current exceeds this predefined value, the programmable logic device on the signal board detects the arc occurrence and turns off the gate signal. The arc detection value in the signal board is set at 60A as a result of a rated load current of 40A.



(a) (b)

Fig. 9. Photos of DUT. (a) HVS1S1P board. (b) HVS12S2P board.

The development works were executed by a single switch board (HVS1S1P), and several single switch boards in series to evaluate the performance of the design circuits. Then, a HVS12S2P board, which is an array of 12 switches in series and 2 switches in parallel, were implemented. Fig. 9 shows photos of the HVS1S1P board and the HVS12S2P board.

VI. EXPERIMENT RESULTS

A. Single Switch Configuration

Fig. 10 shows single-shot test waveforms of a HVS1S1P board at a dc voltage of 1000 V. The normal operation of controlling a IGBT is clearly demonstrated. As can be seen, a single pulse of 10 μs, which is provided to the signal board, generates a bipolar voltage waveform v_{on_off} to the power board of the HVS driver. Hence, the gate driver is able to turn the IGBT off with a negative gate bias voltage. The switch voltage v_{ce} and load current i_l waveforms are obtained by a load R_l of 50 Ω. It can be observed that the normal operation of the gate driver in triggering an IGBT does not interfere with the protection circuits. Fig. 11 illustrates the protection performance of the arc current limiting circuit and soft turn-off circuit of a short-circuit fault at 1600 V. During the

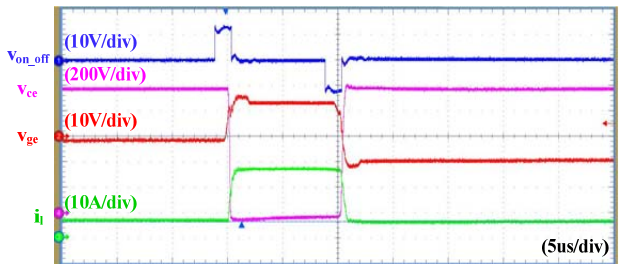


Fig. 10. Single-shot test of HVS1S1P board. Test condition: v_{dc}=1000 V, R_l=50 Ω.

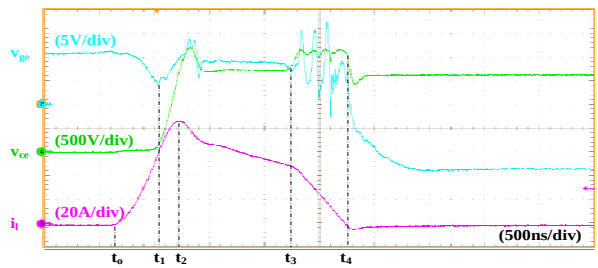


Fig. 11. Short-circuit test waveforms of HVS1S1P board. Test condition: v_{dc}=1600 V, soft turn-off.

(t_0~t_1) interval, a high *di/dt* current results in a voltage drop in v_{ge}, which in turn pulls the IGBT out of saturation at t_1 and limits the peak fault current to 94A at t_2 of 600 ns. After a delay of about 1.4 µs, the gate is turned off which results in a steep fall of the fault current during the (t_3~t_4) interval. As can be seen from the gate voltage waveform v_{ge}, the soft turn-off circuit is active to clamp the switch voltage v_{ce} at around 2100 V. The short-circuit turn-off time, which is defined as the duration of the current decrease from the peak value to zero, is about 1.6 µs.

Short-circuit test waveforms of the arc current limiting circuit and hard turn-off scheme are shown in Fig. 12. The test voltage is 1200 V, which is the maximum drain-to-source voltage of an avalanche MOSFET. As can be seen, the gate voltage v_{ge} is pulled below the threshold voltage which in turn limits the peak current to 77 A within 400 ns. Thanks to the effect of M_{av}, there is a steady decrease from the peak value to zero of the short-circuit current, which shortens the short-circuit turn-off time at about 800ns.

B. Series-Connected Switches Configuration

Three HVS1S1P boards using a soft turn-off technique are connected in series and implemented by a short-circuit test at a dc voltage of 4 kV. The collector-emitter voltage waveforms of the three switches and the load current are shown in Fig. 13. As can be seen, the short-circuit current is limited to 100 A after 200 ns from the occurrence of a fault. In addition, collector-emitter voltage waveforms of the three switches are well clamped below their breakdown voltage by the activation of the soft turn-off circuit. It can be observed that the possibility of the whole voltage being applied to only one of the three IGBTs during a short-circuit transient can be

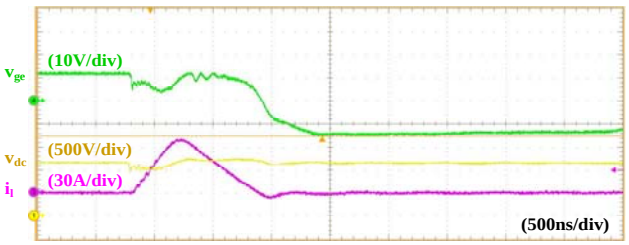


Fig. 12. Short-circuit test waveforms of HVS1S1P board. Test condition: v_{dc}=1200 V, hard turn-off.

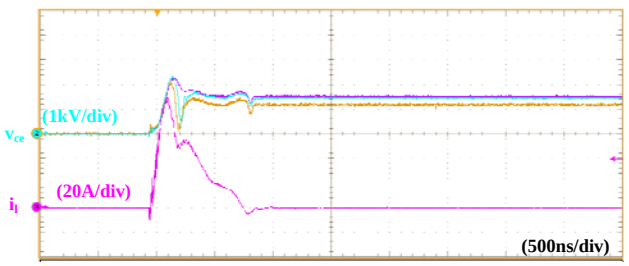


Fig. 13. Short-circuit test waveforms of three HVS1S1P boards in series. Test condition: v_{dc}=4 kV, soft turn-off.

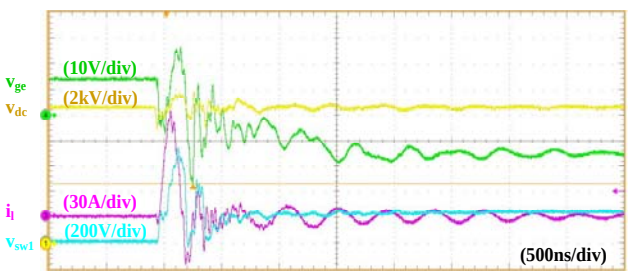


Fig. 14. Short-circuit test waveforms of HVS12S2P board. Test condition: v_{dc}=10 kV, hard turn-off.

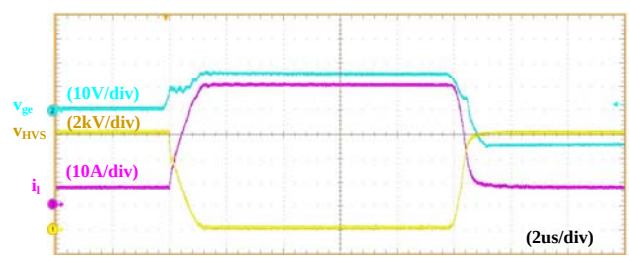


Fig. 15. Single-shot test waveforms of HVS12S2P board. Test condition: v_{dc}=8.4 kV, R_{load}=200 Ω.

eliminated. The peak power is calculated at 210 kW. The short- circuit turn-off time is about 600 ns. Then, ten HVS1S1P boards using a soft turn-off technique, which are connected in series, have been implemented by the short-circuit test. Three of them have been destroyed by the short-circuit test at a dc voltage of 10kV. Next, a HVS12S2P board using a hard turn-off technique has been developed to verify the short-circuit protection at high voltages. Short-circuit test results at a dc link voltage of 10 kV, which are illustrated in Fig. 14, show a significant reduction in the short-circuit turn-off time, which is about 120 ns. The arc current is limited to 125 A within a delay of 100 ns. Finally, normal operation has been tested at 8 kV with a

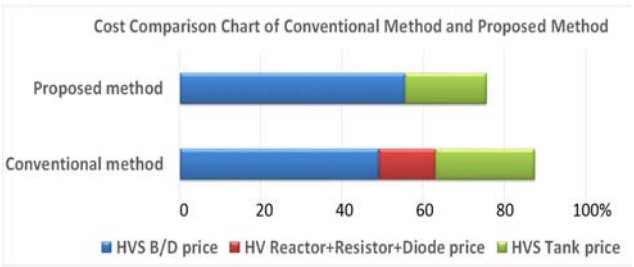


Fig. 16. Cost comparison between the conventional method and the proposed method.

non-inductive resistor load of 200 Ω. The corresponding gate voltage v_{ge}, switch board voltage v_{HVS} and load current i_l waveforms are shown in Fig. 15. The turn-on and turn-off switching times are 950 ns and 630 ns, respectively. It can be observed that the arc current limiting circuit does not affect the switching performance in normal operation.

A designed 80kV/40A HVS, which is formed by a series connection of eight of 10kV/40A HVS12S2P boards, has been used as a standard case to make a comparison between the conventional method and the proposed method. Thanks to the removal of the limiting inductor and its dissipated resistor and diode, the volume size of the HVS tank is reduced by 22% compared with the conventional method. Moreover, the cost of the proposed method is also reduced by 14% which is shown in Fig. 16.

VII. Conclusions

In this paper, the development of short-circuit protection schemes for a 10 kV HVS board have been presented. The arc current limiting and short-circuit turn-off circuits incorporated into the existing pulse shaping circuit have been investigated by short-circuit and normal operation tests at a high voltage. A typical HVS12S2P board was able to withstand a short-circuit fault at a rated voltage of 10 kV. The experimental results have also demonstrated a fast response time of 100 ns to a short-circuit current, which is limited to 125 A. A combination of the arc current limit circuit and the hard turn-off circuit has been selected by a significant reduction in the short-circuit turn-off time.

References

[1] S.-R. Jang, H.-J. Ryoo, and S.-B. Ok, "Pulsed-power system for leachate treatment application," *Journal of Power Electron.*, Vol. 11, No. 4, pp. 612-619, Jul. 2011.

[2] N. Q. T. Vo, Y.-W. Kim, and C.-H. Lee, "Long-pulse modulator for klystron using a high-voltage solid-state switch and a droop compensator," in *Proc. KIPE,* Vol.2, pp. 1339-1345, 2013.

[3] I.-H. Song, H.-S Ahn, Y.-K. Kim, H.-S Shin, C.-H.Choi, and M.-H. Cho, "Development of the 120 kV/70A high voltage switching circuit with MOSFETs operated by simple gate drive unit," *Transactions of Korean Institute of Power Electronics (KIPE)*, Vol. 8, No. 1, pp. 24-29, Feb. 2003.

[4] V. Zorngiebel, M. Hecquard, E. Spahn, A. Welleman, and S. Scharnholz, "Modular 50-kV IGBT switch for pulsed power application," *IEEE Trans. on Plasma Sci.*, Vol. 39, No. 1, pp. 364-367, Jan. 2011.

[5] G. E. Leyh, "A critical analysis of IGBT geometries, with the intention of mitigating undesirable destruction caused by fault scenarios of an adverse nature," in *Proc. Particle Accelerator Conf.*, Vol. 2, pp. 366-368, 2003.

[6] M. N. Nguyen, R. L. Cassel, J. E. deLamare, and G. C. Pappas, "Gate drive for high speed, high power IGBTs," in *Proc. PPPS-2001*, Vol. 2, pp. 1039-1042, 2001.

[7] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters - an overview," in *Proc. IEEE IECON*, pp. 507-513, 2013.

[8] R. Chokhawala, and G. Castino, "IGBT fault current limiting circuit," in *Proc. IEEE IASAM*, Vol. 2, pp. 1339-1345, 1993.

[9] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.,* Vol. 29, No. 7, pp. 3720-3732, Oct. 2014.

[10] B.-S. Suh and D.-S. Hyun, "An improved short circuit protection scheme for IGBT," *Transactions of Korean Institute of Power Electronics (KIPE)*, Vol. 3, No. 2, pp. 426-436, Dec. 1998.

[11] D. Gerber, T. Guillod, R. Leutwyler, and J. Biela, "Gate unit with improved short-circuit detection and turn-off capability for 4.5-kV press-pack IGBTs operated at 4-kA pulse current," *IEEE Trans. Plasma Sci.*, Vol. 41, No. 10, pp. 2641-2648, Oct. 2013.

[12] M. A. Rodríguez-Blanco, A. Vazquez-Pérez, L. Hernández-González, V. Golikov, J. Aguayo-Alquicira and M. May-Alarcón, "Fault detection for IGBT using adaptive thresholds during the turn-on transient," *IEEE Trans. Ind. Appl.*, Vol. 62, No. 3, pp. 1975-1983, Mar. 2015.

[13] B.-G. Park, J.-B. Lee, and D.-S. Hyun, "A novel short-circuit detecting scheme using turn-on switching characteristic of IGBT," in *Proc. IEEE IAS*, pp. 1-5, 2008.

[14] M. A. Rodríguez-Blanco, A. Claudio-Sánchez, D. Theilliol, L. G. Vela-Valdés, P. Sibaja-Terán, L. Hernández-González, J. Aguayo-Alquicira, "A failure-detection strategy for IGBT based on gate-voltage behavior applied to a motor drive system," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 5, pp. 1625-1633, May 2011.

[15] S. Karami, P. Poure, and S. Saadate, "Fast power switch failure detection for fault tolerant voltage source inverters using FPGA," *IET Trans. Power Electron.,* Vol. 2, No. 4, pp. 346-354, Jul. 2009.

[16] R. S. Chokhawala and S. Sobhani, "Switching voltage transient protection schemes for high-current IGBT modules," *IEEE Trans. Ind. Appl.*, Vol. 33, No. 6, pp. 1601-1610, Nov./Dec. 1997.

[17] J. Lutz and T. Basler, "Short-circuit ruggedness of high-voltage IGBTs," in *Proc. of MIEL.*, pp. 243-250, May 2012.

[18] NXP Semiconductors, *AN11158 Application note*, http://www.nxp.com/documents/application_note/AN11158.pdf, 2014.

[19] International Rectifier, *AN-1005 Application note,* www.infineon.com/dgdl/an-1005.pdf

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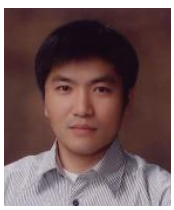

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