JPE 16-4-4

http://dx.doi.org/10.6113/JPE.2016.16.4.1277
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

An Isolated High Step-Up Converter with Non-Pulsating Input Current for Renewable Energy Applications

Kuo-Ing Hwu† and Wen-Zhuang Jiang*

†,*Department of Electrical Engineering, National Taipei University of Technology, Taipei City, Taiwan

Abstract

This study proposes a novel isolated high step-up galvanic converter, which is suitable for renewable energy applications and integrates a boost converter, a coupled inductor, a charge pump capacitor cell, and an LC snubber. The proposed converter comprises an input inductor and thus features a continuous input current, which extends the life of the renewable energy chip. Furthermore, the proposed converter can achieve a high voltage gain without an extremely large duty cycle and turn ratio of the coupled inductor by using the charge pump capacitor cell. The leakage inductance energy can be recycled to the output capacitor of the boost converter via the LC snubber and then transferred to the output load. As a result, the voltage spike can be suppressed to a low voltage level. Finally, the basic operating principles and experimental results are provided to verify the effectiveness of the proposed converter.

Key words: Isolated high step-up galvanic converter, Continuous input current, Coupled inductor, Charge pump, LC snubber

I. INTRODUCTION

In recent years, high step-up DC-DC converters have been widely used in many renewable energy systems, such as fuel cells and photovoltaic panels. However, the output voltages of these renewable energy systems are not always stable, and they are not high enough to supply the output load or to be linked to an AC power grid via a DC-AC inverter [1]-[3]. Consequently, a high step-up converter is required to obtain a high output voltage. For non-isolated converters to be considered, traditional boost and buck-boost converters [4] are widely used because of their simple structures. However, achieving high output voltages with a moderate duty cycle is difficult because of the parasitic components of these converters. In addition, the switches must block high output voltages. Accordingly, switches with high on-resistance are required; thus, the conduction loss is high. Many non-isolated step-up converters using different voltage-boosting techniques have been presented to achieve high output voltages. These voltage-boosting techniques include coupled inductors [5]-[10], switched capacitors [11], [12], voltage multipliers [13], [14], etc. However, in some applications, isolated converters are preferred to meet the safety requirements of galvanic isolation [15]. Therefore, the traditional flyback converter is appealing in industrial applications because of its low component count, simple structure, and low cost. However, it suffers from low voltage gain. Therefore, a number of isolated step-up converters have been presented [16]-[18]. In [16], a converter integrating an active clamp flyback converter and a voltage multiplier is presented. However, the input current is pulsating, hence the high input current ripple. In [17], an isolated converter comprising a tapped inductor and isolated switched capacitor is presented. However, the voltage gain is not high enough, the voltage spike is considerably high, and the input current is pulsating. In [18], an isolated converter consisting of a boost converter and a series resonant converter is presented. Even though the input current is non-pulsating, this converter involves two stages and comprises six switches, which increase the complexity of the overall circuit and the number of drivers. In [19] and [20], a two-switch flyback is presented. An additional MOSFET switch and two additional diodes are

Manuscript received Oct. 3, 2015; accepted Feb. 21, 2016
Recommended for publication by Associate Editor Yan Xing.
†Corresponding Author: eaglehwu@ntut.edu.tw
Tel: +886-2-2771-2171 ext. 2159, Fax: +886-2-2731-7187, National Taipei University of Technology
*Department of Electrical Engineering, National Taipei University of Technology, Taiwan

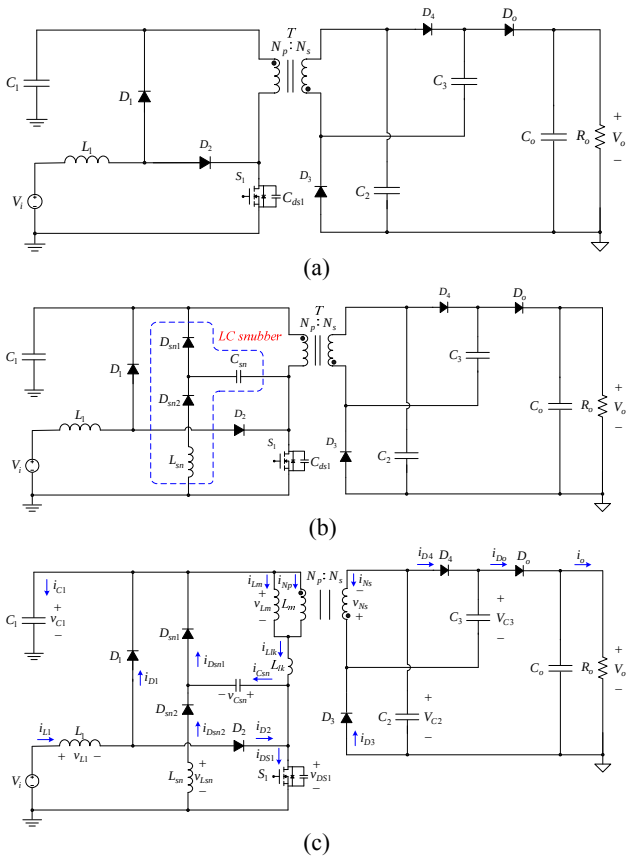

Fig. 1. Proposed isolated step-up converter: (a) without snubber; (b) with snubber but without current and voltage symbols; (c) with snubber and with current and voltage symbols.

added to the classic single-switch flyback converter to provide a recycling path for leakage inductance energy. Thus, the voltage spike can be clamped to the input voltage. In [21], an isolated high voltage-boosting converter derived from a forward converter is presented. An active clamp circuit is employed to reduce the voltage spike across the switch. However, the input current is pulsating; thus, this converter is not suitable for renewable energy applications. Moreover, this converter comprises four windings, and its selection of turn ratios is limited. Thus, designing a coupled inductor is difficult. In [22], an LC snubber used in a synchronously rectified flyback converter to clamp the switch voltage stress is presented because LC snubbers do not dissipate the energy theoretically and do not use any active switch. However, the input currents of the three aforementioned converters are pulsating. In renewable energy applications, DC-DC converters with a high voltage gain and non-pulsating input current are required. Therefore, in [23]-[26], non-isolated step-up converters featuring a continuous input current is presented. High step-up converters with a non-pulsating input current offers several advantages. First, the input current ripple is relatively small. Therefore, the life of the input capacitor can be upgraded. For high step-up converters with a pulsating input current, the input capacitor must absorb the high AC component of the input current. Second, a high input ripple may reduce the power outputted from the solar energy [27]. In [28], an isolated step-up converter featuring a continuous input current is presented.

As indicated by the discussion above, achieving a high output voltage necessitates a non-pulsating input current, galvanic isolation, and high efficiency. Thus, the present study proposes a novel isolated high step-up converter, which integrates a boost converter, a coupled inductor, a charge pump capacitor cell, and an LC snubber. In the proposed converter, the input current supplied from the source is continuous, a high voltage gain can be realized without a high turn ratio and a large duty cycle, the leakage inductance energy can be recycled to the output load, the voltage stresses across switches are low, and galvanic isolation exists between the input terminal and the output terminal.

II. Proposed Topology

Fig. 1(a) shows the proposed converter, which is composed of one input inductor L_1, one boost capacitor C_1, one boost diode D_1, one MOSFET switch S_1, one coupled inductor T comprising a primary winding with N_p turns and a secondary winding with N_s turns, two snubber diodes D_{sn1} and D_{sn2}, one snubber inductor L_{sn}, one snubber capacitor C_{sn}, two charge pump capacitors C_2 and C_3, two charge pump diodes D_3 and D_4, and one output capacitor C_o. Fig. 2(b) shows the proposed converter with the snubber. V_i, V_o, and R_o denote the input voltage, output voltage, and output resistor, respectively.

III. Basic Analysis of the Proposed Converter

For ease of analysis, we derive a number of assumptions and adopt voltage and current symbols.

1) The coupled inductor is modeled as an ideal transformer but with one magnetizing inductor L_m connected in parallel with the primary winding.
2) The MOSFET switch and diodes are viewed as ideal components.
3) The values of all the capacitors C_1, C_2, C_3, and C_o are large enough such that the voltages across them are kept constant at certain values.
4) The capacitances of C_2 and C_3 are equal.
5) The magnitude of the switching ripple is negligible. Therefore, small ripple approximation is adopted in the following analysis.
6) The turn ratio n of the coupled inductor is defined as N_s/N_p.

As shown in Fig. 1(c), the currents flowing through L_1, D_1, S_1, L_m, and the windings N_p and N_s are denoted by i_{L1}, i_{D1}, i_{DS1}, i_{Lm}, i_{Np}, and i_{Ns}, respectively. The currents flowing through D_{sn1} and D_{sn2} or L_{sn}, C_{sn}, D_2, D_3, D_4, D_o, and R_o are denoted by i_{Dsn1}, i_{Dsn2}, i_{Csn}, i_{D2}, i_{D3}, i_{D4}, i_{Do}, and i_o, respectively. Moreover,

the voltages across L_1, L_{sn}, C_{sn}, and S_1 are denoted by v_{L1}, v_{Lsn}, v_{Csn}, and v_{DS1}, respectively. The voltages across L_m or N_p, N_s, C_1, C_2, C_3, and C_o are denoted by v_{Lm}, v_{Ns}, V_{C1}, V_{C2}, V_{C3}, and V_o, respectively.

The following analysis covers the (i) operating principles, (ii) voltage gain, (iii) boundary condition for the input inductor, (iv) boundary condition for the magnetizing inductor, and (v) comparison of the proposed converter, the converter in [21], and the quasi-resonant (QR) flyback converter.

A. Operating Principles

The proposed converter comprises eight operating modes, and the key waveforms are shown in Fig. 2. The gate driving signal v_{gs1} of the switch S_1 has a duty cycle of D, where D is the DC quiescent duty cycle created from the controller.

1) Mode 1 [$t_0 \le t \le t_1$]: During this interval [Fig. 3(a)], S_1 is turned on, and D_2 is forward-biased. The currents i_{D3} and i_{D4} continue charging C_2 and C_3, respectively. The voltage across L_m and v_{Lm} is a negative value, which is induced from the secondary winding N_s. Hence, L_m remains demagnetized. The voltage $V_{C1}+(N_p/N_s)\times V_{C3}$ is imposed on L_{lk}, thereby causing i_{Llk} to increase rapidly. Furthermore, D_1 becomes reverse-biased, D_{sn2} becomes forward-biased, and D_{sn1} remains reverse-biased. Therefore, the input voltage V_i is imposed on L_1, thus causing L_1 to be magnetized. Moreover, C_{sn} releases energy to L_{sn}, thereby causing C_{sn} and L_{sn} to resonate during a positive cycle. D_o remains reverse-biased; hence, only C_o supplies energy to the load. This mode ends when i_{Llk} is equal to i_{Lm} at t=t_1.

2) Mode 2 [$t_1 \le t \le t_2$]: During this interval [Fig. 3(b)], S_1 is still turned on, D_3 and D_4 become reverse-biased, and D_o becomes forward-biased. Therefore, C_1, C_2, and C_3 provide energy to the load. Meanwhile, the voltage V_{C1} is imposed on L_m and L_{lk}, thus causing their continuous magnetization. Moreover, the energy stored in C_{sn} is continuously released to L_{sn} until v_{Csn} reaches zero. Thereafter, the energy stored in L_{sn} is released to charge C_{sn}. As a result, the voltage across C_{sn} and v_{Csn} increases in the opposite direction. This mode ends when v_{Csn} reaches $-V_{C1}$ at t=t_2.

3) Mode 3 [$t_2 \le t \le t_3$]: During this interval [Fig. 3(c)], S_1 is turned on; D_1, D_3, and D_4 are reverse-biased; and D_{sn2} and D_o are forward-biased. The voltage across the snubber capacitor v_{Csn} is clamped to $-V_{C1}$. Moreover, the diode D_{sn1} is forced to conduct by the current from L_{sn}. Therefore, the energy stored in L_{sn} is transferred to the output load via the coupled inductor. This mode ends when the energy from L_{sn} drops to zero, i.e., i_{Dsn2} reaches zero at t=t_3.

4) Mode 4 [$t_3 \le t \le t_4$]: During this interval [Fig. 3(d)], S_1 is turned on; D_1, D_2, and D_3 are reverse-biased; and D_o is forward-biased. After i_{Dsn2} reaches zero, the diodes D_{sn1} and D_{sn2} become reverse-biased. This mode ends when S_1 is turned off at t=t_4.

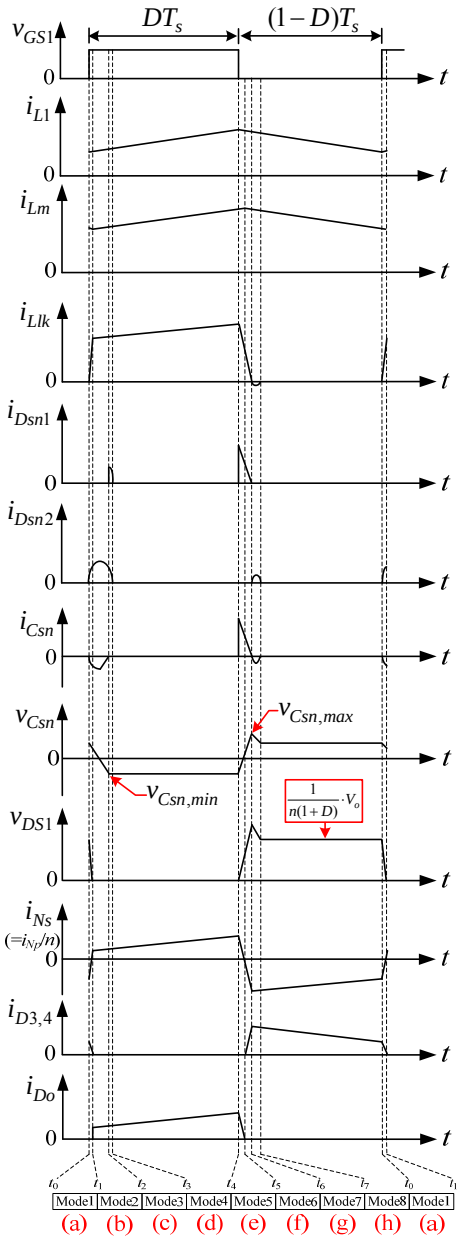

Fig. 2. Illustrated waveforms of the proposed converter in CCM for both L_1 and L_m.

5) Mode 5 [$t_4 \le t \le t_5$]: During this interval [Fig. 3(e)], S_1 is turned off, but C_2, C_3, and the coupled inductor continue to supply energy to the load. Moreover, the energy stored in L_1 is released to C_1 via D_1, and the leakage inductance current i_{Llk} charges the snubber capacitor C_{sn} via D_{sn1} and the parasitic capacitor C_{ds1}. Therefore, v_{Csn} increases linearly from $-V_{C1}$. This mode ends when i_{Ns} reaches zero at t=t_5.

6) Mode 6 [$t_5 \le t \le t_6$]: During this interval [Fig. 3(f)], S_1 is turned off. The only difference between the previous mode and the current mode is that the energy stored in the

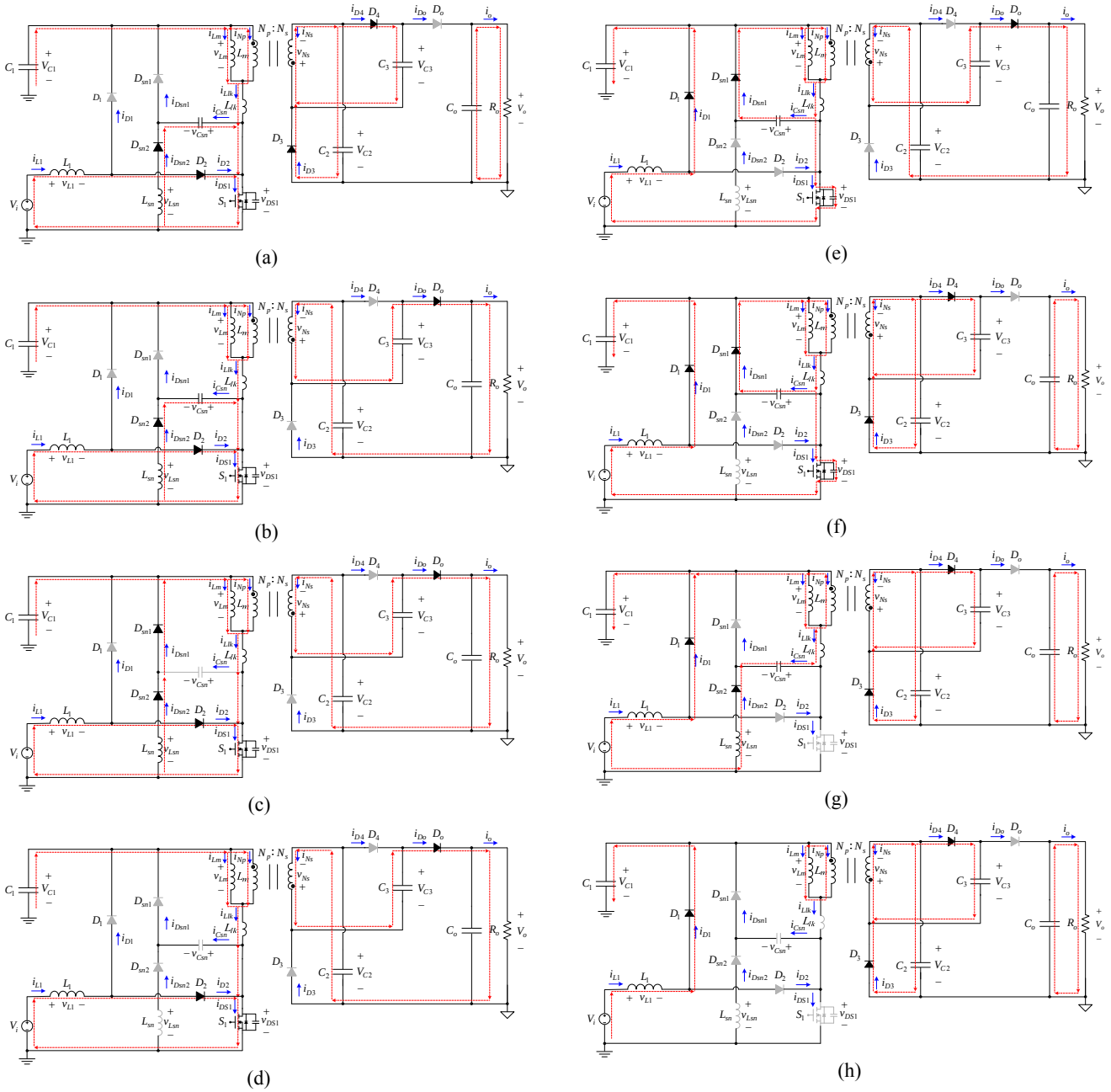

Fig. 3. Power flow paths over one switching period in CCM. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

magnetizing inductor L_m is transferred to C_2 and C_3, which are connected in parallel via D_3 and D_4. Meanwhile, the output diode D_o becomes reverse-biased. Therefore, only the output capacitor C_o provides energy to the load. Moreover, the leakage inductance current i_{Llk} continuously releases energy to the snubber capacitor C_{sn}, thereby causing v_{Csn} to increase gradually. The voltage across S_1 also increases and becomes equal to $V_{C1}+v_{Csn}$. This mode ends when i_{Llk} reaches zero at $t=t_6$.

7) Mode 7 [$t_6 \le t \le t_7$]: During this interval [Fig. 3(g)], S_1 is turned off. The snubber capacitor voltage v_{Csn} reaches the maximum value, which is higher than $V_{C1}+V_{C2}/n$. Consequently, the diode D_{sn2} becomes forward-biased. Therefore, the energy stored in C_{sn} is discharged to C_1 and the secondary side. During this period, L_m is clamped to $-V_{C3}\cdot(N_p/N_s)$. Moreover, the snubber capacitor C_{sn}, snubber inductor L_{sn}, and leakage inductor L_{lk} resonate together. This mode ends when i_{Dsn2} reaches zero at $t=t_7$.

8) Mode 8 [$t_7 \le t \le t_0$]: During this interval [Fig. 3(h)], S_1 remains turned off. With i_{Dsn2} reaching zero, D_{sn2} becomes reverse-biased. Moreover, L_m continuously delivers energy to charge C_2 and C_3. Therefore, i_{Lm} decreases gradually. During

this period, the voltage across L_{lk} is zero. Thus, the voltage stress of S_1 is $V_{C1}+(N_p/N_s)\cdot V_{C3}$. This mode ends when S_1 is turned on at $t=t_0$. The next cycle is subsequently repeated.

B. Voltage Gain

Only Figs. 3(b) and (f) are considered, and the leakage inductor L_{lk} and LC snubber are ignored to obtain the voltages across C_1, C_2, and C_3, as well as the voltage gain. The voltages across L_1 and L_m, as shown in Fig. 3(b), are written as follows:

$$v_{L1}=V_i \tag{1}$$

$$v_{Lm}=V_{C1} \tag{2}$$

The voltages across L_1 and L_m, as shown in Fig. 3(f), are written as follows:

$$v_{L1}=V_i-V_{C1} \tag{3}$$

$$v_{Lm}=-V_{C2}/n \tag{4}$$

First, by applying the voltage–second balance principle to L_1 over one switching period, the following equation can be obtained:

$$V_i\times D+(V_i-V_{C1})\times(1-D)=0 \tag{5}$$

By rearranging the above equation, the voltage across C_1 can be obtained as

$$V_{C1}=V_i\times\frac{1}{1-D} \tag{6}$$

Second, by applying the voltage–second balance principle to L_m over one switching period, the following equation can be obtained:

$$V_{C1}\times D+(-V_{C2}/n)\times(1-D)=0 \tag{7}$$

By rearranging the above equation, the voltages across C_2 and C_3 can be obtained as

$$V_{C2}=V_{C3}=n\times\frac{D}{1-D}\times V_{C1}=n\times\frac{D}{(1-D)^2}\times V_i \tag{8}$$

On the basis of Fig. 3(b), the output voltage can be determined as follows:

$$\begin{aligned}V_o&=V_{C2}+V_{C3}+v_{Ns}\\&=\frac{2nD}{(1-D)^2}V_i+\frac{n}{1-D}V_i=\frac{n(1+D)}{(1-D)^2}V_i\end{aligned} \tag{9}$$

The corresponding voltage gain can be expressed as

$$\frac{V_o}{V_i}=\frac{n(1+D)}{(1-D)^2} \tag{10}$$

Fig. 4 shows the curves of the voltage gain versus the duty cycle of the proposed converter with different turn ratios considered.

C. Boundary Condition for Input Inductor

The condition for the magnetizing inductor L_1 operating in a specific region is described as follows:

$$\begin{cases}2I_1\ge\Delta i_{L1}, & \text{for CCM}\\ 2I_1<\Delta i_{L1}, & \text{for DCM}\end{cases} \tag{11}$$

where I_{L1} and Δi_{L1} are the DC and AC components of i_{L1}, respectively.

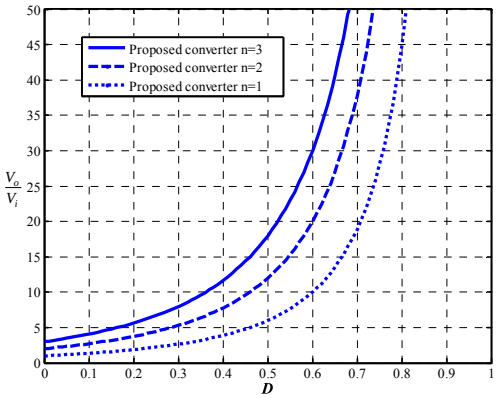

Fig. 4. Curves of voltage gain versus duty cycle of the proposed converter with different values of turn ratio *n*.

For ease of analysis, we assume that the input power is equal to the output power. Therefore, the input current I_{L1} can be expressed as

$$I_{L1}=\frac{n(1+D)}{(1-D)^2}\times I_o \tag{12}$$

Substituting V_o/R_o into I_o in (12) yields the following equation:

$$I_{L1}=\frac{n(1+D)}{(1-D)^2}\times\frac{V_o}{R_o} \tag{13}$$

Moreover, Δi_{L1} can be written as

$$\Delta i_{L1}=\frac{v_{L1}\Delta t}{L_1}=\frac{V_iDT_s}{L_1} \tag{14}$$

Given that $2I_{L1}\ge\Delta i_{L1}$, L_1 operates in the CCM. The further deduction is shown as follows:

$$\begin{aligned}&2I_{L1}\ge\Delta i_{L1}\\&\Rightarrow 2\times[\frac{n(1+D)}{(1-D)^2}\times\frac{V_o}{R_o}]\ge\frac{V_iDT_s}{L_1}\\&\Rightarrow\frac{2L_1}{R_oT_s}\ge\frac{D(1-D)^4}{[n(1+D)]^2}\\&\Rightarrow K_1\ge K_{crit1}(D)\end{aligned} \tag{15}$$

where $K_1=\dfrac{2L_m}{R_oT_s}$ and $K_{crit1}(D)=\dfrac{D(1-D)^4}{[n(1+D)]^2}$

Based on (15), the relationship between $K_{crit1}(D)$ and D is shown in Fig. 5 under the condition that n is set to 3. As shown in Fig. 5, L_1 operates in CCM if K_1 is larger than $K_{crit1}(D)$; otherwise, L_1 operates in DCM.

D. Boundary Condition for Magnetizing Inductor

The condition for the magnetizing inductor L_m operating in a given region is described as follows:

$$\begin{cases}2I_{Lm}\ge\Delta i_{Lm}, & \text{for CCM}\\ 2I_{Lm}<\Delta i_{Lm}, & \text{for DCM}\end{cases} \tag{16}$$

where I_{Lm} and Δi_{Lm} are the DC and AC components of i_{Lm}, respectively.

The expression of I_{Lm} can be derived from (17) to (20). For

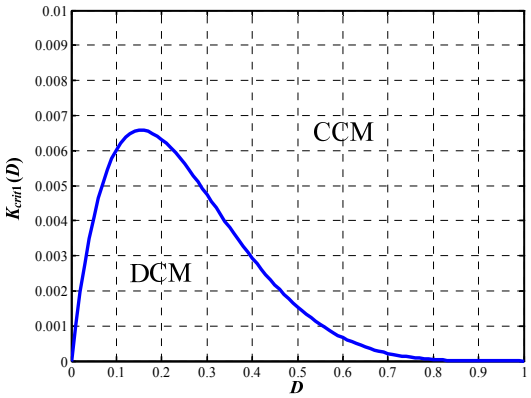

Fig. 5. Boundary condition for the input inductor L_1.

ease of analysis, we assume that the input power is equal to the output power. According to the voltage–second balance principle for inductors and the ampere–second balance principle for capacitors, the DC component of the inductor voltage and the DC component of the capacitor current are both zero over one switching period in the steady state.

Therefore, as shown in Fig. 6(a), the DC component of i_{Ns} and I_{Ns} is equal to the output current I_o. Similarly, the DC component of i_{Lm} and I_{Lm} is equal to the current I_x entering the primary side of the coupled inductor plus the DC component of i_{Np} and I_{Np} (Figs. 6(a) and (b)). Therefore,

$$I_x = (1-D)\times I_{L1} \tag{17}$$

On the basis of (13) and (17), I_x can be derived as

$$I_x = (1-D)\times\frac{n(1+D)}{(1-D)^2}\times I_o \tag{18}$$

$$I_{Np} = n\times I_{Ns} = n\times I_o \tag{19}$$

$$I_{Lm} = I_x + I_{Np} = [\frac{n(1+D)}{(1-D)}+n]\times I_o = \frac{2n}{1-D}\times\frac{V_o}{R_o} \tag{20}$$

In addition, Δi_{Lm} can be written as

$$\Delta i_{Lm} = \frac{v_{Np}\Delta t}{L_m} = \frac{V_{C1}DT_s}{L_m} = \frac{V_iDT_s}{(1-D)L_m} \tag{21}$$

As $2I_{Lm} \geq \Delta i_{Lm}$, L_m operates in CCM. The further deduction is shown as follows:

$$\begin{aligned} &2I_{Lm} \geq \Delta i_{Lm} \\ &\Rightarrow 2\times(\frac{2n}{1-D}\times\frac{V_o}{R_o}) \geq \frac{V_iDT_s}{(1-D)L_m} \\ &\Rightarrow \frac{2L_m}{R_oT_s} \geq \frac{D(1-D)^2}{2n^2(1+D)} \\ &\Rightarrow K_2 \geq K_{crit2}(D) \end{aligned} \tag{22}$$

where $K_2 = \frac{2L_m}{R_oT_s}$ and $K_{crit2}(D) = \frac{D(1-D)^2}{2n^2(1+D)}$.

Based on (22), the relationship between $K_{crit2}(D)$ versus D is shown in Fig. 7 under the condition that n is set to 3. As shown in Fig. 7, L_m operates in CCM if K_2 is larger than $K_{crit2}(D)$; otherwise, L_m works in DCM.

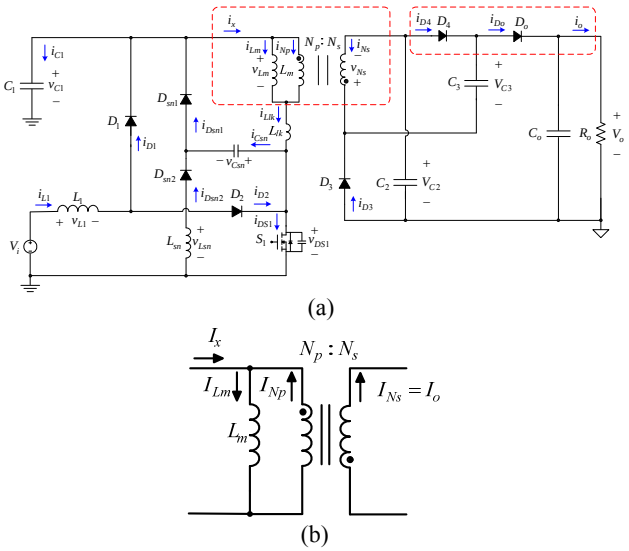

Fig. 6. DC component: (a) marked areas in the proposed converter used to analyze I_{Lm}; (b) equivalent model for the DC analysis of the coupled inductor.

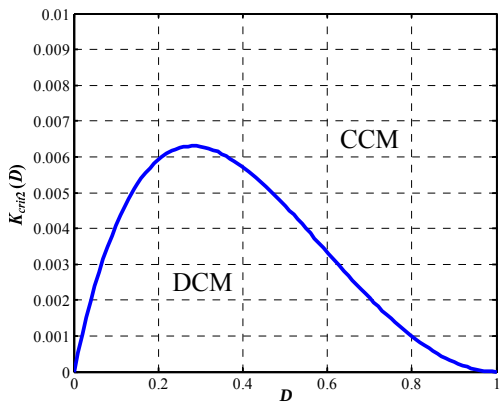

Fig. 7. Boundary condition for the magnetizing inductor L_m.

E. Comparison of the Proposed Converter, the Converter in [21], and the QR Flyback Converter

With the snubber disregarded, the proposed converter is compared with the converter in [21] and the quasi-resonant flyback converter (Table I).

Table I shows that the voltage gain of the converter in [21] can be determined by the duty cycle and four windings N_1, N_2, N_3, and N_4. However, the selection of turn ratios is limited, that is, $N_4 > N_3 - N_2$. The design procedure of the coupled inductor of the converter in [21] is more complicated than that of the proposed converter. Furthermore, the proposed converter entails a continuous input current and is thus suitable for renewable energy applications. The converter in [21] includes an output inductor; hence, the voltage gain is low. Therefore, in comparison with the proposed converter, the converter in [21] achieves a higher duty cycle and turn ratio. When voltage stress is considered, the duty cycle can be relatively short because the voltage gain of the proposed converter is high. Thus, voltage stress can be maintained at a low value.

TABLE I
COMPARISON OF THE PROPOSED CONVERTER, THE QR FLYBACK CONVERTER, AND THE CONVERTER IN [21]

Converter	QR flyback	[21]	Proposed
Voltage gain	$\frac{D}{1-D}(\frac{N_2}{N_1})$	$D(\frac{N_2}{N_1}+\frac{N_3}{N_1}\frac{D}{1-D}+\frac{N_4}{N_1})$	$\frac{N_p}{N_s}\cdot\frac{(1+D)}{(1-D)^2}$
Number of switches	1	1	1
Number of diodes	1	3	5
Number of capacitors	1	2	4
Number of coupled inductors	1	1	1
Number of coupled inductor windings	2	4	2
Number of input inductors	0	0	1
Number of output inductors	0	1	0
Switch voltage stress without spike	$\frac{1}{1-D}\cdot V_i$	$\frac{1}{1-D}\cdot V_i$	$\frac{1}{(1-D)^2}\cdot V_i$
DC magnetizing inductance current	$\frac{1}{1-D}\cdot\frac{N_2}{N_1}I_o$	$\frac{(\frac{D}{1-D})N_3+N_4}{N_1}\cdot I_o$	$\frac{2}{1-D}\cdot\frac{N_p}{N_s}I_o$
Input current	Pulsating	Pulsating	Non-pulsating
Isolation	Yes	Yes	Yes

Table I also shows the details of the QR flyback converter. Its voltage gain is much lower than that of the proposed converter. Thus, to achieve a high voltage gain, the flyback converter requires a high duty cycle and a high turn ratio. Moreover, it is often used in low-power applications. The MOSFET switch can be turned on at its voltage valley to reduce the switching loss resulting from the QR control [29]. For conduction loss to be considered, the component characteristics, component count, and root mean square (RMS) must be taken into account. The flyback converter exhibits a smaller component count than the proposed converter. For the flyback converter to achieve the same voltage gain as the proposed converter, its duty cycle and turn ratio should be significantly larger. In such a case, current stress and the resistance of the coupled inductor become considerably high. In comparison with the flyback converter, the proposed converter exhibits a much higher voltage gain, hence the minimal duty cycle and turn ratio that it requires.

IV. DESIGN CONSIDERATIONS

To verify the effectiveness of the proposed converter, we build and test a prototype. Tables II and III show the specifications and components of the proposed converter, respectively.

The design procedures for the input inductor L_1, magnetizing inductor L_m, and LC snubber [22] are described as follows.

A. Inductor Design

TABLE II
SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Input voltage (V_i)	12 V
Rated output voltage (V_o)	200 V
Rated output current ($I_{o,rated}$)/power ($P_{o,rated}$)	0.5 A/100 W
Minimum output current ($I_{o,min}$)/power ($P_{o,min}$)	0.1 A/20 W
Switching frequency (f_s)	100 kHz
Quiescent duty cycle (D)	0.483

TABLE III
COMPONENTS USED IN THE PROPOSED CONVERTER

Components		Specifications
MOSFET switch S_1		STP120NF
Diodes	D_1, D_2	MBR40100PT
	D_3, D_4, D_o	MUR860
Boost capacitor C_1		68 μF electrolytic capacitor
Charge pump capacitors C_2, C_3		68 μF electrolytic capacitor
Output capacitor C_o		120μF electrolytic capacitor
Input inductor L_1		40 μH
Coupled inductor T		L_m=51 μH, L_{lk}=0.62 μH, n=3
Gate driver		TC4420
Photocoupler		TLP250
LC snubber	L_{sn}	15 μH
	C_{sn}	Two 22 nF film capacitors
	D_{sn1}, D_{sn2}	V20120C

1) Input Inductor Design: To ensure that the input inductor current i_{L1} is always in CCM, we derive the corresponding equations as follows:

$$I_{L1,min} = \frac{n(1+D)}{(1-D)^2} \times I_{o,min} = \frac{3(1+0.483)}{(1-0.483)^2} \times 0.1 \approx 1.66\text{A} \quad (23)$$

$$L_1 > \frac{v_{L1}\Delta t}{\Delta i_{L1}} = \frac{V_i D T_s}{2 \times I_{i,min}} = \frac{12 \times 0.483 \times 10\mu}{2 \times 1.66} \approx 17.5\mu\text{H} \quad (24)$$

where $I_{L1,min}$ is the minimum DC current in L_1. Hence, the value of L_1 is set to 40 μH.

Based on (15) and the parameters selected for the proposed converter, the input inductor current i_{L1} is under CCM when the output current I_o is higher than 0.0436 A, which is calculated in (25). When the output current I_o is lower than 0.0436 A, the input inductor current i_{L1} enters into DCM.

$$\begin{aligned} &\frac{2L_1}{R_o T_s} \geq \frac{D(1-D)^4}{[n(1+D)]^2} \\ &\Rightarrow I_o \geq \frac{D(1-D)^4}{[n(1+D)]^2} \times (\frac{T_s}{2L_1}) \times V_o \\ &\Rightarrow I_o \geq \frac{0.483 \times (1-0.483)^4}{[3 \times (1+0.483)]^2} \times (\frac{10\mu}{2 \times 40\mu}) \times 200 \\ &\Rightarrow I_o \geq 0.0436\text{A} \end{aligned} \quad (25)$$

Finally, the current ripple of i_{L1} is shown in (26).

$$\Delta i_{L1} = \frac{v_{L1}\Delta t}{L_1} = \frac{V_i D T_s}{L_1} = \frac{12 \times 0.483 \times 10\mu}{40 \times 10^{-6}} \approx 1.5\text{A} \quad (26)$$

2) Magnetizing Inductor Design: To ensure that the magnetizing inductor current i_{Lm} is always in CCM, we write the corresponding equations as follows:

$$I_{Lm,min} = \frac{2n}{1-D} \times I_{o,min} = \frac{2 \times 3}{1-0.483} \times 0.1 \approx 1.16\text{A} \quad (27)$$

$$\begin{aligned} L_m &> \frac{V_i D T_s}{(1-D)\Delta i_{Lm}} = \frac{V_i D T_s}{(1-D) \times 2 \times I_{Lm,min}} \\ &= \frac{12 \times 0.483 \times 10\mu}{(1-0.483) \times 2 \times 1.16} \approx 48.3\mu\text{H} \end{aligned} \quad (28)$$

where $I_{Lm,min}$ is the minimum DC current in L_m. Hence, the value of L_m is set to 51 μH.

Based on (22) and the parameters selected for the proposed converter, the magnetizing inductor current i_{Lm} is under CCM when the output current I_o is higher than 0.0948 A, which is calculated in (29). When the output current I_o is lower than 0.0948 A, the magnetizing inductor current i_{Lm} enters into DCM.

$$\begin{aligned} &\frac{2L_m}{R_o T_s} \geq \frac{D(1-D)^2}{2n^2(1+D)} \\ &\Rightarrow I_o \geq \frac{D(1-D)^2}{2n^2(1+D)} \times (\frac{T_s}{2L_m}) \times V_o \\ &\Rightarrow I_o \geq \frac{0.483 \times (1-0.483)^2}{2 \times 3^2 \times (1+0.483)} \times (\frac{10\mu}{2 \times 51\mu}) \times 200 \\ &\Rightarrow I_o \geq 0.0948\text{A} \end{aligned} \quad (29)$$

Finally, the current ripple of i_{Lm} is shown in (30).

$$\begin{aligned} \Delta i_{Lm} &= \frac{v_{Lm}\Delta t}{L_m} = \frac{V_i D T_s}{(1-D)L_m} \\ &= \frac{12 \times 0.483 \times 10\mu}{(1-0.483) \times 51 \times 10^{-6}} \approx 2.2\text{A} \end{aligned} \quad (30)$$

B. LC Snubber Design

The voltage spike is severe when the output load is rated. Hence, the LC snubber is designed at a rated load (CCM for both L_1 and L_m).

1) Snubber capacitor design: The energy stored in the primary-side leakage inductance L_{lk} during the turn-on period is

$$E_{Llk} = \frac{1}{2} \cdot L_{lk} \cdot [(i_{Llk,max})^2 - (i_{Llk,min})^2] \quad (31)$$

The energy stored in the snubber capacitor is

$$E_{Csn} = \frac{1}{2} \cdot C_{sn} \cdot [(v_{Csn,max})^2 + (v_{Csn,min})^2] \quad (32)$$

If the primary-side leakage inductance energy is released entirely to the snubber capacitor, then the following equality can be obtained:

$$E_{Llk} = E_{Csn} \quad (33)$$

Based on (31), (32), and (33), the value of the snubber capacitor can be determined as follows:

$$C_{sn} = \frac{L_{lk}(i_{Llk,max}^2 - i_{Llk,min}^2)}{v_{Csn,max}^2 + v_{Csn,min}^2} \quad (34)$$

where $i_{Llk,max}$ is the maximum leakage inductance current, $i_{Llk,min}$ is the minimum leakage inductance current, $v_{Csn,max}$ is the maximum voltage across C_{sn}, and $v_{Csn,min}$ is the minimum voltage across C_{sn} (Fig. 8).

In mode 2 [Fig. 3(b)], $v_{Csn,min}$ is clamped to $-V_{C1}$. In mode 5 [Fig. 3(e)] and mode 6 [Fig. 3(f)], Δv_{Csn} is identical to Δv_{DS1}. Therefore, $v_{Csn,min}$ can be obtained as follows:

$$\begin{aligned} v_{Csn,min} &= -V_{C1} = -V_i \times \frac{1}{1-D} \\ &= -12 \times \frac{1}{1-0.483} = -23.2\text{V} \end{aligned} \quad (35)$$

In mode 5 [Fig. 3(e)] and mode 6 [Fig. 3(f)], Δv_{Csn} is identical to Δv_{DS1}. Accordingly, the maximum spike voltage of v_{DS1} is assumed to be 60 V because of the leakage inductance. Therefore, $v_{Csn,max}$ can be obtained as follows:

$$v_{Csn,max} = \Delta v_{Csn} + (-V_{C1}) = 60 - 23.2 = 36.8\text{V} \quad (36)$$

Based on (34), the value of the snubber capacitor can be determined as follows:

$$\begin{aligned} C_{sn} &= \frac{L_{lk}(i_{Llk,max}^2 - i_{Llk,min}^2)}{v_{Csn,max}^2 + v_{Csn,min}^2} \\ &= \frac{0.62\mu \times (10^2 - 0)}{(36.8)^2 + (-23.2)^2} \approx 33\text{nF} \end{aligned} \quad (37)$$

Finally, two 22 nF film capacitors connected in parallel are chosen for C_{sn}.

2) Snubber inductor design: The snubber inductance L_{sn} can be estimated by using the following equation:

$$f_{sn} = \frac{1}{2\pi\sqrt{L_{sn}C_{sn}}} \quad (38)$$

If the resonance frequency of the LC snubber is assumed to

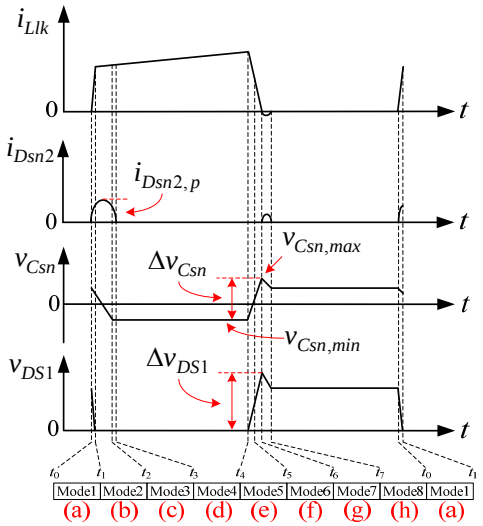

Fig. 8. Waveforms for designing the LC snubber for both L_1 and L_m operating in CCM.

be twice the switching frequency, then the snubber inductance can be obtained as follows:

$$L_{sn} = \frac{1}{(2\pi)^2 \times C_{sn} \times f_{sn}^2} = \frac{1}{(2\pi)^2 \times (2 \times 22 \times 10^{-9}) \times (2 \times 100 \times 10^3)^2} \approx 14.4\mu H \quad (39)$$

Finally, the value of L_{sn} is set to 15 μH.

V. Experimental Results

Figs. 9 and 10 show the measured waveforms at a rated load. Fig. 9 shows the gate driving signal for S_1, v_{GS1}; the voltage across S_1, v_{DS1}; and the input current, i_{L1}. Fig. 10 shows the gate driving signal for S_1, v_{GS1}; the current flowing through L_{lk}, i_{Lk}; and the secondary side current, i_{Ns}.

Fig. 9 shows that the spike voltage of v_{DS1} is clamped at 56 V and that the voltage stress without a spike is about 45 V, which is approximately equal to the calculated value of $V_o/[n(1+D)] \approx 44.9$V. The input current is continuous, and its peak-to-peak current value is about 1.5 A. Fig. 10 shows that during the turn-off period of S_1, i_{Ns} is a negative current, which matches the waveform of i_{Llk} shown in Fig. 2.

Figs. 11 and 12 show the measured waveforms at a light load. Fig. 11 shows the waveforms of v_{DS1} and i_{L1}. At a light load, i_{L1} enters into DCM. The voltage spike is low, and the voltage stress without a spike is about 45 V. As a result of the entry to DCM, a resonance voltage is noted across v_{DS1}. This effect is attributed to L_m and L_{lk} resonating with C_{ds1}. Fig. 12 shows i_{Lk} and i_{Ns}. Here, i_{lk} is low at a light load. Therefore, when S_1 is turned off, the voltage spike becomes considerably low.

Fig. 13 shows the curve of efficiency versus the load current. The efficiency across the load range ranges from 82% to 89%, whereas the rated load efficiency is about 85%.

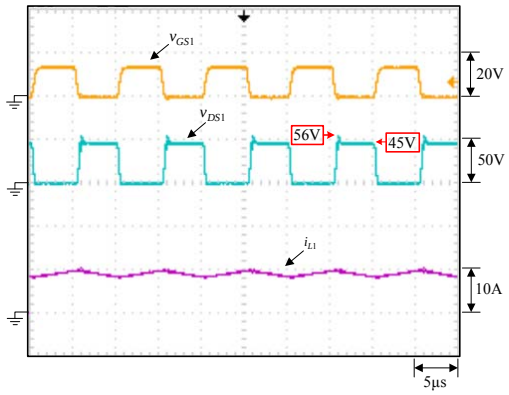

Fig. 9. Waveforms at a rated load: (1) v_{GS1}; (2) v_{DS1}; (3) i_{L1}.

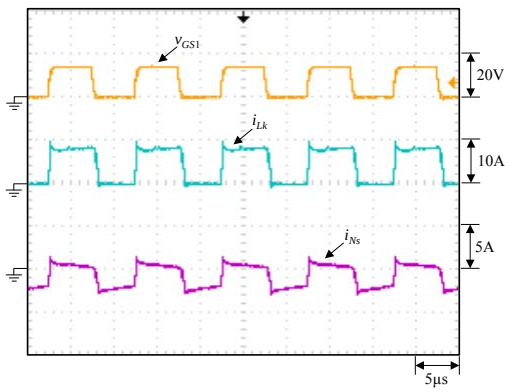

Fig. 10. Waveforms at a rated load: (1) v_{GS1}; (2) i_{Lk}; (3) i_{Ns}.

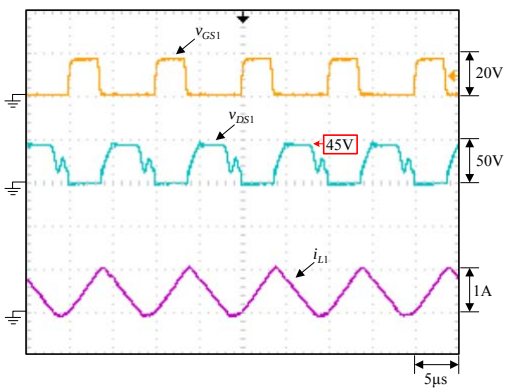

Fig. 11. Waveforms at a light load: (1) v_{GS1}; (2) v_{DS1}; (3) i_{L1}.

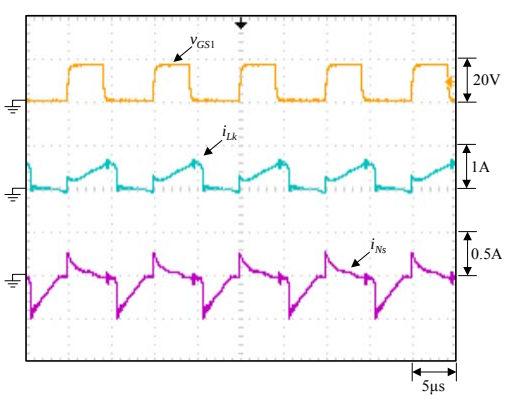

Fig. 12. Waveforms at a light load: (1) v_{GS1}; (2) i_{Lk}; (3) i_{Ns}.

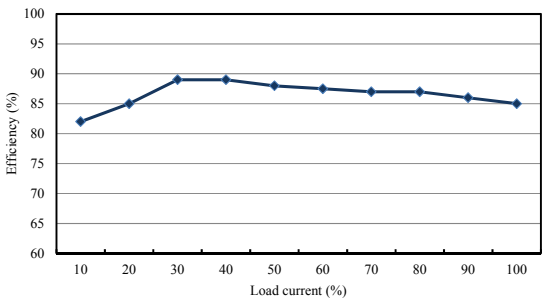

Fig. 13. Efficiency versus load current.

VI. CONCLUSION

An isolated high step-up converter with continuous input current is presented. The proposed converter comprises a boost converter, a coupled inductor, and a charge pump capacitor cell. Hence, a high step-up voltage gain can be achieved with a relatively low duty cycle. Moreover, the leakage inductance energy can be recycled to the output capacitor of the boost converter with the LC snubber and then transferred to the output load. Therefore, the voltage spike of the switch can be clamped at a low value, and the switch with a low turn-on resistance can be used. In doing so, efficiency is improved. The operating principle analyses, designs, and experimental results are provided to verify the effectiveness of the proposed converter.

REFERENCES

[1] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "Power decoupling techniques for micro-inverters in PV systems-a review," *IEEE ECCE'10*, pp. 3235-3240, 2010.

[2] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configurations," *IEEE Trans. Power Electron.*, Vol. 23, No. 3, pp. 1320-1333, May 2008.

[3] M. David, N. Scholten, and W. L. Soong, "Mirco-inverters in small scale PV systems: a review and future directions," *IEEE AUPEC'13*, pp. 1-6, 2013.

[4] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Norwell: KLuwer Academic Publishers, 2001.

[5] K. I. Hwu and T. J. Peng, "High-voltage-boosting converter with charge pump capacitor and coupling inductor combined with buck-boost converter," *IET Power Electron.*, Vol. 47, No. 1, pp. 177-188, Jan. 2014.

[6] G. M. L. Chu, D. D. C. Lu, and V. G. Agelidis, "Flyback-based high step-up converter with reduced power processing," *IET Power Electron.*, Vol. 5, No. 3, pp. 349-357, Mar. 2012.

[7] S. Dwari and L. Parsa, "An efficient high-step-up interleaved dc-dc converter with a common active clamp," *IEEE Trans. Power Electron.*, Vol. 26, No. 1, pp. 66-78, Jan. 2011.

[8] K. I. Hwu and Y. T. Yau, "High step-up converter based on coupling inductor and bootstrap capacitors with active clamping," *IEEE Trans. Power Electron.*, Vol. 29, No. 6, pp. 2655-2660, Jun. 2014.

[9] Y. Berkovich and B. Axelrod, "High step-up dc-dc converter with coupled inductor and reduced switch-voltage stress," *IEEE IECON'12*, pp. 453-458, 2012.

[10] K. I. Hwu and W. Z. Jiang, "Voltage gain enhancement for a step-up converter constructed by KY and buck-boost converters," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 4, pp. 1758-1768, Apr. 2014.

[11] Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active network converter with high voltage gain," *IEEE Trans. Power Electron.*, Vol. 29, No. 6, pp. 2959-2968, Jun. 2014.

[12] K. I. Hwu and W. C. Tu, "Voltage-boosting converters with energy pumping," *IET Power Electron.*, Vol. 5, No. 2, pp. 185-195, Feb. 2012.

[13] Y. J. A. Alcazar, D. de Souza Oliveira, F. L. Tofoli, and R. P. Torrico-Bascope, "DC-DC nonisolated boost converter based on the three-state switching cell and voltage multiplier cells," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 10, pp. 4438-4449, Oct. 2013.

[14] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated dc-dc converters," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, pp. 871-887, Mar. 2008.

[15] M. Pavlovsky, S. W. H. de Hann, and J. A. Ferreira, "Reaching high power density in multikilowatt dc-dc converters with galvanic isolation," *IEEE Trans. Power Electron.*, Vol. 24, No. 3, pp. 603-612, Mar. 2009.

[16] G. Spiazzi, P. Mattavelli, and C. Alessandro, "High step-up ratio flyback converter with active clamp and voltage multiplier," *IEEE Trans. Power Electron.*, Vol. 26, No. 11, pp. 603-612, Nov. 2011.

[17] J. H. Jang, D. H. Kim, J. W. Seo, and J. H. Park, "Series-connected isolated switched-capacitor tapped-inductor boost converter," *IEEE PEDS'13*, 277-279, 2013.

[18] M. Kasper, M. Ritz, D. Bortis, and J. W. Kolar, "PV panel-integrated high step-up high efficiency isolated GaN dc-dc boost converter," *IEEE INTELEC'13*, pp. 1-7, 2013.

[19] D. Murthy-Bellur and M. K. Kazimierczuk, "Two-switch flyback PWM DC-DC converter in discontinuous-conduction mode," *Int. J. Circ. Theor. Appl.*, Vol. 39, No. 8, pp. 849-864, Aug. 2011.

[20] D. Murthy-Bellur and M. K. Kazimierczuk, "Two-switch flyback PWM DC-DC converter in continuous-conduction mode," *Int. J. Circ. Theor. Appl.*, Vol. 39, No. 11, pp. 1145-1160, Nov. 2011.

[21] K. I. Hwu, W. Z. Jiang, and J. Y. Chien, "Isolated high voltage-boosting converter derived from forward converter," *Int. J. Circ. Theor. Appl.*, Vol. 44, No. 2, pp. 280-304, Feb. 2016.

[22] K. I. Hwu, Y. T. Yau, and L. L. Lee, "Powering LED using high-efficiency SR flyback converter," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 1, pp. 376-386, Jan./Feb. 2011.

[23] K. Patidar and A. C. Umarikar, "A step-up PWM DC-DC converter for renewable energy applications," *Int. J. Circ. Theor. Appl.*, Vol. 44, No. 4, pp. 817-832, Apr. 2016.

[24] T. Takiguchi and H. Koizumi, "Quasi-Z-source DC-DC converter with voltage-lift technique," *IEEE IECON'13*, pp. 1191-1196, 2013.

[25] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "Quasi-Y-source boost DC-DC converter," *IEEE Trans. Power Electron.*, Vol. 30, No. 12, pp. 6514-6519, Dec. 2015.

[26] K. Patidat and A. C. Umarikar, "High step-up pulse-width modulation DC-DC converter based on quasi-Z-source

topology," *IET Power Electron.*, Vol. 8, No. 4, pp. 477-488, Apr. 2015.
[27] C. T. Pan, M. C. Cheng, C. M. Lai, and P. Y. Chen, "Current-ripple-free module integrated converter with more precise maximum power tracking control for PV energy harvesting," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 1, pp. 271-278, Jan./Feb. 2015.
[28] K. I. Hwu, W. Z. Jiang and Y. T. Yau, "An isolated high step-up converter with continuous input current and LC snubber," *IEEE APEC'16*, pp. 2415-2421, 2016.
[29] "L6565 Quasi-resonant controller," *ST Tech. Rep.*, 2003.

Kuo-Ing Hwu was born in Taichung, Taiwan, on August 24, 1965. He received his B.S. and Ph.D. degrees in Electrical Engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1995 and 2001, respectively. From 2001 to 2002, he was the Team Leader of the Voltage-Regulated Module (VRM) at AcBel Company. From 2002 to 2004, he was a Researcher at the Energy and Resources Laboratories, Industrial Technology Research Institute. He is currently a Professor at the Institute of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan, where he served as the Chairman of the Center for Power Electronics Technology from 2005 to 2006. His current research interests include power electronics, converter topology, and digital control. Dr. Hwu has been a member of the Program Committee of the IEEE Applied Power Electronics Conference and Exposition since 2005. He has also been a member of the Technical Review Committee of the Bureau of Standards, Metrology, and Inspection since 2005. Since 2008, he has been a member of the IET.

Wen-Zhuang Jiang was born in Changhua, Taiwan, on May 09, 1989. He received his B.S. and M.S. degrees in Electrical Engineering from National Taipei University of Technology, Taipei, Taiwan, in 2011 and 2013, respectively. Currently, he is working toward his Ph.D. degree at National Taipei University of Technology. His research interests include power electronics and digital control.