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# A Power Regulation and Harmonic Current Elimination Approach for Parallel Multi-Inverter Supplying IPT Systems

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## Abstract

The single resonant inverter is widely employed in typical inductive power transfer (IPT) systems to generate a high-frequency current in the primary side. However, the power capacity of a single resonant inverter is limited by the constraints of power electronic devices and the relevant cost. Consequently, IPT systems fail to meet high-power application requirements, such as those in rail applications. Total harmonic distortion (THD) may also violate the standard electromagnetic interference requirements with phase shift control under light load conditions. A power regulation approach with selective harmonic elimination is proposed on the basis of a parallel multi-inverter to upgrade the power levels of IPT systems and suppress THD under light load conditions by changing the output voltage pulse width and phase shift angle among parallel multi-inverters. The validity of the proposed control approach is verified by using a 1,412.3 W prototype system, which achieves a maximum transfer efficiency of 90.602%. Output power levels can be dramatically improved with the same semiconductor capacity, and distortion can be effectively suppressed under various load conditions.

**Key words:** Inductive power transfer (IPT), Parallel multi-inverter, Power regulation, Selective harmonic elimination

## NOMENCLATURE

| | |
|---|---|
| $E$ | DC input voltage of each H-bridge inverter |
| $L_k$ | Link inductance of each inverter |
| $n$ | Number of parallel inverters |
| $i_k$ | Output current of each H-bridge inverter |
| $C_P$ | Compensation capacitance of the primary circuit |
| $i_p$ | Current in the primary coil |
| $L_p$ | Inductance of the primary coil |
| $M$ | Mutual inductance between the primary and secondary coils |
| $L_S$ | Inductance of the secondary coil |
| $C_S$ | Compensation capacitance of the secondary coil |
| $i_S$ | Current in the secondary coil |
| $R_L$ | Equivalent load resistance |
| $U_{out}$ | Output voltage across the load |
| $R_0$ | Reflected resistance of the secondary circuit |
| $(\boldsymbol{A})^*$ | Conjugate operation of **A** |

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## I. INTRODUCTION

Inductive power transfer (IPT) systems are employed in many ultra-clean, ultra-dirty environments as a power provider to transfer power from the primary side to the secondary load side over a moderate air-gap distance through magnetic coupling [1]-[9] on the basis of specific application requirements. The potential advantages of IPT systems include immunity to ice, water, and other chemicals; environmental friendliness; and zero maintenance requirement. In addition, IPT systems have been adopted in a number of applications, including in the wireless charging of biomedical implants [10], mining applications [11], underwater power supply [12], electric vehicles [13]-[20], and railway applications [21], because of their ease of use, environmental sustainability, and

low lifecycle cost.

An IPT system is composed of a high-frequency AC power supply, a resonance tank, magnetic structures for inductive coupling, a pickup in the secondary side, and a rectifier load. The power supply produces an alternating electric current in the primary coil, which in turn produces a time-changing magnetic field. This variable magnetic field induces an electric current (which produces a magnetic field) in the secondary solenoid windings. The induced AC and voltage are then rectified to a direct current (DC) to recharge the battery and/or the load.

Unlike consumer electronic devices, applications such as electric vehicles and rail transit systems require a large amount of power. The transferred power capacity of single inverter-based IPT systems [22]-[23] is restricted by the constraints of power electronic devices, which may be unavailable in the market or too expansive to pursue.

To enhance the capacity of the resonant inverter source, the use of multiple inverters connected in parallel is proposed in [24]-[27]. A parallel connected system for induction heating based on a high-frequency inductor-capacitor-inductor (LCL) resonant inverter is described in [24]. This system requires no additional device for connecting inverters in parallel, and flexible power levels can be achieved by choosing the number of parallel inverters. A phase shift control power regulation approach for multiple LLC resonant inverters for induction heating is presented in [25] to regulate the output power of paralleled inverters by controlling the phases among them. A novel soft-switching high-frequency resonant inverter comprising two half-bridges connected in parallel is described in [26]. By employing a new current phasor control for changing the phase shift angle between two half-bridge inverter units, the output power can be regulated continuously under a wide range of soft-switching operations. A parallel topology, which can achieve high output power levels in a cost-effective manner for IPT systems with LCL-T resonant inverters, is proposed in [27] with high reliability of functioning even when a faulty parallel H-bridge inverter is electronically shut down.

However, low-order harmonics dramatically degrade the performance of some IPT systems, and such issue in harmonics is not effectively addressed by the aforementioned approaches. Safe levels of magnetic field exposure is a strict requirement for IPT systems and is a growing public concern. The maximum allowable field intensity at a given frequency related to the track current in an IPT system with an operating frequency of 20–100 kHz is provided in the guidelines [28] and does not vary with frequency. At the same time, the harmonics in the track current may increase the peak value of the track current, especially under light load conditions. Consequently, field intensity increases significantly that it violates the standards. Therefore, an approach to harmonic reduction should be developed to maintain magnetic field intensity within safe levels.

A novel parallel multi-inverter IPT system is presented in the current study to upgrade the power levels of IPT systems. The phase shift pulse width modulation method employed in parallel inverters is proposed to realize power regulation and selective harmonic elimination. The explicit solutions against phase shift angle and pulse width are given according to the constraint of the selective harmonic elimination equation and the required power to avoid solving the non-linear transcendental equation. Thus, the proposed method is suitable for real-time applications, especially for IPT systems with high operation frequency.

The remainder of this paper is organized as follows. The basic principle of the parallel multi-inverter IPT system is described in Section II. An analysis of selective harmonic elimination and output power regulation is performed by using the equivalent circuit of the proposed parallel multi-inverter IPT system in Section II. The experimental verifications on selective harmonic elimination, circulating current, and wide-ranging power regulation are carried out by using a 1,412.3 W 20 kHz prototype of an IPT system. The details are presented in Section III. The conclusion is finally drawn in Section IV.

## II. Basic Principle of Parallel Multi-Inverter

### A. Topology Analysis of Parallel Multi-Inverter

The schematic diagram of the proposed parallel multi-inverter series-series (S-S)-tuned IPT system with voltage-fed H-bridge inverters is illustrated in Fig. 1. The inverter is composed of $N$ identical H-bridge inverters connected in parallel. Each H-bridge inverter is connected in series to a link inductor $L_n$. The resonant and compensation capacitor $C_P$ is then connected in series to the parallel H-bridge inverter. The synthesized current flowing through the primary coil $L_P$ establishes magnetic coupling with the secondary coil. The secondary circuit consists of the pick-up coil $L_S$, the compensation capacitor $C_S$, and the load $R_L$.

The H-bridge inverters $\mathrm{H}_1-\mathrm{H}_n$ produce output voltages $u_1-u_n$, which are controlled by changing the phase shift angles and pulse widths in the gate pulse signals. Accordingly, the output power of each H-bridge inverter can be regulated individually. Each inverter is equipped with a protection device composed of two anti-series-connected semiconductors [29] to isolate the fault inverter from the system.

Fig. 2 shows the equivalent circuit whose resonant angular frequency is defined as

$$\omega = \frac{1}{\sqrt{L_0 C_P}} = \frac{1}{\sqrt{L_S C_S}} \tag{1}$$

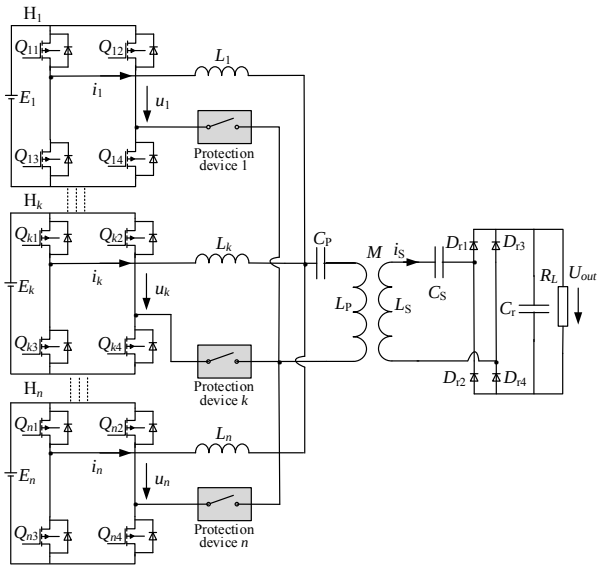


Fig. 1. S-S-tuned IPT system based on a parallel multi-inverter with protection devices.

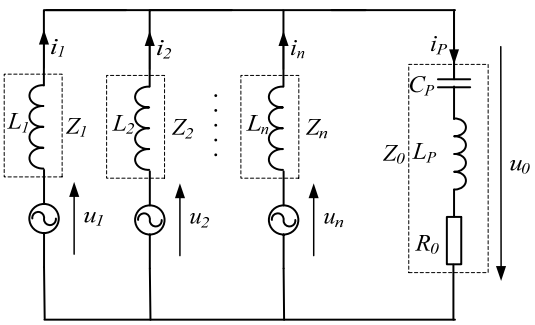


Fig. 2. Equivalent circuit of the IPT system with a parallel multi-inverter.

$$L_0 = L_P + \left(\sum_{n=1}^{N} \frac{1}{L_n}\right)^{-1} \tag{2}$$

To simplify the analysis of the operating principle of the proposed parallel multi-inverter system, we let $L_n = L$ and substitute (2) into (1). The operating angular frequency of the inverter can be expressed as

$$\omega = \frac{1}{\sqrt{\left(L/N + L_P\right)C_P}} \tag{3}$$

$$\begin{cases} \dot{U}_1(k) = \dot{I}_1(k)\cdot Z_1(k) + \dot{U}_0(k) \\ \quad\vdots \\ \dot{U}_N(k) = \dot{I}_N(k)\cdot Z_N(k) + \dot{U}_0(k) \\ \dot{U}_0(k) = Z_0(k)\cdot \sum_{n=1}^{N} \dot{I}_N(k) \end{cases} \tag{4}$$

where

$$Z_0(k) = R_0 + jk\omega L_P + 1/(jk\omega C_P) = R_0 + j\omega(NL_Pk^2 - L - NL_P)/(Nk)$$

and

$Z_1(k) = Z_N(k) = Z_n(k) = jk\omega L = Z(k)$ .

The current of each branch and the track current can be derived by

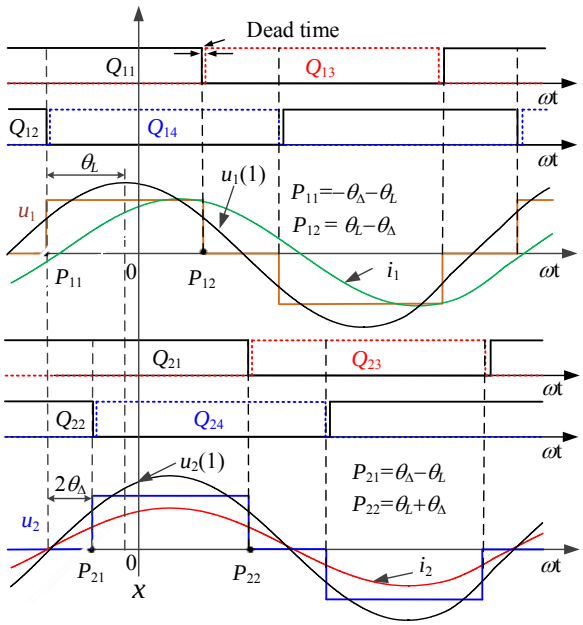


Fig. 3. Output voltage and current waveform of the inverters.

$$\dot{I}_n(k) = \frac{\left[N\cdot Z_0(k) + Z(k)\right]\cdot \dot{U}_n(k) - Z_0\cdot \sum_{n=1}^{N} \dot{U}_n(k)}{Z(k)^2 + N\cdot Z(k)\cdot Z_0(k)} \tag{5}$$

$$\dot{I}_p(k) = \sum_{n=1}^{N} \dot{I}_n(k) = \frac{\sum_{n=1}^{N} \dot{U}_n(k)}{Z(k) + N\cdot Z_0(k)} \tag{6}$$

According to [22], the reflected impedance of the secondary circuit under resonant conditions becomes purely resistive; it can be derived by

$$R_0 = \frac{\omega^2 M^2 \pi^2}{8R_L} \tag{7}$$

### *B. Topology Analysis of Parallel Multi-Inverter*

*1) Waveform Analysis of Voltage Source*: The operating waveforms of the output voltages of the two H-bridge inverters are two identical staircases with a phase shift, as depicted in

Fig. **3**. A coordinate system is constructed accordingly. Line x is the symmetrical center line of the staircase waveform. The origin is chosen at the point where line x and the abscissa ( $\omega t$ ) intersect. To simplify the notation, we denote the pulse width of the staircase as $2\theta_L$ and the phase shift angle between the two staircases as $2\theta_\Delta$. $T_S$ is the period of the fundamental voltage. The current changing rate caused by two parallel inverters with opposite output voltages is twice as large as that with one inverter with zero output, as shown in the following equation.

$$\frac{di}{dt} = \frac{u_1 - u_2}{L_1 + L_2} = \pm\frac{E}{L} \tag{8}$$

Therefore, $\theta_\Delta$ and $\theta_L$ must meet the restriction.

$$\theta_\Delta + \theta_L \le \frac{\pi}{2} \tag{9}$$

The output voltage $u_i(t)$ ( $i$ =1, 2 ) of each H-bridge inverter in one operation cycle is defined as

$$u_i(t) = \begin{cases} E, & \omega t \in [-\theta_L, \theta_L] - (-1)^i \theta_\Delta \\ -E, & \omega t \in [-\theta_L, \theta_L] - (-1)^i \theta_\Delta + \pi \\ 0, & otherwise. \end{cases} \tag{10}$$

After applying Fourier transformation to (10), the $k^{th}$-order harmonic phasor is given by

$$\begin{aligned} \dot{U}_i(k) = \frac{\sqrt{2}}{T_S}\Bigg( & \int_{\frac{-\theta_L+(-1)^i\theta_\Delta}{2\pi}\cdot T_S}^{\frac{\theta_L+(-1)^i\theta_\Delta}{2\pi}\cdot T_S} E\cdot e^{\frac{-j2\pi kx}{T_S}}\,dx \\ & + \int_{\frac{-\theta_L+(-1)^i\theta_\Delta+\pi}{2\pi}\cdot T_S}^{\frac{\theta_L+(-1)^i\theta_\Delta+\pi}{2\pi}\cdot T_S} -E\cdot e^{\frac{-j2\pi kx}{T_S}}\,dx\Bigg) \\ = & \begin{cases} \dfrac{2\sqrt{2}E\sin(k\theta_L)\cdot e^{-jk(-1)^i\theta_\Delta}}{k\pi} & (k \text{ is an } odd \text{ } number) \\ 0 & (k \text{ is an } even \text{ } number) \end{cases} \end{aligned} \tag{11}$$

*2) Harmonic* Analysis: The DC bus voltage is not guaranteed to be the same in practice. Take for example $E_2$=$E$ , $E_1$=(1+$\alpha$)$E$ , and $N$=2. By applying (11) to (6), we obtain

$$\dot{I}_p(k) = \frac{2\sqrt{2}E\sin(k\theta_L)[(\alpha+2)\cos(k\theta_\Delta) + i\alpha\sin(k\theta_\Delta)]}{k\pi[Z(k)+2Z_0(k)]} \tag{12}$$

Let $k=1$ . Then,

$$\dot{I}_P(1) = \frac{2\sqrt{2}E\sin(\theta_L)[(\alpha+2)\cos(\theta_\Delta) + i\alpha\sin(\theta_\Delta)]}{\pi(j\omega L + 2R_0)} \tag{13}$$

Let $k=3$ . Then,

$$\dot{I}_P(3) = \frac{2\sqrt{2}E\sin(3\theta_L)[(\alpha+2)\cos(3\theta_\Delta) + i\alpha\sin(3\theta_\Delta)]}{3\pi(j3\omega L + 2R_0)} \tag{14}$$

This research focuses mainly on eliminating the third-order harmonics because low harmonics exert a significant influence on loads with resonant filter characteristics, that is, letting the third-order harmonic phasor be equal to zero. Thus, the harmonic elimination equation is provided by

$$\frac{2\sqrt{2}E\sin(3\theta_L)[(\alpha+2)\cos(3\theta_\Delta) + i\alpha\sin(3\theta_\Delta)]}{k\pi(j3\omega L + 2R_0)} = 0 \tag{15}$$

When the DC bus voltages are the same, i.e., $\alpha$=0 , the solution for (15) is given by

$$\cos(3\theta_\Delta)\sin(3\theta_L) = 0 \tag{16}$$

Two solutions are derived with (16): (I) $\theta_L = \pi/3$ and (II) $\theta_\Delta = \pi/6$ . That is to say, when satisfying one of the two conditions, the third-order harmonic current can be eliminated theoretically with the same DC bus voltage.

TABLE I
DESIGN SPECIFICATIONS AND CIRCUIT PARAMETERS OF IPT PROTOTYPE

| Parameters | Value |
|---|---|
| DC voltage of the H-bridge inverter, *E/V* | 150 |
| Inverter frequency, *f/kHz* | 20 |
| Inductance of the primary coil, $L_P$/*uH* | 186.78 |
| Link inductance of $H_1$, $L_1$/*uH* | 304.12 |
| Link inductance of $H_2$, $L_2$/*uH* | 303.87 |
| Resonant compensation capacitance of the primary circuit for two inverters, $C_P$/*nF* | 219.54 |
| Resonant compensation capacitance of the primary circuit for a single inverter, $C'_P$/*nF* | 441.86 |
| Mutual inductance of the primary and secondary coils, *M*/*uH* | 60.04 |
| Inductance of the secondary coil, $L_S$/*uH* | 506.47 |
| Resonant compensation capacitance of the secondary circuit, $C_S$/*nF* | 124.81 |
| Equivalent resistance of the load, $R_L$/Ω | 10 |

Take for example $\alpha$=0 . By applying (11) to (6), we obtain

$$\dot{I}_p'(k) = \frac{2\sqrt{2}E\sin(k\theta_L)\cdot e^{-jk\theta\Delta}}{k\pi R_0} \tag{17}$$

Let $k=1$ . Then,

$$\dot{I}_p'(1) = \frac{2\sqrt{2}E\sin(\theta_L)\cdot e^{-j\theta\Delta}}{\pi R_0} \tag{18}$$

Let $k=3$ . Then,

$$\dot{I}_p'(3) = \frac{2\sqrt{2}E\sin(3\theta_L)\cdot e^{-j3\theta\Delta}}{3\pi R_0} \tag{19}$$

Under condition (I), the third-order harmonic can be eliminated even with the DC bus voltage difference according to (15). The amplitude of the third-order harmonic is a function against $\alpha$ under condition (II).

Here, the detailed performance analysis of the third-order harmonic elimination is provided by setting $\alpha$=5% and $\alpha$=10% .

The design specifications of the experimental setup are listed in Table I. In the experimental evaluation, we assume that the H-bridge inverters share identical circuit parameters and power ratings.

Obviously, the third-order harmonic amplitude of the proposed algorithm is significantly smaller than that of the single inverter approach, which merely changes the pulse width, as shown in Fig. 4 along with the configurations in Table I and (13), (14), (18), and (19). The amplitude of the third-order harmonic (maximum of 0.7 A) of the single inverter approach is considerably larger than that of the proposed algorithm (maximum of 0.02 A). Moreover, the influence of the DC bus voltage difference on the third-order harmonic elimination is negligible.

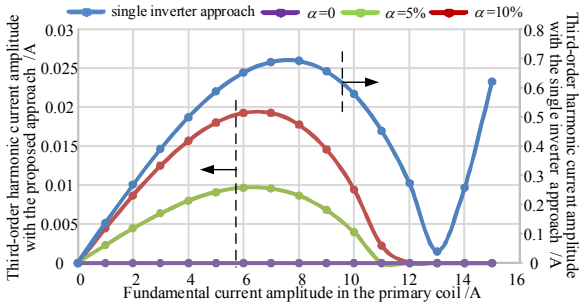


Fig. 4. Comparison of third-order harmonic currents of the primary coil currents of the two approaches.

*3) Power Regulation of IPT System*: Based on (12), the fundamental phasor of the primary coil current is denoted by

$$\dot{I}_P(1)=\frac{2\sqrt{2}E\cos(\theta_\Delta)\sin(\theta_L)}{\pi R_0} \tag{20}$$

According to [22], the output power of the IPT system can be expressed as

$$\begin{aligned}P_{out}&=\frac{\omega^2M^2\pi^2\dot{I}_P(1)\cdot\left(\dot{I}_P(1)\right)^*}{8R_L}\\&=\frac{64E^2R_L\cos^2(\theta_\Delta)\sin^2(\theta_L)}{\pi^4\omega^2M^2}\end{aligned} \tag{21}$$

When fixing $\theta_\Delta=\pi/6$, the third-order harmonic is eliminated. Under the restriction of (9), the range of $\theta_L$ is

$$0\le\theta_L\le\frac{\pi}{3} \tag{22}$$

After substituting $\theta_\Delta=\pi/6$ into (21), the range of output power $P_{out}$ can be given by

$$0\le P_{out}\le\frac{36E^2R_L}{\pi^4\omega^2M^2} \tag{23}$$

Similarly, by fixing $\theta_L=\pi/3$, the range of $\theta_\Delta$ is

$$0\le\theta_\Delta\le\frac{\pi}{6} \tag{24}$$

Consequently, under this condition, the range of $P_{out}$ with harmonic elimination under various settings is provided by

$$\frac{36E^2R_L}{\pi^4\omega^2M^2}\le P_{out}\le\frac{48E^2R_L}{\pi^4\omega^2M^2} \tag{25}$$

When a large amount of power is required, the inverters generate a pulse width ($2\theta_L$) of more than $2\pi/3$ with the same phase to increase the output power while disabling harmonic elimination. By setting $\theta_L=\pi$ and $\theta_\Delta=0$, the output power increases to

$$P_{out}=\frac{64E^2R_L}{\pi^4\omega^2M^2} \tag{26}$$

By changing the values of $\theta_L$ and/or $\theta_\Delta$, the output power of the IPT system $P_{out}$ can be continuously regulated from zero to $48E^2R_L/\pi^4\omega^2M^2$ with harmonic elimination and to $64E^2R_L/\pi^4\omega^2M^2$ without harmonic elimination.

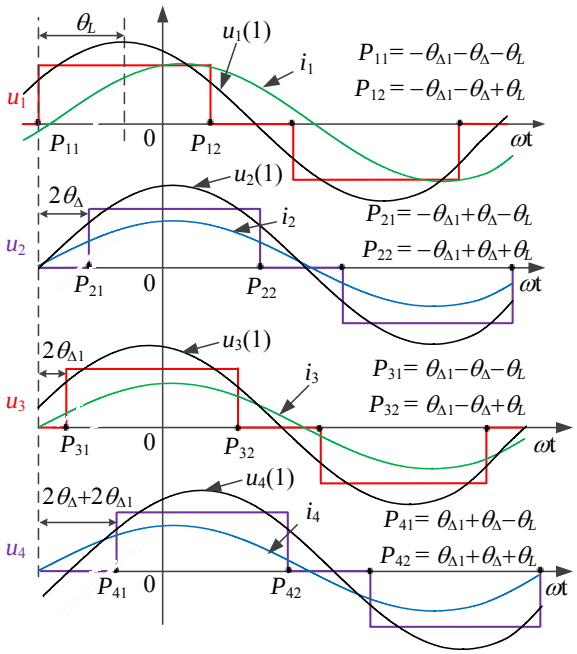


Fig. 5. Output voltage waveform of four-inverter approach.

## C. Multi-Inverter Case Study

On the basis of the two-inverter case study, another two-inverter is considered to form a four-inverter base system. The output voltage waveforms are shown in Fig. 5.

Similar to that in (12), the Fourier transformations of the output voltages are described as

$$\dot{U}_1(k)=\begin{cases}\dfrac{2\sqrt{2}E\sin(k\theta_L)\cdot e^{-jk[\theta_\Delta-\theta\Delta1]}}{k\pi} & (k\ is\ an\ odd\ number)\\ 0 & (k\ is\ an\ even\ number)\end{cases}$$

$$\dot{U}_2(k)=\begin{cases}\dfrac{2\sqrt{2}E\sin(k\theta_L)\cdot e^{-jk[-\theta_\Delta-\theta\Delta1]}}{k\pi} & (k\ is\ an\ odd\ number)\\ 0 & (k\ is\ an\ even\ number)\end{cases}$$

$$\dot{U}_3(k)=\begin{cases}\dfrac{2\sqrt{2}E\sin(k\theta_L)\cdot e^{-jk[\theta_\Delta+\theta\Delta1]}}{k\pi} & (k\ is\ an\ odd\ number)\\ 0 & (k\ is\ an\ even\ number)\end{cases}$$

$$\dot{U}_4(k)=\begin{cases}\dfrac{2\sqrt{2}E\sin(k\theta_L)\cdot e^{-jk[-\theta_\Delta+\theta\Delta1]}}{k\pi} & (k\ is\ an\ odd\ number)\\ 0 & (k\ is\ an\ even\ number)\end{cases} \tag{27}$$

where $\dot{U}_1(k)$ and $\dot{U}_2(k)$ are the output voltages of the first two inverters and $\dot{U}_3(k)$ and $\dot{U}_4(k)$ are the output voltages of the remaining inverters. $2\theta_{\Delta1}$ is the radian difference between the output voltages of the two-inverter system, as shown in Fig. 5. The phasor of the primary coil current can be derived from (6).

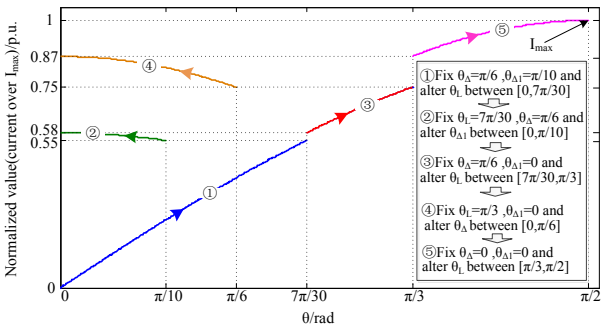


Fig. 6. Primary coil current response of the proposed approach against $\theta_L$, $\theta_\Delta$, and $\theta_{\Delta 1}$.

$$\dot{I}_p(k)=\frac{8\sqrt{2}E\sin(k\theta_L)\cdot\cos(k\theta_\Delta)\cos(k\theta_{\Delta 1})}{\pi\left[Z(k)+N\cdot Z_0(k)\right]} \tag{28}$$

Evidently, $\theta_{\Delta 1}$ can be simply set to zero to double the output power relative to that of the two-inverter system. As discussed previously, as long as $\theta_L$ and $\theta_\Delta$ meet the restriction of the third-order harmonic elimination, the output current of the four-inverter system does not exhibit the third-order harmonic. Through a careful design, another harmonic can be eliminated as well. Take for example the fifth-order harmonic. The harmonic elimination equation is given by

$$\sin(5\theta_L)\cdot\cos(5\theta_\Delta)\cos(5\theta_{\Delta 1})=0 \tag{29}$$

Combining (16) and considering the changing rate of the branch current, the track current of proposed approach against various settings is shown in Fig. 6.

① Setting $\theta_\Delta=\pi/6$ and $\theta_{\Delta 1}=\pi/10$, let $\theta_L$ change from 0 to $7\pi/30$ with the third- and fifth-order harmonic elimination.

② Setting $\theta_\Delta=\pi/6$ and $\theta_L=7\pi/30$, let $\theta_{\Delta 1}$ decrease from $\pi/10$ to 0 with the third-order harmonic elimination.

③ Setting $\theta_\Delta=\pi/6$ and $\theta_{\Delta 1}=0$, let $\theta_L$ change from $7\pi/30$ to $\pi/3$ with the third-order harmonic elimination.

④ Setting $\theta_L=\pi/3$ and $\theta_{\Delta 1}=0$, let $\theta_\Delta$ decrease from $\pi/6$ to 0 with the third-order harmonic elimination.

⑤ Setting $\theta_\Delta=0$ and $\theta_{\Delta 1}=0$, let $\theta_L$ increase from $\pi/3$ to $\pi/2$ without any harmonic elimination. The output power increases to the maximum.

We must clarify that the number of parallel inverters to be used is determined by the following factors.

1. The capacity ($S_{each}$) of each inverter should be slightly greater than $1/N$ of the power demand required by the load with consideration of the circulating current flowing among the inverters. $N$ is the number of parallel inverters. Therefore, when the capacity of each inverter is large, only a few inverters are needed given the same power requirement.

2. The number of parallel inverters is also decided by the number of harmonics to be eliminated. As discussed in this paper, at least $2^{N'}$ inverters are needed to eliminate $N'$ orders of harmonics.

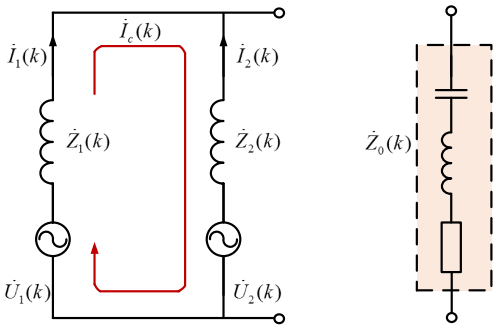


Fig. 7. Circulating current between two inverters.

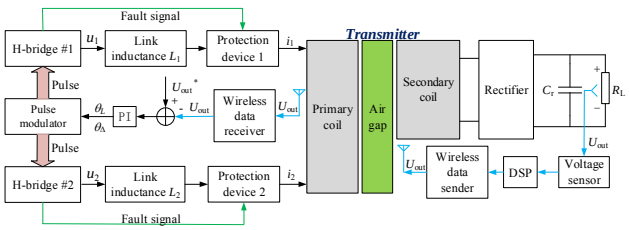


Fig. 8. Control block diagram.

## D. Analysis of Circulating Current

Take the two-inverter-based model for example. According to [30], the circulating current between the first and the second H-bridge inverter (Fig. 7) can be expressed by

$$\dot{I}_c(k)=\frac{\dot{I}_1(k)-\dot{I}_2(k)}{2} \tag{30}$$

By substituting (5) into (30), the fundamental circulating current phasor can be expressed as

$$\dot{I}_c(1)=\frac{2\sqrt{2}E\sin(\theta_\Delta)\sin(\theta_L)}{\pi\omega L} \tag{31}$$

According to (31), the circulating current $\dot{I}_c(1)$ obviously relates to the operating angular frequency $\omega$, the link inductance of the H-bridge inverter $L$, the DC voltage source $E$, and the phases $\theta_L$ and $\theta_\Delta$. When satisfying the elimination conditions ($\theta_\Delta=\pi/6$ or $\theta_L=\pi/3$), the circulating current phasor derived from (31) varies in the range of

$$0\le\dot{I}_c(1)\le\frac{\sqrt{6}E}{2\pi\omega L} \tag{32}$$

Therefore, by choosing proper link inductors and by enlarging the value of link inductance, the circulating current between two inverters is effectively controlled.

## E. Control Diagram

The control block diagram is shown in Fig. 8. The DC load voltage is sent to the controller in the primary side via a wireless data sender. The load voltage and reference voltage

are treated as inputs to the PI controller to yield the control parameters $\theta_L$ and $\theta_\Delta$, which are used to generate the pulse width for the H-bridge inverter.

If any inverter becomes faulty, then its fault signal is sent to the controller to isolate this branch and thereby ensure that the other parts of the system work continuously. In this way, reliability is improved dramatically. The inverters do not perform the harmonic elimination method, and they work under the condition in which their output voltages are controlled to be in phase with the same pulse width.

## III. Experimental Results

### A. Prototype System

To validate the proposed approach, we construct an experimental IPT prototype in the laboratory. The prototype comprises two identical H-bridge inverters connected in parallel and is designed to operate up to 1412.3 W in the experiment. Its functions include selective harmonic elimination and power regulation by changing the output voltage pulse width and phase shift angles.

The exterior appearance of the experimental setup is shown in Fig. 9 and Fig. 10. The TMS320F28335 digital signal processing unit (DSP, Texas Instrument) is used to generate the gate pulse signals for the semi-conductors. The primary coil (L: 32 cm, W: 31.1 cm) on the bottom and the secondary coil (L: 24 cm, W: 31.1 cm) on top are made of U-shaped ferrite. The distance between the primary coil and the secondary coil is about 10 cm. The two coils are mounted to the acrylic board for mechanical support. MOSFETs (AP80N30W) and a gate driver (CONCEPT-2SC0108T2A0-17) are adopted for the H-bridge inverters. The DSP unit is utilized as the controller of the IPT system to achieve control and protection functions among others.

The two H-bridge inverters are separately powered by two isolated DC supplies, and their AC outputs are connected in parallel to provide transmitting current in the primary coil compensated by a series capacitor. An electronic load is employed as the secondary load connected to the rectifier.

The experimental waveforms are measured and displayed by using an Agilent MSO-X 4034A scope, which allows built-in harmonic analysis. The efficiency of the system is analyzed with a YOKOGAW WT1800 power analyzer.

### B. Experimental Results

To provide a clear comparison of different operating conditions, we show in Fig. 11 the experimental values of the output power, load consumption, and transmission efficiency of the IPT system against the output power.

The wide-ranging output power regulation can evidently be achieved by changing the phase shift angle and pulse width of the proposed approach and by changing the pulse width of the single inverter approach (Fig. 11). The output powers of the two inverters are approximately the same (about half of that of the single inverter approach) despite their difference resulting from the presence of a phase shift between them. Consequently, a circulating current exists between the two inverters and results in the occurrence of a loss and a decrease in efficiency, as shown in Zones 1 and 2. At Zone 3, the overall efficiency of the proposed approach increases up to 90.602% at an output power of 1,412.3 W. This value is nearly the same as that of the single inverter approach.

The THD of the proposed algorithm is significantly smaller than that of the single inverter approach, and the third-order harmonic of the proposed approach is dramatically suppressed under various output power conditions, as shown in Fig. 12. In Zones 1 and 2, the THD of the track current of

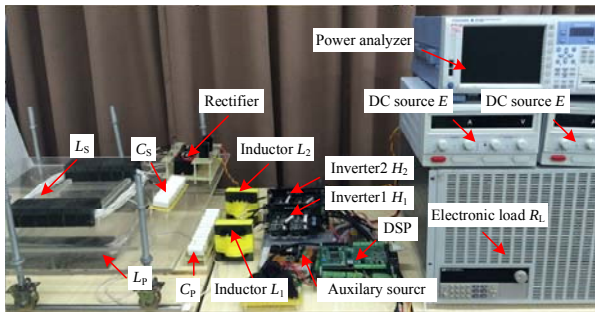


Fig. 9. Exterior appearance of the proposed IPT prototype.

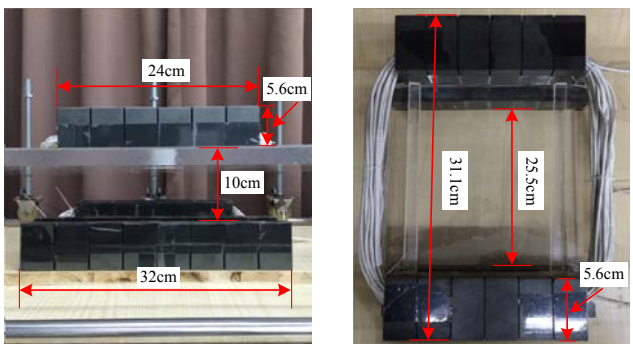


Fig. 10. Primary and secondary coils wound with a Litz wire.

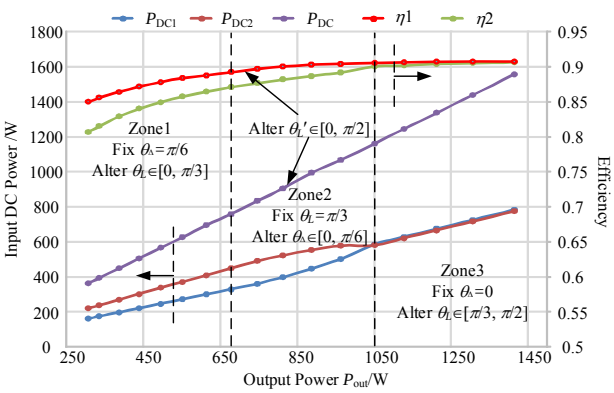


Fig. 11. Input power and overall system efficiency against the output power.

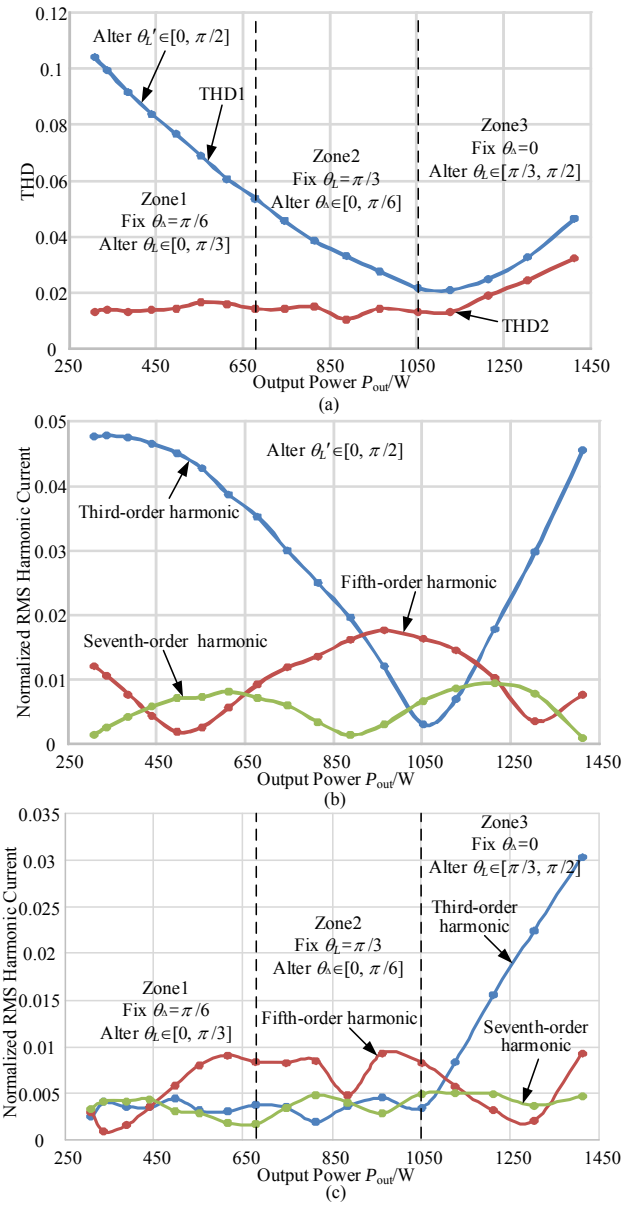


Fig. 12. Comparison of THD and normalized RMS of the primary coil current of the two approaches: (a) THD values of the two approaches, (b) normalized RMS of the primary coil current of the single inverter approach, and (c) normalized RMS of the primary coil current of the proposed approach.

the proposed approach is maintained within 2%, whereas in Zone 3, the THD increases because the proposed approach cannot eliminate the third-order harmonic in this zone. The blue line (THD1) represents the THD value of the single inverter approach, and the red line (THD2) represents the THD value of the proposed algorithm. The third-, fifth-, and seventh-order harmonics are suppressed by the proposed algorithm in Zones 1 and 2 but not in Zone 3, as shown in Fig. 12(b) and (c).

Unlike the single inverter approach, the proposed algorithm can dramatically suppress the third-order harmonic of the

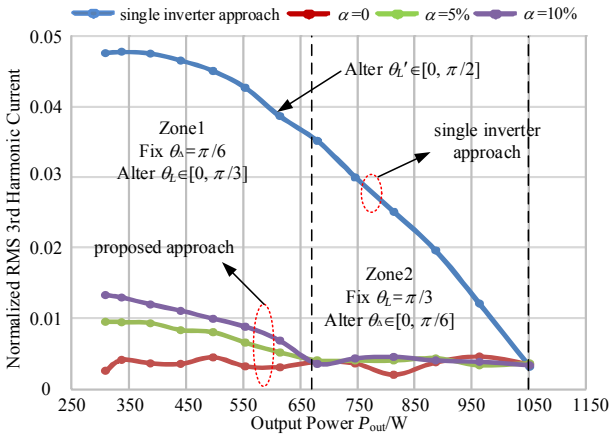


Fig. 13. Comparison of normalized RMS of the third-order harmonic of the primary coil current of the two approaches.

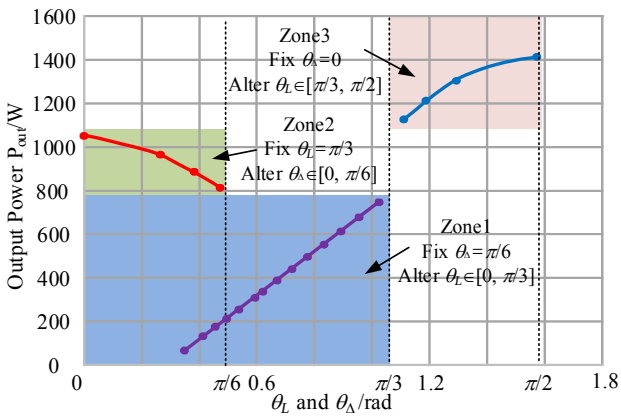


Fig. 14. Output power against $\theta_\Delta$ and $\theta_L$.

experiment even with different DC bus voltages, as shown in Fig. 13. The output power of the experiment measured with the prototype is provided in Fig. 14. The output power can be continuously regulated from almost 0 W to 1,400 W by changing the value of $\theta_L$ and/or $\theta_\Delta$. The comparison of the waveforms of the two approaches indicates that the proposed approach dramatically suppresses the harmonic and nearly eliminates the third-order harmonic. The same result is obtained in the theoretical analysis. The overall efficiency of the proposed approach is about 82.9%, as shown in Fig. 15. The waveforms of the current and voltage of the IPT system, as well as the overall efficiency (90.602%), under the maximum output power point (1,412.3 W) are shown in Fig. 16. Other working points are shown in Fig. 11.

The dynamic response is provided in Fig. 17. The reference voltage of the load changes from 50 V to 70 V and then back to 50 V, as shown in Fig. 17(a). The response of the proposed algorithm is fast, taking about 18 ms to reach 70 V and 17.5 ms to return to 50 V.

The load resistance change test is performed, and the dynamic response of the proposed algorithm is given in Fig. 17(b). The proposed algorithm converges to 50 V in 16 ms

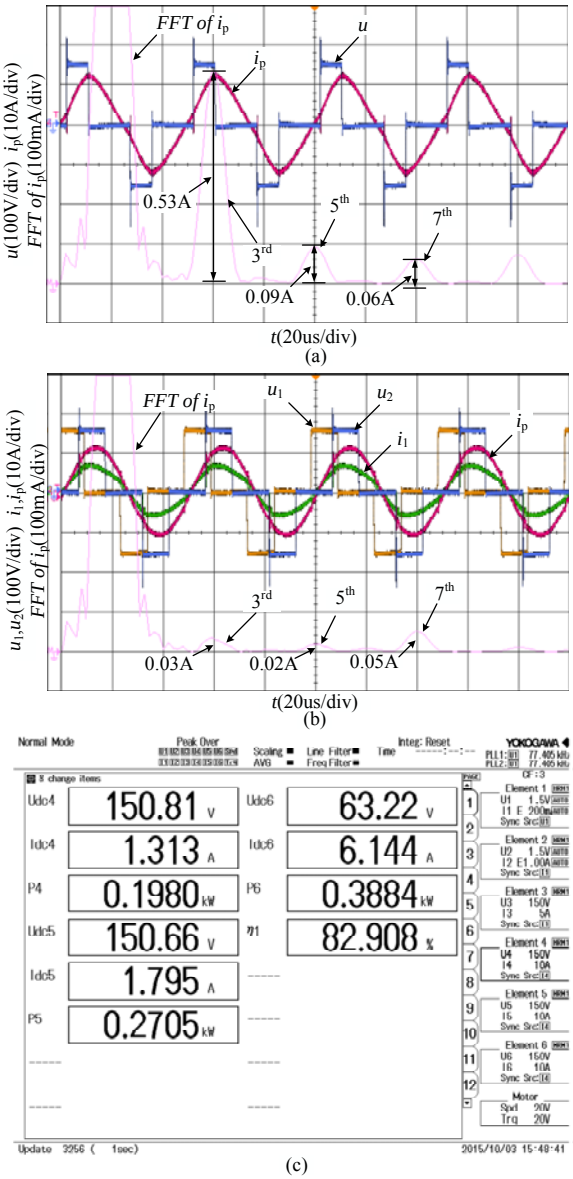


Fig. 15. Measurement of the key system waveforms of the two approaches at $P_{out}$ = 388.4 W. (a) Waveforms of output voltage, the primary track current, and the harmonic analysis of the single inverter approach. (b) Waveforms of the output voltage, the primary track current, and the harmonic analysis of the proposed approach. (c) Overall efficiency of the proposed approach measured with a power analyzer.

with the load resistance changing from 10 Ω to 8 Ω and in 17 ms with the load resistance changing from 8 Ω to 10 Ω.

The waveforms of the current and voltage of the IPT system are shown in Fig. 18 with the operation of the protection device of inverter 2. At the beginning, the voltage of the load at the secondary side is set to 30 V. When a fault occurs in inverter 2, inverter 2 is cut off by the protection device while inverter 1 continues to operate. After 17 ms, the load voltage returns to 30 V despite the voltage drop. Clearly, the proposed algorithm can remove the faulty H-bridge inverter and improve system reliability.

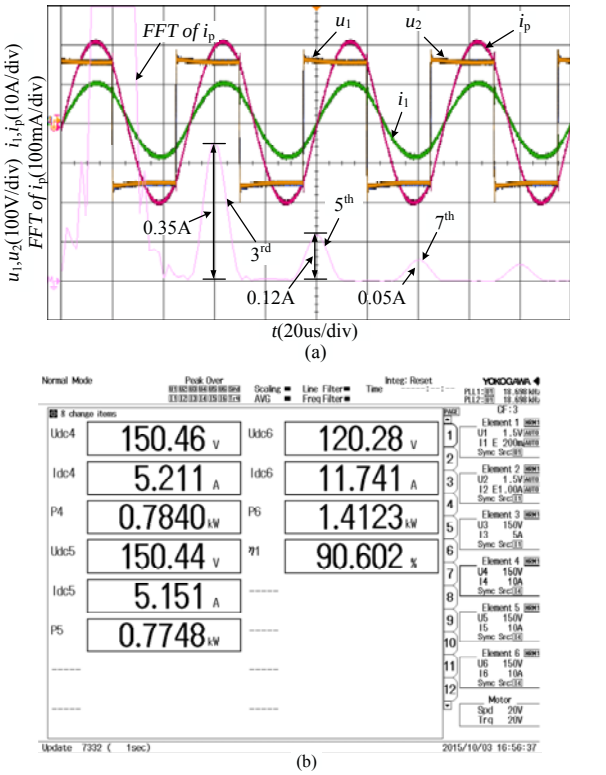


Fig. 16. Measurement of the key system waveforms of the two approaches at $P_{out}$ = 1,412.3 W. (a) Waveforms of output voltage, the primary track current, and the harmonic analysis of the single inverter approach. (b) Waveforms of output voltage, the primary track current, and the harmonic analysis of the proposed approach. (c) Overall efficiency of the proposed approach measured with a power analyzer.

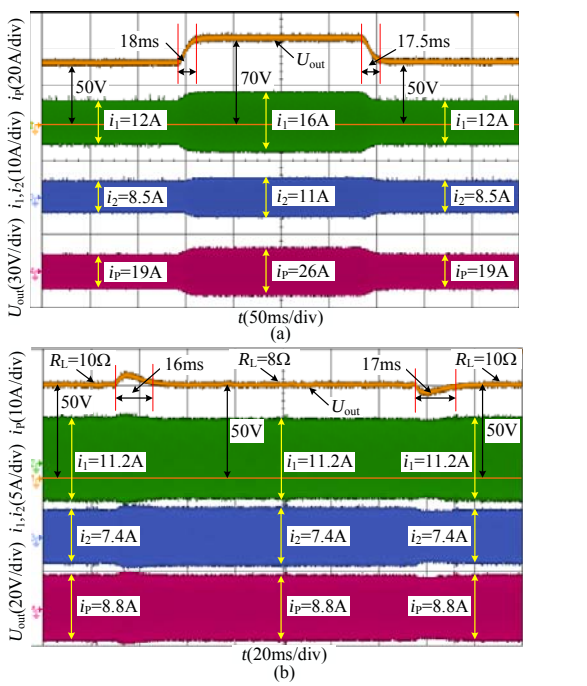


Fig. 17. System response with a step change. (a) Step change of reference voltage from 50 V to 70 V and then back to 50 V. (b) Step change of load resistance from 8 Ω to 10 Ω and then back to 8 Ω.

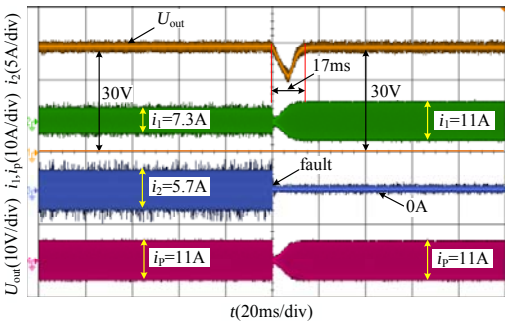


Fig. 18. Waveforms when a fault occurs in H-bridge inverter 2.

## IV. Conclusions

A novel power regulation control approach with selective harmonic elimination based on a parallel multi-inverter for IPT systems is proposed in this work. The operating principle of harmonic elimination and power regulation is explained and described in detail. By changing the output voltage pulse width and the phase shift angle of the inverters, the third-order harmonic current of the primary coil could be eliminated while continuously regulating the IPT output power. A 1,412.3 W experimental prototype is set up and tested. The experimental results verify the performance of the proposed control approach, which is suitable for high-power IPT applications with various power requirements. Moreover, the output of the proposed approach involves a lower harmonic distortion under light load conditions in comparison with that of the single inverter approach. A protection scheme is provided to improve the reliability of the proposed system. The test results also show that the output voltage can be maintained to the desired value even in cases of faults, which are removed by the protection device.

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