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A 32-Gb/s Inductorless Output Buffer Circuit with Adjustable Pre-emphasis in 65-nm CMOS

Tomoki Tanaka[1], Keiji Kishine[1], Akira Tsuchiya[2], Hiromi Inaba[1], and Daichi Omoto[1]

[1] Department of Electronic Systems Engineering, The University of Shiga Prefecture / Shiga, Japan
oz23ttanaka@gmail.com
[2] Department of Communications and Computer Engineering, Kyoto University / Kyoto, Japan

* Corresponding Author: Keiji Kishine

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***Abstract*:** Optical communication systems are rapidly spread following increases in data traffic. In this work, a 32-Gb/s inductorless output buffer circuit with adjustable pre-emphasis is proposed. The proposed circuit consists of an output buffer circuit and an emphasis circuit. The emphasis circuit emphasizes the high frequency components and adds the characteristics of the output buffer circuit. We proposed a design method using a small-signal equivalent-circuit model and designed the compensation characteristics with a 65-nm CMOS process in detail using HSPICE simulation. We also realized adjustable emphasis characteristics by controlling the voltage. To confirm the advantages of the proposed circuit and the design method, we fabricated an output buffer IC with adjustable pre-emphasis. We measured the jitter and eye height with a 32-Gb/s input using the IC. Measurement results of double-emphasis showed that the jitter was 14% lower, and the eye height was 59% larger than single-emphasis, indicating that our proposed configuration can be applied to the design of an output buffer circuit for higher operation speed.

***Keywords*:** 32 Gb/s, Output buffer, Pre-emphasis, 65-nm CMOS

1. Introduction

Optical communication systems are rapidly spread following increases in data traffic. 100G Ethernet was formally standardized in 2010 and is used in core and access networks [1]. In 100G Ethernet, the data speed between an optical transceiver and a host board is 25 Gb/s per channel and four channels are used [2]. In higher speed communication, CML I/O buffers are required for higher speed operation [3, 4]. However parasitic capacitances hinder high-speed operation of the transistor and I/O buffer do not have enough bandwidth. Moreover, by a transmission line outside the IC, degradation of high-frequency components becomes larger than that of low-frequency components, which leads to unstable operation [5]. Signal degradation is a key issue with high speed communication circuits. With this issue, peaking techniques are used in a high-speed communication circuit for compensation [6-10]. The peaking circuit realizes compensation characteristics by emphasizing the high-frequency component. However, the peaking circuit with an inductor occupies a huge area and the circuit tends to be large in size. Therefore, peaking techniques without the inductor are proposed [10, 11].

In this work, to realize higher speed communications, we propose a 32-Gb/s inductorless output buffer circuit with adjustable pre-emphasis. The proposed circuit consists of an output buffer circuit and an emphasis circuit without an inductor. The emphasis circuit emphasizes the high frequency components and adds the characteristics of the output buffer circuit. We design the proposed circuit using a small-signal equivalent-circuit model. Moreover, the emphasis circuit has a control voltage, and the emphasis magnitude can be adjusted against various loads. Then, to confirm the advantages of the proposed circuit and design method, we fabricate an output buffer IC with adjustable pre-emphasis in a 65-nm CMOS process. In an evaluation of the IC, we measure the output buffer eye diagrams with the 32-Gb/s input.

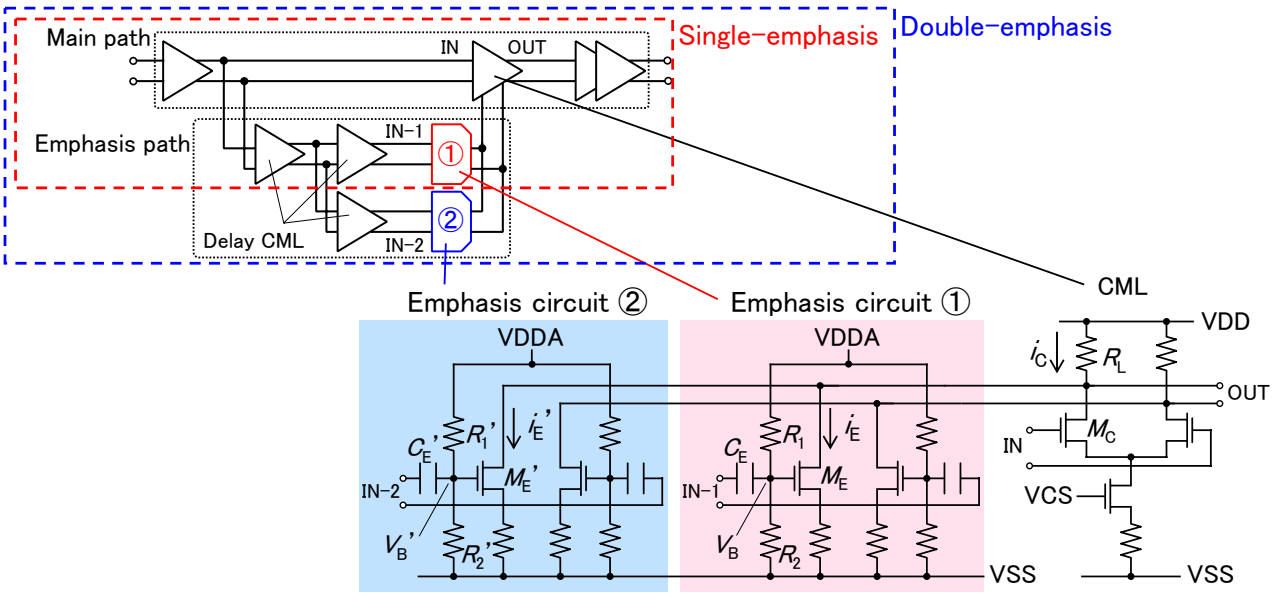

Fig. 1. Block and circuit diagrams of output buffer circuit with pre-emphasis.

2. Block and Circuit Diagrams

2.1 Emphasis Techniques for Signal Degradation

The output buffer is used for signal amplification and impedance matching in signal lines. In high speed communication circuits of several Gb/s and more, a differential signaling is used and the output buffer circuit consists of current mode logic (CML) [3, 4]. However, parasitic capacitance and the transmission line degrade the high-frequency characteristics of the output buffer. This problem leads to unstable operation in the following circuits. To avoid signal degradation, peaking circuits are used to emphasize the gain at the high frequency component. However, the peaking circuit using an inductor occupies huge area and the circuit tends to be large in size. De-emphasis is technique which emphasizes the high frequency component by suppressing a low-frequency component. This technique does not compensate a signal degradation by parasitic capacitances in high speed communication circuits.

We propose an output buffer circuit with adjustable pre-emphasis to realize the compensation characteristics by emphasizing the high-frequency components. The proposed circuit uses de-emphasis and pre-emphasis techniques. Fig. 1 shows the block and circuit diagrams of the proposed circuit. The proposed circuit consists of a main path and an emphasis path.

2.2 Output Buffer Circuit and Emphasis Circuit

The main path consists of four CML circuits. The four CML circuits use a current amplifier for impedance matching in the transmission line. The first stage CML has 100Ω output resistance and a tail current of 4mA, and the last stage CML has 50Ω output resistance and a tail current of 16mA. The supply voltage is VDD and the VCS is a control voltage for adjusting the tail current.

The emphasis path consists of an emphasis circuit and delay CML. The emphasis circuit need to compensate the high-speed operation of the CML and consists of MOSFET and a high pass filter (HPF). By using the HPF, the V_B voltage changes on the basis of the input voltage. Then, on the basis of the V_B voltage, current i_E is generated by M_E. The emphasis circuit does not have a tail current for realizing low power and has differential configurations to match the operation of the CML. The VDDA is a control voltage for adjusting the emphasis characteristics.

2.3 Output Buffer Circuit with Pre-emphasis

The signal generated in the emphasis path is added to the second-CML signal of the main path. The added signal realizes the addition of the current, and only the high-frequency components are emphasized. Then, when the tail current of the CML is i_C and the current generated by the emphasis circuit is i_E as shown Fig. 1, the gain can be expressed by

$$G_C = \frac{v_{CML}+v_{EM}}{v_{IN}} = \frac{R_L(i_C+i_E)}{v_{IN}}. \quad (1)$$

At a low frequency, i_E is zero. Therefore, the gain (1) shows the characteristics of emphasizing the high-frequency components by increasing the current. In this work, we proposed and designed two types of output buffer circuits with pre-emphasis. One is single-emphasis which uses one emphasis circuit, and the other is double-emphasis which uses two emphasis circuits. By using two emphasis circuits, the emphasis performance can be improved, and the proposed circuit can realize appropriate compensation characteristics against various degrees of degradation.

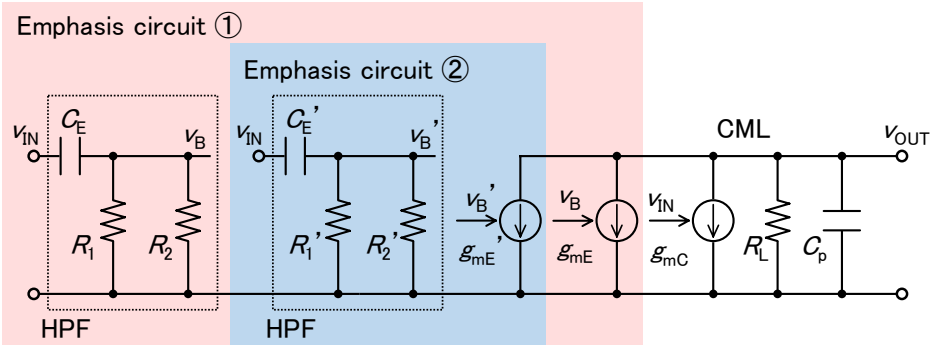

Fig. 2. Small-signal equivalent circuit model.

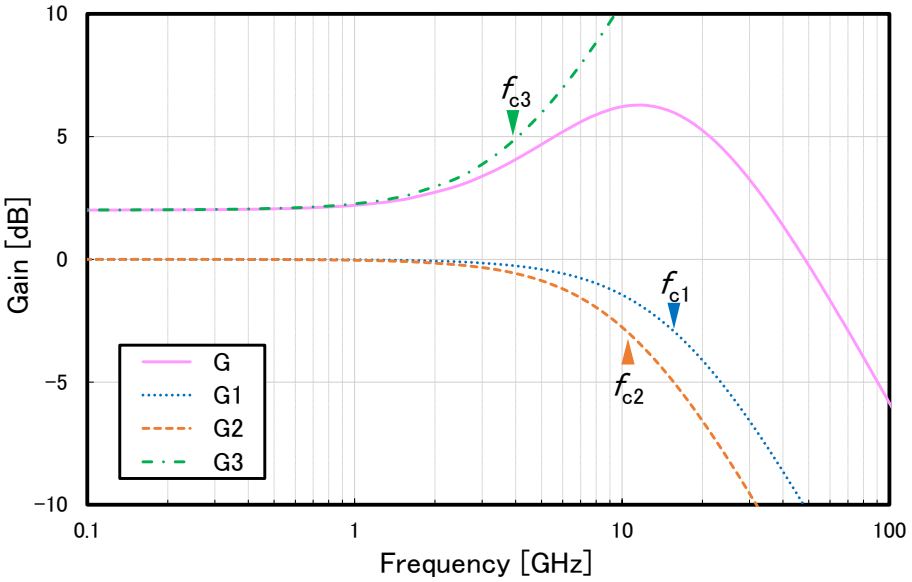

Fig. 3. Gain characteristics of G, G1, G2, and G3.

3. Design Method

In the design of the proposed circuit, we use a small-signal equivalent-circuit model [11]. Fig. 2 shows a small-signal equivalent-circuit model of Fig. 1. MOSFET can be expressed as the parameter g_{mE} which depends on the drain current and the voltage between the gate and source. C_p shows the parasitic capacitance. In the case of single-emphasis, that model is shown by the no-emphasis circuit 2 of Fig. 2. From this model, the gain characteristics are expressed by

$$G_D = \sqrt{\frac{R_L^2\left\{\left(g_{mC}-\omega^2 TT'g\right)^2+\omega^2 X^2\right\}}{\left(1+\left(\omega C_p R_L\right)^2\right)\left(1+(\omega T)^2\right)\left(1+\left(\omega T'\right)^2\right)}},$$
$$\text{where } g = g_{mC}+g_{mE}+g_{mE}',$$
$$X = T\left(g_{mC}+g_{mE}\right)+T'\left(g_{mC}+g_{mE}'\right). \quad (2)$$

T shows the time constant of the HPF and is expressed by

$$T = C_E\left(\frac{R_1 R_2}{R_1+R_2}\right). \quad (3)$$

In addition, considering the two emphasis circuits share the same parameter, the parameter dependence of the gain can be clarified easily. Then, the gain characteristics can be expressed by

$$G = \sqrt{\frac{\left(g_{mC}R_L\right)^2+\left(\omega R_L T\left(g_{mC}+Ng_{mE}\right)\right)^2}{\left(1+\left(\omega C_p R_L\right)^2\right)\left(1+(\omega T)^2\right)}}. \quad (4)$$

N shows the number of emphasis circuit; single-emphasis is N=1, and double-emphasis is N=2. Therefore, Eq. (4) shows the gain of single-emphasis and double-emphasis using one equation. Eq. (4) is divided into three components, G1, G2, and G3.

$$G1 = \sqrt{\frac{1}{\left(1+\left(\omega C_p R_L\right)^2\right)}} \quad (5)$$

$$G2 = \sqrt{\frac{1}{(1+(\omega T)^2)}} \tag{6}$$

$$G3 = \sqrt{(g_{mC}R_L)^2 + \left(\omega R_L T(g_{mC}+Ng_{mE})\right)^2} \tag{7}$$

G1 and G2 express the denominator of Eq. (4), and G3 shows the numerator. Fig. 3 is plotted on a semi-log scale to show G, G1, G2, and G3. G shows the graph of G1 + G2 + G3. G1 shows the characteristics of the CML, and the cutoff frequency is f_{c1}.

$$f_{c1} = \frac{1}{2\pi C_p R_L} \tag{8}$$

G2 and G3 show the characteristics of the emphasis circuit. The cutoff frequency of G2 is f_{c2}, and that of G3 is f_{c3}.

$$f_{c2} = \frac{1}{2\pi T} \tag{9}$$

$$f_{c3} = \frac{1}{2\pi R_L T(g_{mC}+Ng_{mE})} \tag{10}$$

In Eq. (4), the gain at the low frequency can be designed by the parameter g_{mC} and R_L by considering ω is 0. The degradation characteristics of the gain at the high frequency depend on C_p, R_L, and T from (8) and (9). The emphasized characteristics depend on f_{c3}. Therefore, the designing of G3 is an important parameter for determining the emphasized frequency. In this work, we focused on the parameter T and g_{mE} for designing the compensation characteristics.

3.1 The *T* Dependence of the Gain Characteristics

T is the time constant of HPF in the emphasis circuit. To emphasize the high-frequency component, we fix the parameter T at a smaller value to design f_{c3} as larger. Fig. 4 shows the simulation results of the parameter T dependence of the gain characteristics on the output buffer circuit with pre-emphasis. In the case of smaller T, f_{c3} becomes larger, and a frequency of the gain peak becomes higher. However, when T is fixed too small, the effect of emphasis becomes small by degradation of the G1. In the case of larger T, f_{c3} becomes lower, and the gain of low frequency components becomes larger. Excessive emphasis characteristics for the low frequency cause degradation of the signal quality. As shown in the T dependence of the gain characteristics mentioned above, we design the parameter T considering the emphasized frequency and the magnitude in the 65-nm CMOS process using the HSPICE simulation.

3.2 The g_{mE} Dependence of the Gain Characteristics

g_{mE} expresses the trans-conductance of M_E. g_{mE} affects G3, and the effect of emphasis becomes larger by fixing the larger g_{mE}. By increasing the number of finger, the g_{mE} becomes larger. However, the parasitic components become larger, which lead to the degradation of the emphasis performance. To avoid this, we propose increasing the emphasis with two emphasis circuits, which is double-emphasis. By using the two emphasis circuit with different paths, the burden on the previous-stage CML can be smaller.

The advantage of double-emphasis is clarified by using the gain equation. By using the two emphasis circuits, N is 2, which shows that f_{c3} becomes small and the inclination of G3 becomes large. Therefore, the emphasis characteristics of high-frequency components increase. Fig. 5 shows the gain characteristics of the single-emphasis and double-emphasis. From Fig. 5, it is clarified that the effect of emphasis using double-emphasis becomes larger than that of using single-emphasis.

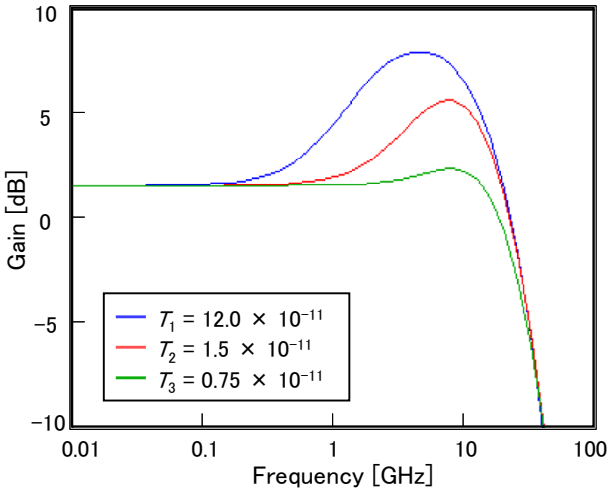

Fig. 4. Simulation results of parameter T dependence of gain characteristics.

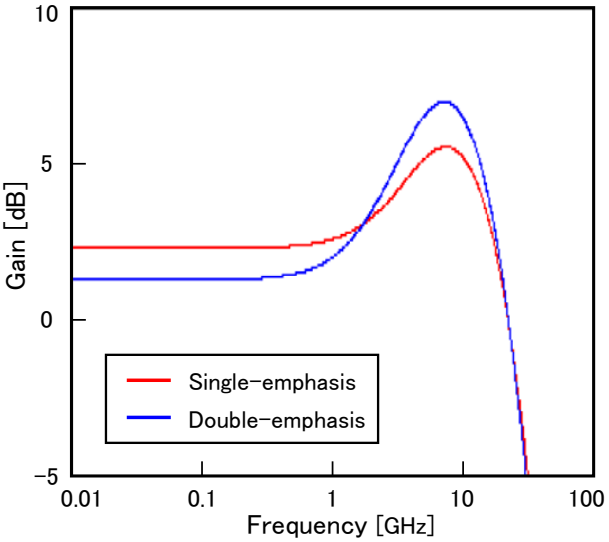

Fig. 5. Simulation results of gain characteristics of single-emphasis and double-emphasis.

3.3 Adjustable Emphasis Magnitude

The proposed circuit has an adjustable emphasis magnitude by using the control voltage VDDA of the emphasis circuit. By using this function, we can adjust the appropriate compensation characteristics against various loads. This function is realized by the changing of the parameter g_{mE}. g_{mE} depends on the bias voltage V_B, and the bias of V_B is expressed by

$$V_B = \frac{R_2}{R_1+R_2}\text{VDDA}. \quad (11)$$

In Eq. (11), V_B depends on the voltage VDDA. Therefore, by controlling the voltage VDDA outside the chip, we can adjust the emphasis magnitude. Fig. 6 shows the voltage VDDA dependence of the gain characteristics using HSPICE simulation. As shown in Fig. 6, the effect of the emphasis becomes larger with a larger voltage VDDA. Fig. 7 shows the voltage VDDA dependence of the emphasis magnitude which defines the gain as 16 GHz minus DC gain. From Fig. 7, we can confirm that the emphasis magnitude of double-emphasis is 2.6 times larger than that of single-emphasis at the 1.2 V VDDA.

4. Experimental Results

To confirm the advantages of the proposed circuit and design method, we fabricated an output buffer IC with pre-emphasis using a 65-nm CMOS process. Fig. 8 shows the chip photograph of the output buffer IC with the double-emphasis. The chip size is 1 mm x 1 mm, which consists of the core circuit, input buffer, input and output pads, DC pads. The area for the core circuit which was the output buffer circuit with double-emphasis was 276 x 117 um^2, and the emphasis path occupied 52% of the core circuit. The core circuit was located near the output pads, so we used the four CMLs for an input buffer. The measured power consumption was 81 mW with VDD = 1.2 V and VCS = 1.0 V.

To evaluate the IC, we measured output eye diagrams observed an oscilloscope (Agilent 86100). The input differential signal is a 32 Gb/s (@2^{31}-1 PRBS data) from a pulse-pattern-generator (PPG). We used the output cable which shows a loss of 7.15 dB @ 16 GHz. The output buffer IC had the control voltage VDDA for adjusting compensation characteristics against signal degradation.

Fig. 9 shows the VDDA dependence of the rms jitter and eye height from output eye diagrams. In the results of the measured jitter, the smaller marks show the approximate rms jitter which was calculated from the measured peak-to-peak jitter with the cursor using the Agilent 86100. The larger marks show the rms jitter from the Agilent 86100. As shown in Fig. 9, the measured jitter using the IC with pre-emphasis was lower than that of without pre-emphasis. When the VDDA was low, the jitter and eye height were improved with a larger voltage VDDA. When the VDDA was large, the jitter and eye height were worsened with a larger voltage VDDA. In the single-emphasis, the minimum jitter was 1.38 ps rms with 1.2 V

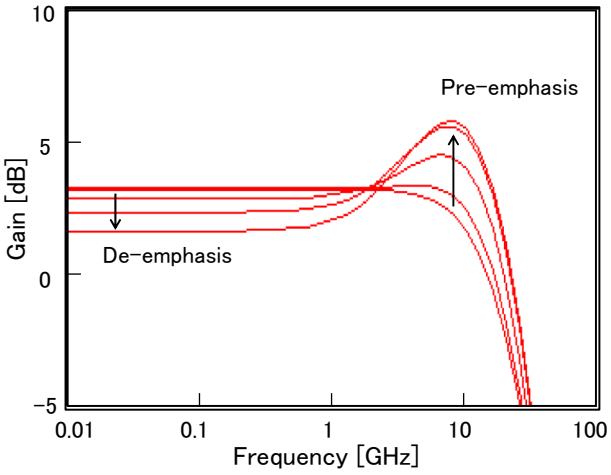

Fig. 6. The gain characteristics dependence of the control voltage, VDDA.

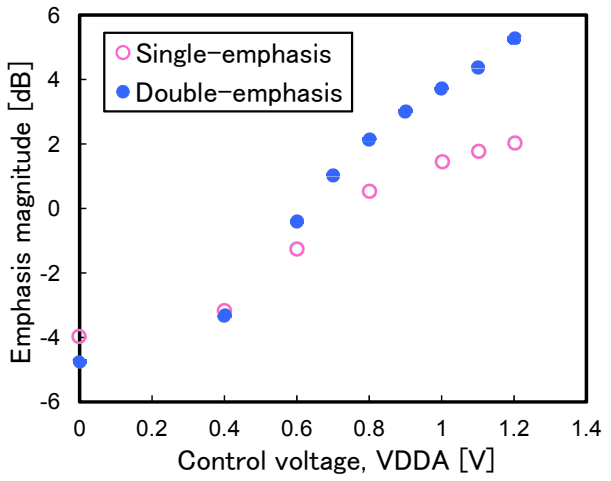

Fig. 7. Emphasis magnitude dependence of control voltage, VDDA.

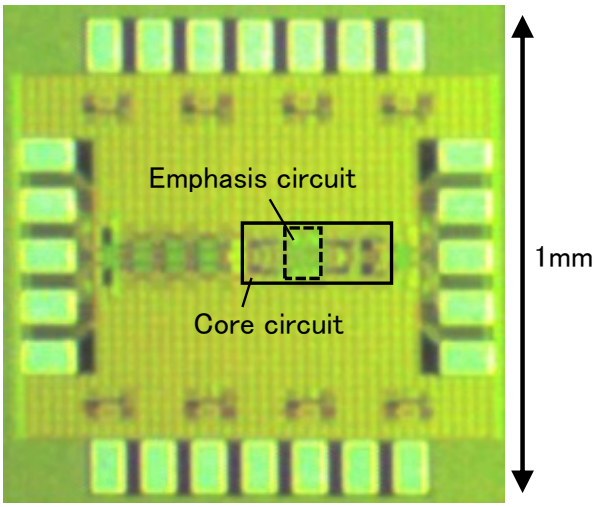

Fig. 8. Chip photograph.

VDDA and the eye height was 12.8 mV. In the double-emphasis, the minimum jitter was 1.19 ps rms with 1.0 V VDDA and the eye height was 20.4 mV. These results

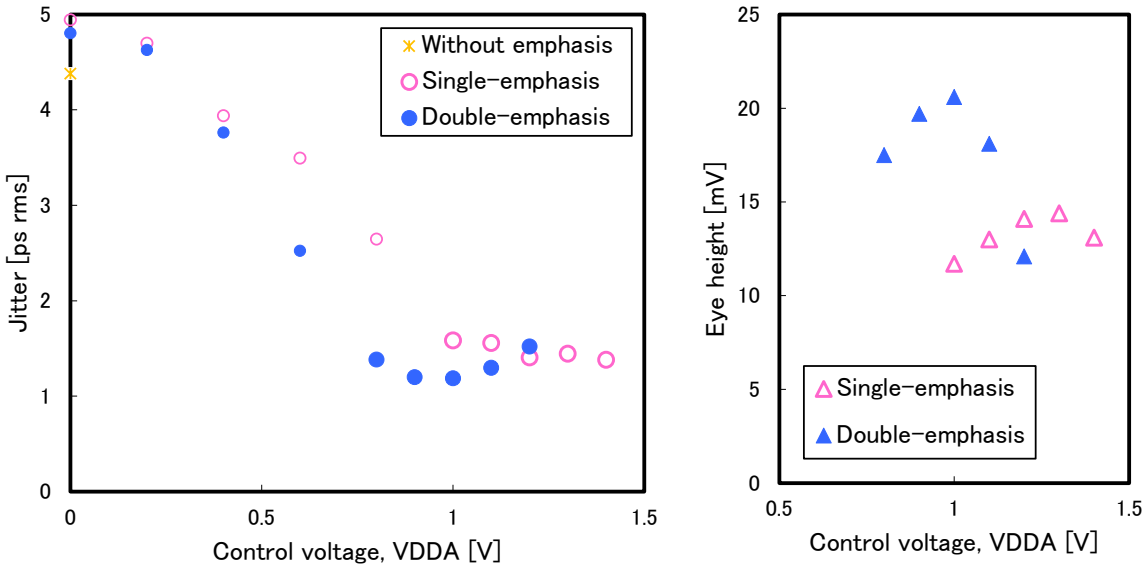

Fig. 9. VDDA dependence of measured jitter and eye height from output eye diagrams at 32-Gb/s input using output buffer IC.

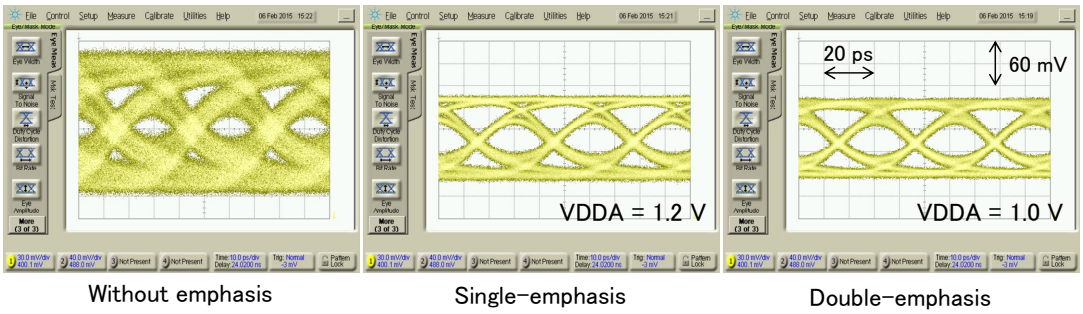

Fig. 10. Measured eye diagrams.

Table 1. Comparison with others

Reference	[8]	[9]	This work
Data rate (Gb/s)	20.4	25 - 28	32
Supply (V)	1.3	3.3/1.0	1.2
Power (mW)	138	137.5	81
Peaking gain	6.5dB@8GHz (Maximum)	7.7dB @12.5GHz	5.3dB @16GHz
Process	90-nm CMOS	65-nm CMOS	65-nm CMOS
Area (mm^2)	0.89 (Chip size)	0.32 (TIA)	0.032 (Core)

showed that the double-emphasis achieved 14% lower jitter and 59% larger eye height than the single-emphasis. Fig. 10 shows the measured eye diagrams of that without emphasis, single-emphasis, and with double-emphasis. The measured and simulated result are summarized in Table 1.

5. Conclusion

In this paper, a 32-Gb/s inductorless output buffer circuit with adjustable pre-emphasis was proposed. The proposed circuit is single-emphasis using a single emphasis circuit and double-emphasis using double emphasis circuits. In the design, we clarified the parameter dependence of the gain characteristics by using a small-signal equivalent-circuit model and designed the proposed circuit using the HSPICE simulation in detail. The emphasis circuit also has a control voltage VDDA to realize the appropriate compensation characteristics against various loads. We fabricated an output buffer IC with adjustable pre-emphasis in a 65-nm CMOS process. In an evaluation of the IC, we measured the jitter and eye height from output eye diagrams using a cable with a loss of 7.15 dB. The IC with the double-emphasis achieves a 14% lower jitter and a 59% larger eye height than the single-emphasis at 32 Gb/s.

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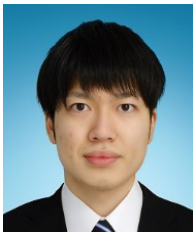
Tomoki Tanaka received the B.S. degree of electronic systems engineering from The University of Shiga Prefecture in 2014. Since the same year, he has enrolled a master's course Graduate school of Engineering in The University of Shiga Prefecture. His research interest is an ultra-high-speed IC design.

Keiji Kishine (M97') received the B.S., and M.S. degrees in engineering science from Kyoto University, Kyoto, Japan, and Ph.D. degree in informatics from Kyoto University, Kyoto, Japan, in 1990, 1992, and 2006, respectively. In 1992, he joined the Electrical Communication Laboratories, Nippon Telegraph and Telephone Corporation (NTT), Tokyo, Japan. He has been engaged in research and design of high-speed, low-power circuits for Gb/s LSIs using Si-bipolar transistors, with application to optical communication systems in NTT System Electronics Laboratories, Kanagawa, Japan. From 1997, he has been worked on research and development of over Gb/s Clock and Data Recovery IC at Network Service Innovation Laboratory in NTT Network Innovation Laboratories, Kanagawa, Japan. He worked at Ubiquitous Interface Laboratory in NTT Microsystems Integration Laboratories, Kanagawa, Japan. Since 2008, he has been an Associate Professor with the school of engineering, Shiga-prefecture University, Shiga, Japan. Dr. Kishine is a member of the IEEE Solid-State Circuits Society (SSCS) and Circuits and Systems (CAS), the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan, the Institute of Electrical Engineers (IEE) of Japan.

Akira Tsuchiya received the B.E., M.E. and Ph.D degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 2001, 2003, and 2005, respectively. Since 2005, he has been an Assistant Professor in the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto niversity. His research interest includes modeling and design of on-chip passive components of high-frequency CMOS, and high-speed analog circuit design. He is a member of the IEICE.

Hiromi Inaba was born in Tokyo, Japan, on September 1, 1950. He received the B.S. and Dr. Eng. degrees from Hokkaido University, Hokkaido, Japan, in 1974 and 1997, respectively. In 1974 he joined Hitachi Research Laboratory, Hitachi, Ltd., Ibaraki, Japan. He has been engaged in research and development on an elevator and steel control system. In 2008, he became a Professor with the school of engineering, The University of Shiga prefecture, Shiga, Japan. Dr. Inaba is a member of the IEEE Industry Applications Society (IAS) and the Institute of Electrical Engineers (IEE) of Japan.



Daichi Omoto received the B.S. degree of electronic systems engineering from The University of Shiga Prefecture in 2014. Since the same year, he has enrolled a master's course Graduate school of Engineering in The University of Shiga Prefecture. His research interest is a high-performance RF communication system.