IEIE Transactions on Smart Processing and Computing, vol. 5, no. 3, June 2016
http://dx.doi.org/10.5573/IEIESPC.2016.5.3.164

A Low Insertion–Loss, High–Isolation Switch Based on Single Pole Double Throw for 2.4GHz BLE Applications

Truong Thi Kim Nga, Dong-Soo Lee, and Kang-Yoon Lee*

College of Information and Communication Engineering, Sungkyunkwan University / Suwon, Korea
{kimnga, blackIds, klee}@skku.edu

* Corresponding Author: Kang-Yoon Lee

Received March 30, 2016; Accepted May 24, 2016; Published June 30, 2016

* *Short paper*

***Abstract*:** A low insertion–loss, high-isolation switch based on single pole double throw (SPDT) for a 2.4GHz Bluetooth low-energy transceiver is presented in this paper. In order to increase isolation, the body floating technique is implemented. Based on characteristics whereby the ratio of the sizes of the shunt and the series transistors significantly affect the performance of the switches, the device sizes are optimized. A simple matching network is also designed to enhance the insertion loss. Thus, the SPDT switch has high isolation and low insertion loss without increasing the complexity of the circuit. The proposed SPDT is designed and simulated in a complementary metal-oxide semiconductor 65nm process. The switch has a 530μm x 270μm area and achieves 0.9dB, 1.78dB insertion loss and 40dB, 41dB isolation of transmission, reception modes, respectively.

***Keywords*:** RF CMOS switches, T/R switch, Low insertion loss, High isolation

1. Introduction

In recent years, the trends in intermediate frequency (IF) and radio frequency (RF) wireless communications are towards low loss, small area, and low cost. In a Bluetooth low energy (BLE) transceiver, all the components are designed for low-power applications. In a conventional RF transceiver, two antennas are used on transmission (TX) and reception (RX) sides to operate as transmitter and receiver antennas, as shown in Fig. 1(a). This leads to a large die size, high power consumption, and high cost.

Most of the recent research uses a transmitter/receiver single pole double throw (SPDT) switch that provides mode selection for the required signal paths. As shown in Fig. 1(b), the SPDT switch allows one antenna to be shared between the transmitter and receiver, instead of two antennas, as in a conventional transceiver. A reduction of one antenna helps minimize die area and power consumption, but also brings to designers new challenges. The insertion loss of the selected SPDT mode needs to be designed with an ultra-low value to reduce the loss of signal in the transmission line. On the other hand, isolation between selected and non-selected modes must be well maintained to eliminate coupling or disturbance by the disabled signal of the enabled one. The switch shown in Fig. 1(b) has to connect the antenna with the TX side and separate the antenna on the RX side completely in TX mode, and then revert in RX mode.

Several approaches have been proposed and implemented to improve the insertion loss and isolation of the SPDT design [1-4]. The approach presented by Yeo and Kwon [1] uses thick anodized aluminum (Al2O3) layers and bare high-power high electron mobility transistors (HEMTs) directly mounted on an aluminum substrate for high electrical isolation. The SPDT structure consists of a power splitter and two pairs of capacitive micro electro-mechanical system (MEMS) shunt switches implemented on a quartz substrate, as presented by Cheng et al. [2]. Both these approaches were applied for an off-chip level. The approaches presented by Wu et al. [3, 4] were applied for an on-chip level. A gallium arsenide (GaAs) high-electron mobility transistor process is applied to construct the SPDT. Due to the electronic characteristics of GaAs devices, the GaAs-based SPDT design has impressive performance, but it also has some drawbacks due to the cost and integration ability with traditional complementary metal-oxide semiconductor (CMOS)

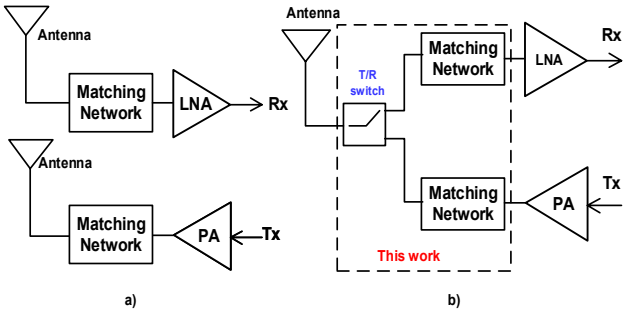


Fig. 1. RF transceiver system diagram (a) separated antenna transceiver, (b) shared antenna transceiver.

processes.

This paper adopts the body floating technique used in the traditional CMOS process to implement a high performance SPDT [5]. The body floating technique is combined with an impedance matching technique to improve insertion loss and isolation of the SPDT. The proposed SPDT-based switch is implemented with standard CMOS 65nm technology. Our proposed SPDT achieved 0.9dB and 1.78dB insertion loss, with 40dB and 41dB isolation in TX and RX modes, respectively.

The switch has to connect the antenna with the TX side and separate the antenna from the RX side completely in TX mode, and then revert. This paper proposes a high-performance SPDT that adopts the body floating technique [1] to improve insertion loss and isolation. The proposed variable switch based on SPDT is implemented in standard CMOS 65nm technology.

This paper is organized as follows. Section 2 describes the proposed variable switch. The layout and simulation results are presented in Section 3. Finally, a conclusion is given in Section 4.

2. Proposed SPDT

The SPDT switch is used to select the signal path of the RF transceiver. It will decide if the signal is connected from the transmitter to the antenna or from the antenna to the receiver using voltage controls V and VB. Thus, the transceiver will operate in TX mode or RX mode, respectively. Fig. 2 shows the proposed switch based on SPDT.

In this proposed SPDT switch, the two main switches are series transistors M1,2, and two others are shunt transistors M3,4. The shunt transistors are used to increase the isolation of the switches in the off-stage. When the switch operates in TX mode, control voltage VB goes high. As exhibited in Fig. 2(b), transistors M1,4 are ON and work as resistors R1,on, R4,on, whereas transistors M2,3 are OFF and work as capacitors C2,off, C3,off. The values of inductor L1 and transistor M3 are calculated in order to achieve the optimal performance. In that case, L1 and M3 become a matching network that includes L1 and C3,off. On the RX path, capacitor C2,off prevents the signal flows from the antenna to the receiver that reduce the insertion loss and increase the isolation. The operation of the switch in RX mode is the same and is illustrated in Fig. 2(c).

In order to reduce the insertion loss of the SPDT switch, the body floating technique is used. A resistor, R, is added in series to the body terminal of each transistor, as shown in Fig. 2(a). According to Wu et al. [4], the insertion loss of the circuit is calculated based on the value of the

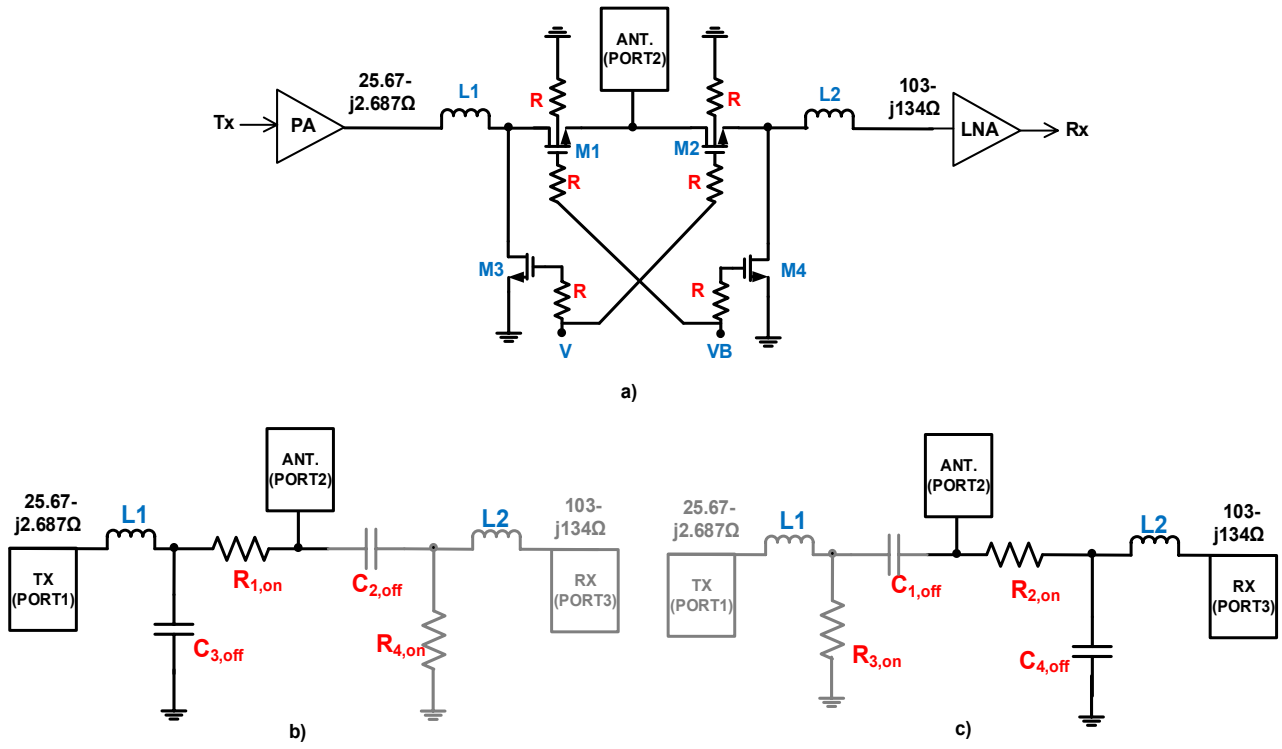
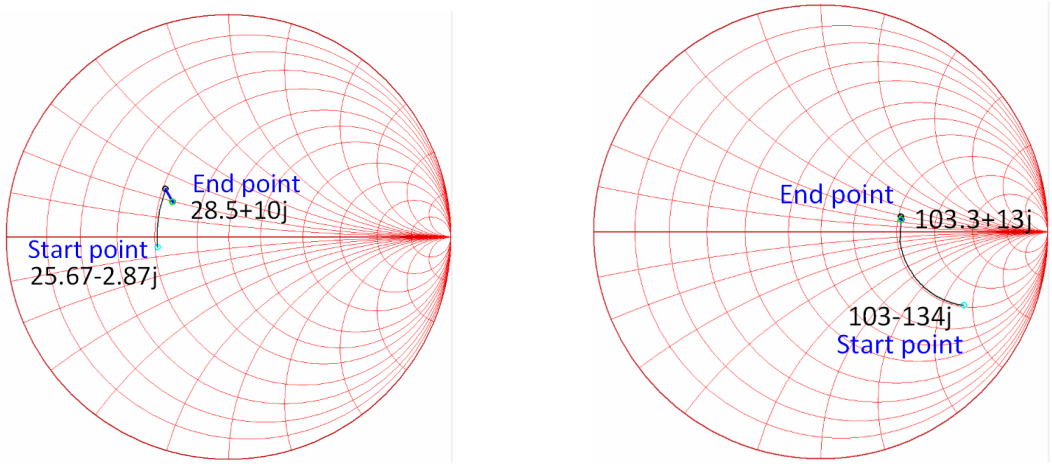


Fig. 2. (a) Proposed SPDT schematic, (b) proposed SPDT in TX mode, (c) proposed SPDT in RX mode.



(a) (b)

Fig. 3. Impedance-matching Smith chart (a) TX mode, (b) RX mode.

Table 1. Device Sizes

Devices	Size
L1 (nH)	1.03
L2 (nH)	9.97
R (KΩ)	15.008
M1 (μm/nm)	640/280
M2 (μm/nm)	400/280
M3 (μm/nm)	576/280
M4 (μm/nm)	80/280

substrate resistance associated with the transistor and the equivalent capacitance of the transistor. Usually, the amount of substrate resistance is very close to Rmax, which gives the insertion loss the maximum value. To improve insertion loss performance, substrate resistance should be either extremely large or approximately zero. As there is always a parasitic resistor, it is impossible to get the substrate resistance close to zero. Therefore, the only way is by increasing the substrate resistor value. In this paper, 15KΩ resistors are chosen using the sizing method.

The size of transistors is optimized to reduce the insertion loss when the channel is on, and increase the isolation when the channel is off. The performance of the switch, especially the insertion loss, is also significantly affected by the ratio of the sizes of the shunt and the series transistor. According to Yeh et al. [5], there are two ways to achieve low insertion loss: (1) using a large size for the series transistor and a small size for the shunt, and (2) simply vice versa. The body floating technique is applied to reduce the leakage of the transistor and contribute to improving insertion loss and the isolation characteristic, and as mentioned above, it still contains impedance mismatch. In an RF system, impedance mismatch between two components causes reflection power at the interface of those components, thus reducing the power that was intended for transfer.

The impedance mismatch problem can be solved simply by applying the L matching network. By assuming the TX part is fully isolated in RX mode, and the RX port

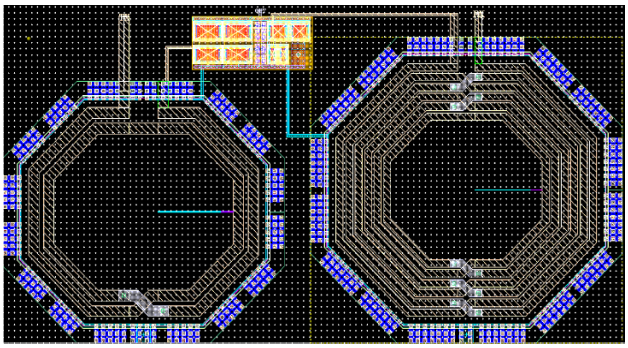


Fig. 4. Proposed SPDT Layout.

is fully isolated in TX mode, the impedance at source terminal M2 and the impedance at drain terminal M1 is measured for the impedance-matching calculation. The L, C values of the matching network in the RX (L2, C4,off) and TX (L1, C3,off) ports are determined by the Schmidt chart method shown in Fig. 3. The impedance of the TX port is matched to the output impedance of the low-noise amplifier (LNA), and the impedance of the RX port is matched to the input of the LNA. The input and output impedance of the LNA specified in Fig. 2 is from the LNA design used in our 2.4GHz Bluetooth low energy transceiver. The sizes of transistors M3 and M4 are optimized to have the drain-source capacitance value (when the channel is off) equal to C3,off and C4,off, respectively. The on-channel resistors M3 (R3,on) and M4 (R4,on) are optimized to increase the impedance of the disabled part of the SPDT operation, and thus, they contribute to increasing the isolation of those parts.

3. Layout and Simulation Results

This work was implemented with CMOS 65nm technology and was simulated using Cadence Spectre. The area of the SPDT switch is 530 μm x 270 μm, which is the layout illustrated in Fig. 4. Fitting the total size of a BLE

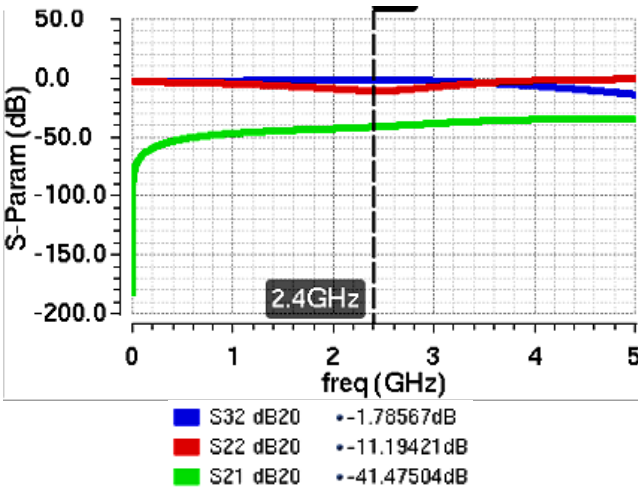


Fig. 5. Insertion Loss and Isolation in RX mode simulation results.

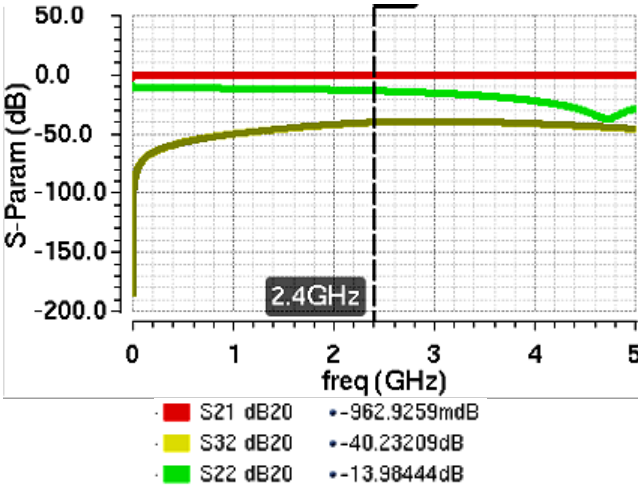


Fig. 6. Insertion Loss and Isolation in TX mode simulation results.

system, our SPDT takes up a small area, but contributes an important role in solving the problems of a system containing double antennas. Compared to using double antennas for the transceiver or using other techniques that require a special CMOS process or an off-chip component, our SPDT design is a better solution.

The port setup for the simulation results, shown in Figs. 5 and 6, is as follows: port 1 is the TX port, port 2 is an antenna, and port 3 is the RX port. The insertion loss S(2,1) in TX mode is better than S(2,3) in RX mode due to the output impedance of the power amplifier (PA) and input impedance of the LNA connected to the TX and RX ports, respectively. S22 is the reflection loss at the antenna port. Our SPDT is designed to maintain reflection at the antenna ports below —11dB over a wide frequency range.

Figs. 5 and 6 illustrate the simulation results of the SPDT switch in RX and TX modes, respectively. The results show low insertion loss and high isolation of the SPDT switch. The proposed switch achieved 0.9dB and 1.78dB insertion loss, and 40dB and 41dB isolation in TX and RX modes, respectively. Even though the matching network is applied to match the impedance of the port, there is still some limitation on matching the big gap impedance mismatch by the single L network.

Table 2. Performance summary and comparison

Parameter	This work		[5]		[6]
Process	CMOS 65nm		CMOS 180nm		CMOS 90nm
Frequency (GHz)	2.4		2.4	5.8	50~67
Mode	Tx	Rx	N/A		N/A
Insertion loss (dB)	0.96	1.78	0.7	1.1	1.9
Isolation (dB)	40	41	35	27	>38
Reflection Loss (dB)	14	11	N/A		N/A
Die size	530μm x 270μm		0.03mm^2		550μm x 550μm

The center frequency in the designed process of our SPDT is 2.4GHz, as mentioned above. The insertion loss is nevertheless maintained constantly low over a wide frequency range up to 5GHz for both RX and TX modes. The isolation of both RX and TX modes is maintained lower than 39dB at up to 4GHz.

4. Conclusion

A low insertion–loss, high-isolation, variable switch based on SPDT for an RF transceiver has been proposed. This work is implemented with standard CMOS 65nm technology. With the operating frequency at 2.4GHz, the switch achieved 0.9dB and 1.78dB insertion loss, and 40dB and 41dB isolation for TX and RX modes, respectively.

The performance summary of the proposed SPDT switch is shown in Table 2. Besides the insertion loss and the isolation performance, the results also illustrate a good matching parameter between the antenna and two terminals of the transceiver.

The performance from insertion loss and isolation of both RX and TX modes is maintained over a wide frequency range, so our SPDT can be applied to many transceiver systems that have an excited frequency in a covered range up to 4GHz. The compact size of our SPDT is suitable for integration into many modern transceiver systems.

Acknowledgement

This work was supported by the Technology Innovation Program (10052624, Development of SoC for Positioning Service using BLE v4.2 IP) funded by the Ministry of Trade, Industry & Energy (MI, Korea)

This work was supported by IDEC (IPC, EDA Tool, and MPW).

References

[1] S. K. Yeo; Y. S. Kwon, "X-band high-power HEMT SPDT switch with selectively anodised aluminium substrate", *Electronics Letters*, Volume: 46, Issue: 24, Pages: 1627 – 1629, 2010. Article (CrossRef Link)

[2] S. Cheng; P. Rantakari; R. Malmqvist; C. Samuelsson; T. Vähä-Heikkilä; A. Rydberg; J. Varis, "Switched Beam Antenna Based on RF MEMS SPDT Switch on Quartz Substrate", *Antennas and Wireless Propagation Letters*, Volume: 8, Pages: 383 – 386, 2009. Article (CrossRef Link)

[3] Y. C. Wu; E. Y. Chang; Y. C. Lin; L. H. Hsu, "Evaluation of Electrical Characteristics of the Copper-Metallized SPDT GaAs Switches at Elevated Temperatures", *Transactions on Device and Materials Reliability*, Volume: 8, Issue: 3, Pages: 621 – 628,2008. Article (CrossRef Link)

[4] Y. C. Wu; E. Y. Chang; Y. C. Lin; H. T. Hsu; S. H. Chen; W. C. Wu; L. H. Chu; C. Y. Chang, "SPDT GaAs Switches With Copper Metallized Interconnects", IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 17, NO. 2, FEBRUARY 2007. Article (CrossRef Link)

[5] Mei-Chao Yeh, Zuo-Min Tsai, Ren-Chieh Liu, Kun-You Lin, Ying-Tang Chang, and Huei Wang; "Design and Analysis for a Miniature CMOS SPDT Switch Using Body-Floating Technique to Improve Power Performance," *IEEE Transactions on Microwave Theory and Techniques*, Volume:54 , Issue: 1, pp. 31 - 39, January 2006. Article (CrossRef Link)

[6] Chul Woo Byeon, Chul Soon Park, "Design and Analysis of the Millimeter-Wave SPDT Switch for TDD Applications"; *IEEE Transactions on Microwave Theory and Techniques*, Volume:61, NO. 8, August 2013. Article (CrossRef Link)

[7] Tomohiro Sano, et al., "A 6.3mW BLE Transceiver Embedded RX Image-Rejection Filter and TX Harmonic-Suppression Filter Reusing On-Chip Matching Network", *Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* 2015 IEEE International, pp. 236-238, Feb. 2015. Article (CrossRef Link)

[8] Feng-Jung Huang and Kenneth O, "A 0.5-um CMOS T/R switch for 900-MHz wireless applications," *IEEE J. Solid State Circuits*, vol. 36, pp. 486-492, May 2000. Article (CrossRef Link)