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General SPICE Modeling Procedure for Double-Gate Tunnel Field-Effect Transistors

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Abstract

Currently there is a lack of literature on SPICE-level models of double-gate (DG) tunnel field-effect transistors (TFETs). A DG TFET compact model is presented in this work that is used to develop a SPICE model for DG TFETs implemented with Verilog-A language. The compact modeling approach presented in this work integrates several issues in previously published compact models including ambiguity about the use of tunneling parameters A_k and B_k, and the use of a universal equation for calculating the surface potential of DG TFETs in all regimes of operation to deliver a general SPICE modeling procedure for DG TFETs. The SPICE model of DG TFET captures the drain current-gate voltage (I_{ds}-V_{gs}) characteristics of DG TFET reasonably well and offers a definite computational advantage over TCAD. The general SPICE modeling procedure presented here could be used to develop SPICE models for any combination of structural parameters of DG TFETs.

Index Terms: Compact model, Drain current, Inverter, Potential profile, TFET, Verilog

I. INTRODUCTION

In recent times the tunneling field-effect transistor (TFET) has attracted a great deal of attention owing to its subthreshold slope (SS) < 60 mV/dec. As such, it is regarded as one of the potential replacements for conventional CMOS technology, which is facing many fundamental challenges in sustaining further technology scaling [1]. The operation principle of the TFET is based on band-to-band-tunneling (BTBT), which enables it to achieve a steeper SS. A TFET can be fabricated using existing semiconductor technologies, and for these reasons TFET is regarded as a very promising technology.

SPICE modeling has been the benchmark of logic- and circuit-level simulation and has played a vital part in the development of current CMOS devices. In order to investigate and better understand the performance of TFET-based logic devices and circuits, a fast compact model with medium accuracy needs to be developed. The literature in this regard is lacking. There are a few TFET Verilog models that exist [2-5]. However, [2, 3] are lookup-table based models that require several fitting parameters; further, the fitting process in [2] is iterative. The model of [4] ignores the source and drain depletion lengths, which limits the accuracy of the model [6]. In the Verilog model of [5], the TFET drain current is found using a short-channel MOSFET model [7], which is physically incorrect for a TFET. Whereas [8] is a standard-reference TFET compact model, there is ambiguity in the use of tunneling parameters A_k and B_k used in the drain current expression of the model. The

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actual A_k and B_k values used in [8, 9] are not clear. While a method to extract the A_k and B_k values from the data of drain current-gate voltage (I_{ds}-V_{gs}) characteristics is presented in [10, 11], the model of [10] and also [12] is for bulk TFET. Further, the model of [11] is piecewise with different equations for saturation and linear regimes of operation which is not suitable for SPICE modeling. Some other models [13, 14] neglect the source depletion region, which at high V_{gs} becomes significant [6] and should not be ignored. Each of these issues restricts the accuracy of the existing models. In light of the above, there is a lack of a clear and accurate TFET compact modeling approach integrating all of the above-mentioned issues from a SPICE model point of view.

This lack of a concise modeling approach integrating all of the above mentioned issues impedes development of SPICE models for TFETs. In this work, we devise a clear double-gate (DG) TFET modeling approach and use it to develop a DGTFET Verilog-A model implemented in SPICE.

The paper is organized in the following sections. Section II explains the DGTFET compact modeling part. Section III includes the verification of the model. The conclusion is presented in Section IV.

II. TFET COMPACT MODEL

This section explains the DGTFET compact model. All the parameters used in the literature are mentioned in Table 1 given below.

Table 1. Electrical and performance parameter description

Symbol	Meaning	Value/unit
L_{ch}	Channel length	5×10^{-6} cm
t_{si}	Channel thickness	1×10^{-6} cm
t_{ox}	Oxide thickness	2×10^{-7} cm
W_{fg}	Gate workfunction	4.2–5.24 eV
N_s=N_d	Source/drain doping	10^{20}/cm^3
ε_{ox}	Dielectric permittivity	3.9–21
ε_{si}	Channel permittivity	11.68
λ	Scaling factor	cm
V_{gs}	Gate bias	V
V_{ds}	Drain bias	V
V_{bis}	Source built-in voltage	V
φ_{s1}	Region I surface potential	V
φ_{s2}	Region II surface potential	V
φ_{dq}	Region III surface potential	V
φ_{s0}	Potential at boundary btw/region I and II	V
φ_{min}	Potential to find l_{tw}	V
L_1	Region I depletion length	cm
L_2	Region II depletion length	cm
l_{tw}	Minimum tunneling distance	cm
E_{avg}	Average electric field	V/cm
A_k	Tunneling parameter	cm^3/V^2·s
B_k	Tunneling parameter	V/cm

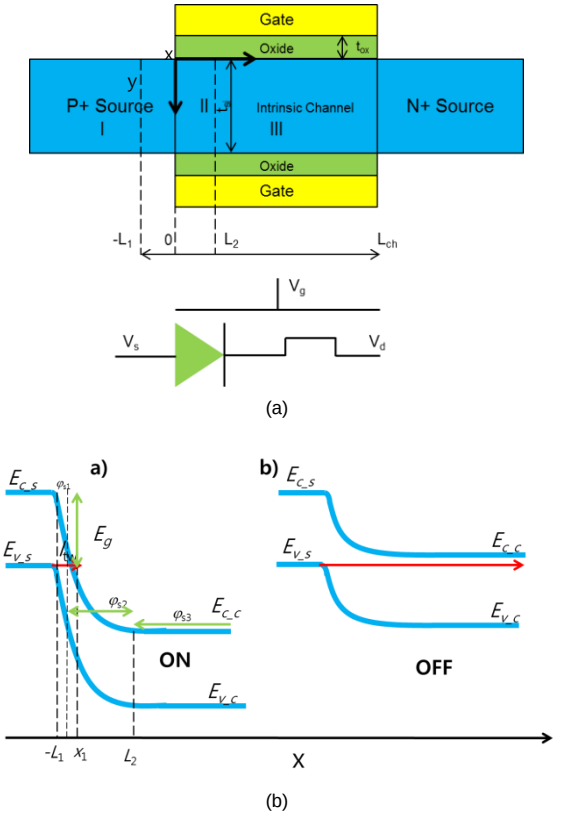

Fig. 1. (a) Schematic of TFET and (b) band diagram of TFET showing the TFET both in its on state (left) and in its off state (right).

Fig. 1 shows the schematic of an N-type DGTFET (N-DGTFET). An N-DGTFET comprises a P^+ source region with doping, an N^+ drain region, and an intrinsic channel.

From a modeling point of view, a DGTFET is divided into 3 regions. Region I is composed of a source depletion region with L_1 highlighting the length of the source depletion region as shown in Fig. 1. Region II comprises the tunneling junction between the source and channel with x=0 being at the boundary of both regions.

Here, L_2 in region II specifies the length of the channel depletion region as indicated in Fig. 1(a). Region III comprises the transport region, where the charge carriers that tunnel through the tunneling barrier are transported to the drain by drift-diffusion with transport along the direction of the x-axis. Fig. 1(b) shows the band diagram of the DGTFET in on (left) and off (right) states.

A Poisson equation is solved in regions I and II with the help of boundary conditions to find the surface potentials in regions I and II. Following [15], the surface potentials φ_{s1} and φ_{s2} are given by

$$\varphi_{s1}(x) = \frac{N_s}{\varepsilon_{si}}(x + L_1)^2, \quad (1)$$

$$\varphi_{s2} = (V_{gs} - V_{fbs}) - [V_{gs} - V_{fbs} - V_{bis} - \varphi_{dg}].\cosh\left(\frac{x-L_2}{\lambda}\right). \quad (2)$$

where V_{fbs} is the flatband voltage. The surface potential in region III, i.e. φ_{dg}, is calculated from [16] after making necessary adjustments for a DGTFET. The depletion lengths of regions I and II, i.e. L_1 and L_2, can be found by solving (1) and (2) together using their continuous potential and electric field at x=0. L_1 and L_2 are given by the following equations [15]:

$$L_1 = \sqrt{\frac{2\varepsilon_{si}\varphi_s(0)}{qN_s}}, \tag{3}$$

$$L_2 = \lambda \cosh^{-1}\left[\frac{V_{gs}-V_{fbs}-\varphi_s(0)}{V_{gs}-V_{fbs}-V_{bis}-\varphi_{dg}}\right]. \tag{4}$$

The potential at the internal boundary between region I and II is given by [15],

$$\varphi_s(0) = -\sqrt{[V_{gs}-V_{fbs}-(V_{bis}+\varphi_{dg})]^2 + 2(V_{gs}-V_{fbs})\emptyset + \emptyset^2} + (V_{gs}-V_{fbs}+\emptyset), \tag{5}$$

where $\emptyset = \left(\frac{qN_s\lambda^2}{\varepsilon_{si}}\right)$ is a constant in (5).

The drain current of the DGTFET can be given by the following expression obtained after making simplifying approximations [9, 11, 17].

$$I_{ds} = qt_{si}l_{tw}A_kE_{avg}^2 \exp\left(-\frac{B_k}{E_{avg}}\right). \tag{6}$$

Here the average electric field is given by [8-14],

$$E_{avg} = \frac{E_g}{ql_{tw}}. \tag{7}$$

The minimum tunneling distance l_{tw} could be described as the distance between the end of the source depletion region (i.e., region I) [8, 10, 11] and the point in region II where the surface potential has a value equal to the band-gap of the channel material. l_{tw} can be given by [8],

$$l_{tw} = L_2 + L_1 - \lambda cosh^{-1}\left(\frac{V_{gs}-V_{fbs}-\varphi_{min}}{V_{gs}-V_{fbs}-V_{bis}-\varphi_{dg}}\right) - \sqrt{\frac{2\varepsilon_{si}}{qN_s}\left(\varphi_{min} - {}^{E_g}/_{q}\right)}. \tag{8}$$

In (8), φ_{min} can be found by setting $\partial l_{tw}/\partial\varphi_{s2} = 0$ [8, 18] and is given by

$$\varphi_{min} = (V_{gs}-V_{fbs}) + \emptyset - \sqrt{\emptyset^2 + [(V_{gs}-V_{fbs}) - (V_{bis}+\varphi_{dg})]^2 + 2\emptyset\left(V_{gs}-V_{fbs}-\frac{E_g}{q}\right)}. \tag{9}$$

In (6), A_k and B_k are found [10, 11] by taking the logarithm on both sides, such that it can be written as

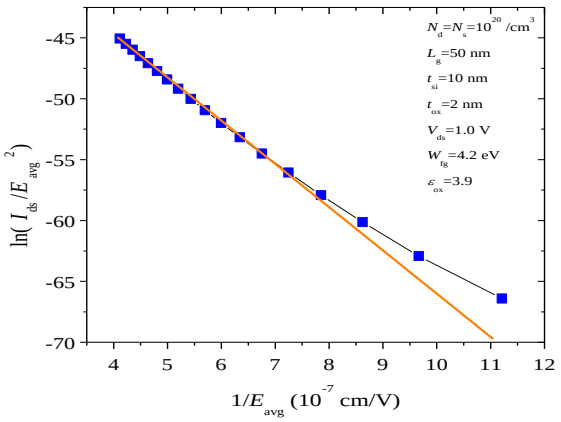

Fig. 2. Illustration of method for extracting A_k/B_k values as a function of V_{ds}(=1.0 V). Here, E_{avg} is a function of V_{gs}. I_{ds} is obtained from TCAD simulation. A_k/B_k can be obtained as the intercept and slope, respectively, of the linear region of the graph shown above.

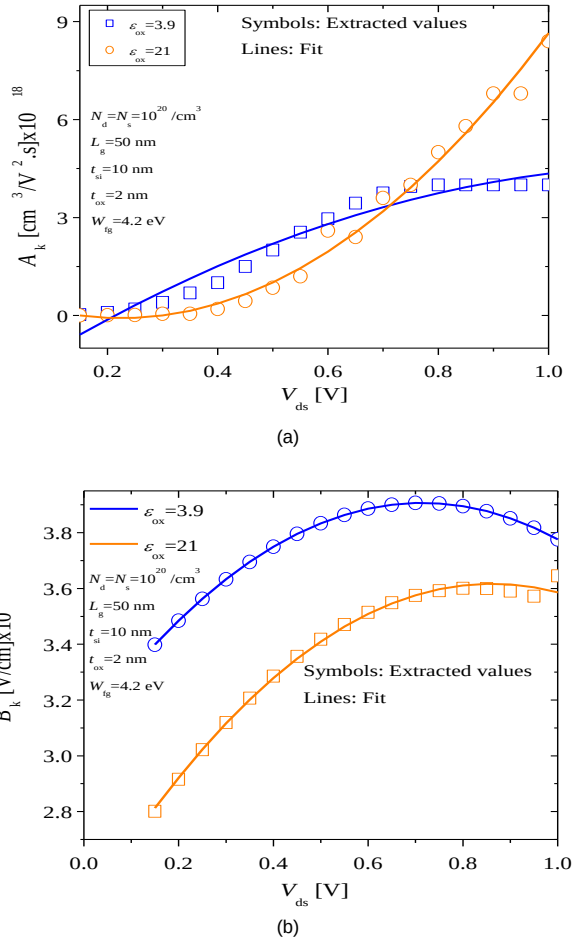

Fig. 3. (a) A_k values as a function of V_{ds} and (b) B_k values as a function of V_{ds}. Symbols in (a): extracted from intercept of (10). Symbols in (b): extracted from slope of log of (10). Lines in (a) and (b): fit for the extracted values given by (11) and (12) for device with ε_{ox}=3.9 (blue), and 21 (orange), respectively. Other device parameters are the same as mentioned in Table 1.

$$\frac{I_{ds}}{E_{avg}{}^2} = \ln(qt_{si}l_{tw}A_k) - \exp\left(\frac{B_k}{E_{avg}}\right). \quad (10)$$

A_k and B_k can be extracted from (10), for a fixed V_{ds} bias value as the intercept and slope of (10). Here I_{ds} is obtained from the TCAD simulation results [19], and E_{avg} is calculated from (7).

The extraction procedure for a fixed V_{ds} value is shown in Fig. 2, whereas extracted A_k and B_k values and their polynomial fits (lines) are shown in Fig. 3(a) and (b), respectively, as a function of V_{ds}. Equations for second-order polynomial fits for A_k and B_k are given below.

$$A_k = A_2V_{ds}{}^2 + A_1V_{ds} + A_0, \quad (11)$$

$$B_k = B_2V_{ds}{}^2 + B_1V_{ds} + B_0, \quad (12)$$

where A_0, A_1, A_2, B_0, B_1, and B_2 are the fitted parameters.

Eqs. (11) and (12) were used to develop the SPICE model for the DGTFET, and are a very important component of the SPICE model. While only 2 dielectric constants were considered in this work, the procedure presented in this work is general and could be used to develop SPICE models for any combination of DGTFET device parameters mentioned in Table 1.

III. MODEL VERIFICATION

Two types of devices were considered in this section. Equivalent parameters (mentioned in Table 1) were considered for both the devices except for ε_{ox}=3.9 with device 1 and ε_{ox}=21 with device 2. N-type (N-DGTFET) and P-type (P-DGTFET) versions of both devices were considered in this work. For simplicity, the equivalent hole and electron tunneling mass was used for the P-DGTFET and N-DGTFET, respectively. In addition, the work function difference for both the P-DFTFET (W_{fg}=5.24 eV) and N-DGTFET (W_{fg}=4.20 eV) were adjusted in TCAD such that the I_{ds}-V_{gs} characteristics obtained were equivalent. Fig. 4 shows the potential profile along the channel length for both

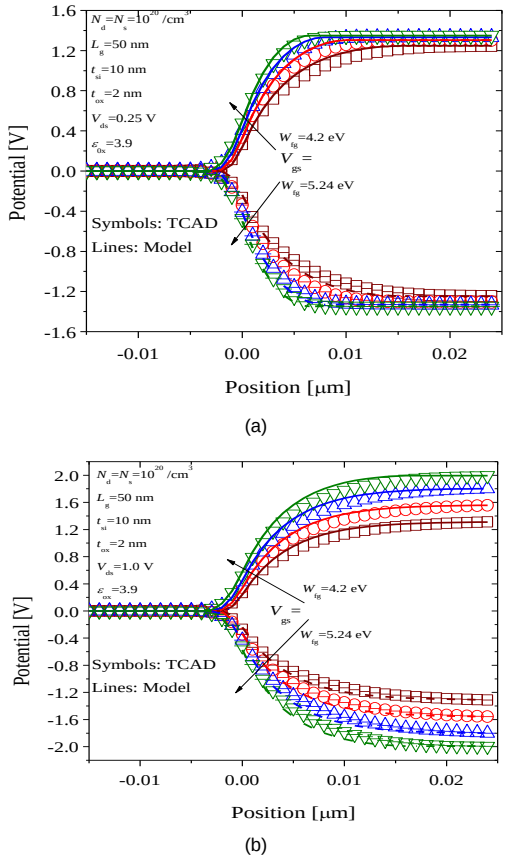

Fig. 4. Surface potential profile for device 1 along channel length for V_{gs} ranging from ±0.25 to ±1 V, and V_{ds} held constant. (a) V_{ds}=±0.25 V. (b) V_{ds}=±1.0 V. Symbols: TCAD, Lines: Model. Open symbols and solid lines: N-type DGTFET, filled symbols and dashed lines: P-type DGTFET. Here '+' and '–' indicate bias for N-DGTFET and P-DGTFET, respectively.

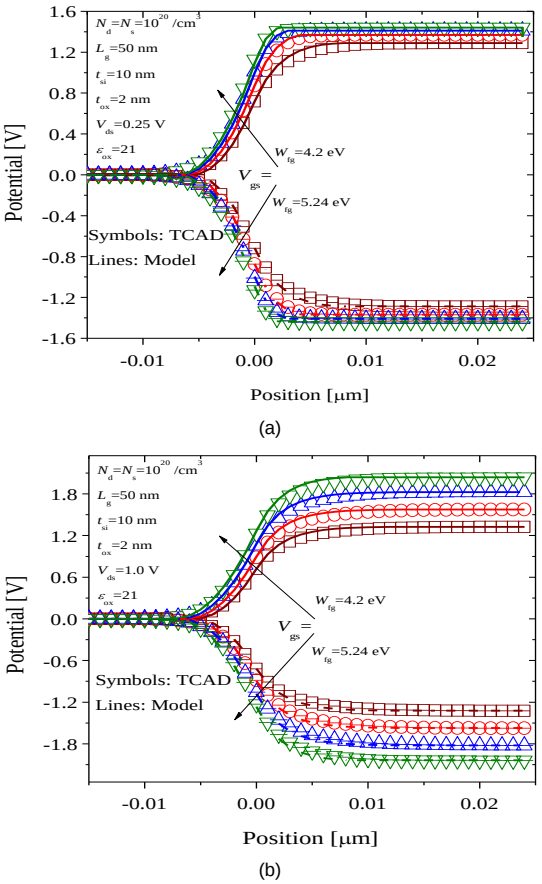

Fig. 5. Surface potential profile for device 2 along channel length for V_{gs} ranging from ±0.25 to ±1 V, and V_{ds} held constant. (a) V_{ds}=±0.25 V. (b) V_{ds}=±1.0 V. Symbols: TCAD, Lines: Model. Open symbols and solid lines: N-DGTFET, filled symbols and dashed lines: P-DGTFET. Here '+' and '–' indicate the bias for the N-DGTFET and P-DGTFET, respectively.

N-type device 1 and P-type device 1 calculated from the model (lines) compared with the potential profile obtained from the simulator (symbols) for V_{gs} ranging from ±0.25 to ±1 V with increments of ±0.25 V and V_{ds} held constant at V_{ds}= ±0.25 V (Fig. 4(a)) and V_{ds}= ±1.0 V (Fig. 4(b)). Here '+' and '–' indicate the bias for the N-DGTFET and P-DGTFET, respectively. The open symbols and solid lines indicate the potential for the N-DGTFET. The filled symbols and dashed lines indicate the potential for the P-DGTFET. The calculated potential profile is in good agreement with that obtained from the simulator.

The potential profile from Fig. 4(a) with V_{ds}=±0.25 V clearly shows the surface potential increasing linearly with increasing V_{gs} and also becoming steeper. This increases the electric field at the source-channel junction resulting in reducing the minimum tunneling distance.

Fig. 4(b), which shows the potential profile for a higher V_{ds}=±1.0 V, demonstrates that with increasing drain bias, the inversion electron concentration is reduced in the channel, allowing for effective unpinning of the channel fermi level.

Fig. 5(a) and (b) show the potential profile for N-type (open symbols [TCAD], and solid lines [model]), and P-type (filled symbols [TCAD] and dashed lines [model]) device 2, which has a higher ε_{ox}=21 at the same V_{gs} and V_{ds} bias conditions as Fig. 4(a) and (b). Fig. 5(a) and (b) clearly show stronger saturation as compared to Fig. 4(a), and (b), respectively, and much shorter channel depletion lengths. This demonstrates that the gate field is stronger in the case of a higher ε_{ox}. Overall, the model results compare very well with simulation results.

Figs. 6 and 7 show I_{ds}-V_{gs} characteristics for N-type device 1 and P-type device 1, respectively, for a V_{ds} ranging from ±0.15 to ±1.0 V. Here '+' and '–' indicate bias for the N-DGTFET and P-DGTFET, respectively. Both the model (lines) and simulation (symbols) show good agreement.

The parameters for A_k and B_k are fitted as A_0 = -2.1195×10^{18}, A_1 = 1.0797×10^{19}, A_2 = -4.3336×10^{18}, B_0 = 2.4356×10^{7}, B_1 = 2.7468×10^{7}, and B_2 = -1.6002×10^{7} shown as blue lines in Fig. 3(a) and (b), respectively.

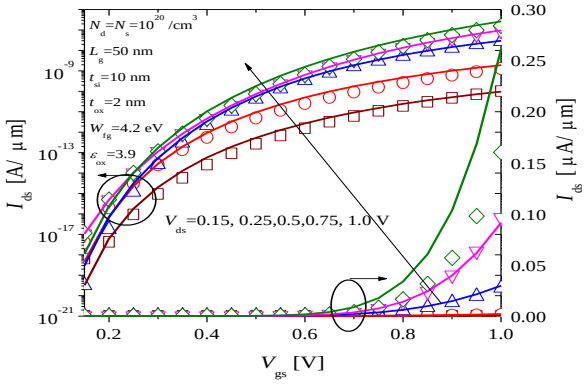

Fig. 6. I_{ds} V V_{gs} for device 1 (N-DGTFET), for different V_{ds} ranging from 0.15 to 1.0 V with increments of 0.25 V. Symbols: TCAD, Lines: Model.

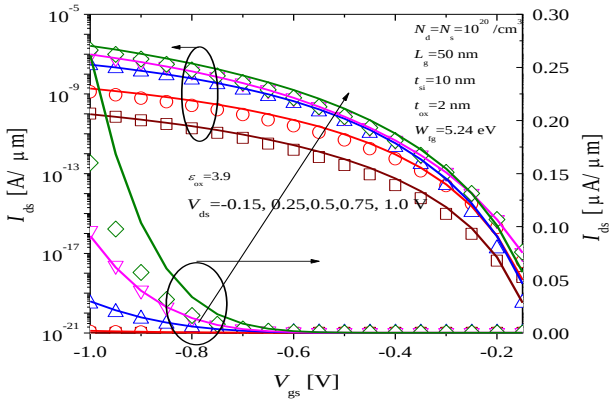

Fig. 7. I_{ds} V V_{gs} for device 1 (P-DGTFET), for different V_{ds} ranging from -0.15 to -1.0 V with increments of -0.25 V. Symbols: TCAD, Lines: Model.

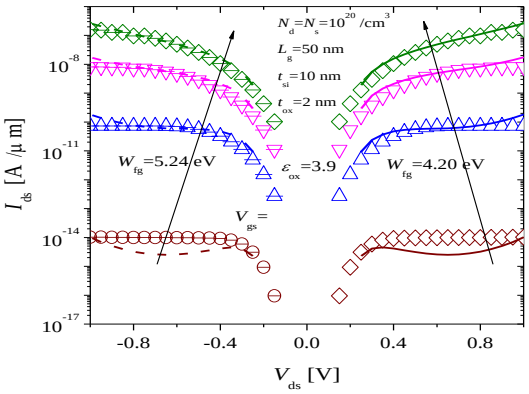

Fig. 8. I_{ds} V V_{ds} for device 1, shown for both N-DGTFET, and P-DGTFET, for different V_{gs} values ranging from ±0.25 V to ±1.0 V in increments of ±0.25 V. Symbols: TCAD, Lines: Model. Open symbols and solid lines: N-DGTFET, Filled symbols and dashed lines: P-DGTFET. Here '+' and '–' indicate bias for N-DGTFET and P-DGTFET, respectively.

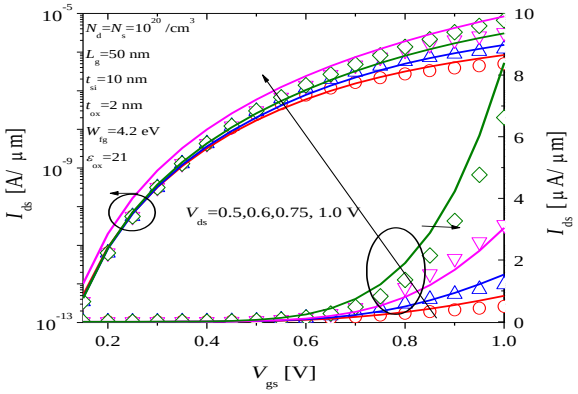

Fig. 9. I_{ds} V V_{gs} for device 1 (N-DGTFET), for different V_{ds} ranging from 0.15 to 1.0 V with increments of 0.25 V. Symbols: TCAD, Lines: Model.

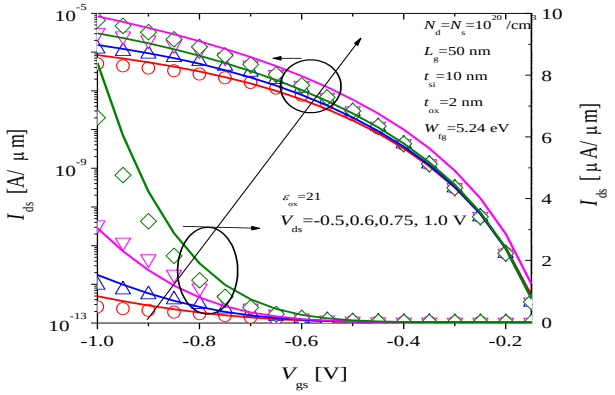

Fig. 10. I_{ds} V V_{gs} for device 2 (P-DGTFET), for different V_{ds} ranging from -0.15 to -1.0 V with increments of -0.25 V. Symbols: TCAD, Lines: Model.

Fig. 8 shows I_{ds}-V_{ds} characteristics for both N-type and P-type device 1, for V_{gs} values ranging from ±0.25 to ±1.0 V. Open (N-DGTFET) and filled symbols (P-DGTFET) indicate simulation results, and solid (N-DGTFET) and dashed lines (P-DGTFET) indicate results from the model. Reasonable agreement can be observed between the model and simulation results, particularly for high V_{gs}, which is a feature of E_{avg}-based models [9]. Here the same fitting parameters for A_k and B_k were used as those in Figs. 6 and 7.

Figs. 9 and 10 show I_{ds}-V_{gs} characteristics for N-type device 2 and for P-type device 2, respectively, calculated from the model (lines) using A_k and B_k with the parameters fitted as A_0 = 3.8153×10^{19}, A_1 = -5.2005×10^{18}, A_2 = 1.3295×10^{19}, B_0 = 3.0917×10^7, B_1 = 2.2843×10^7, and B_2 = -1.597×10^7 as shown by the orange lines in Fig. 3(a) and (b), respectively, with the simulation (symbols). The model captures very well the effect of varying device structural parameters on device characteristics. A much higher I_{ds} is obtained for device 2, which in agreement with Fig. 5, demonstrating that due to a thinner effective oxide, the increased gate field across the tunneling junction results in increased current.

IV. CONCLUSIONS

A SPICE model for a DGTFET is presented in this work. The method of Zhang et al. [8, 15] was adopted to obtain the DGTFET surface potential, and the method developed by [4] was used to extract the A_k and B_k values for 1) a device with conventional SiO_2 as a dielectric and 2) for a high-κ device with ε_{ox}=21. The extracted A_k/B_k values were fitted using a second-degree polynomial. Using the fitting equations, a DGTFET SPICE model was developed. SPICE simulation results were presented for the DGTFET. By finding relevant A_k/B_k fits, the procedure presented in this work could be used to expand the current SPICE model to any combination of DGTFET structural parameters. Future expansion of the current SPICE model includes using constant A_k/B_k values as a function of V_{ds} to achieve I_{ds}-V_{ds} saturation in order to enable SPICE simulation for a wide range of logic devices including inverters. The SPICE model presented here does not need various fitting parameters, unlike [2, 3], and is easy to use. The SPICE model compares very well with TCAD simulation results and offers a definite computational advantage over TCAD.

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