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Estimating Non-Ideal Effects within a Top-Down Methodology for the Design of Continuous-Time Delta-Sigma Modulators

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Abstract—**High-level design aids are mandatory for design of a continuous-time delta-sigma modulator (CTDSM). This paper proposes a top-down methodology design to generate a noise transfer function (NTF) which is compensated for excess loop delay (ELD). This method is applicable to low pass loop-filter topologies. Non-ideal effects including ELD, integrator scaling issue, finite op-amp performance, clock jitter and DAC inaccuracies are explicitly represented in a behavioral simulation of a CTDSM. Mathematical modeling using MATLAB is supplemented with circuit-level simulation using Verilog-A blocks. Behavioral simulation and circuit-level simulation using Verilog-A blocks are used to validate our approach.**

Index Terms—**Excess loop delay, clock jitter, behavioral simulation, DAC linearity, continuous-time delta-sigma modulator**

I. INTRODUCTION

Continuous-time delta-sigma modulators (CTDSM) are now becoming more popular than discrete-time delta-sigma modulators (DTDSM), because CTDSMs have an inherent anti-aliasing property and are more suitable for high sampling rates application than DTDSMs, which are composed of switched-capacitor circuits. Many factors need to be taken into account in designing a CTDSM, due to circuit-level non-idealities: these include active component mismatch resulting from process variation, clock jitter, excess loop delay (ELD), the limited gain-bandwidth product and slew-rate of op-amps, integrator output saturation, and nonlinearity of the digital-to-analog converter (DAC).

Many mathematical models have been proposed for introducing these non-ideal effects into high-level simulations, but a number of factors to be considered makes the simulation of CTDSM very time-consuming.

Behavioral models of switched-capacitor delta-sigma modulators (DSMs) [1] are widely used for the new architectures. These models are of limited accuracy, but are capable of providing a good indication of the way in which performance will be degraded by non-idealities, and so they can help in setting design boundaries and exposing any weaknesses in an architecture. The MATLAB Simulink environment offers adequate simulation time and the possibility of modeling non-linear effects which can added into the delta-sigma modulator structure. It is easy to compose and test the blocks required to model non-ideal effects such as clock jitter, KT/C thermal noise and op-amp non-idealities.

Many techniques have been proposed to speed up the simulation of a CTDSM. Reference [2, 3] proposed methods for the discrete-time (DT) state-space (SS) simulation of CTDSM. Using a DT state-space matrix enhances simulation speed and eliminates the need for user control of the simulation time-step and solver tolerance, allowing precise results to be achieved more rapidly. However, each non-ideality in continuous-time (CT) domain is needed to be converted as DT state-space

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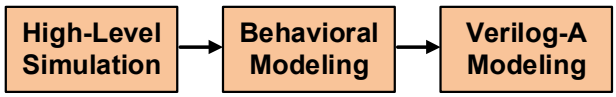

Fig. 1. Top-down design of a delta-sigma modulator.

variables for simulating in DT state-space matrix. It needs complex calculations to combine the functions generated from many different non-idealities in the same DT system matrix. These additional conversions for non-idealities increase the complexity of DT state-space matrix simulation.

In this paper, we propose a top-down design procedure for a CTDSM, which is shown in figure 1. The procedure begins with a high-level simulation to generate a noise transfer function (NTF) which satisfies the application specifications. The NTF is generated in the z-domain, but it must be converted to the s-domain as the convolution of feedback DAC and loop-filter. After the DT-to-CT conversion, we consider the timing delay in the feedback DAC, which is known as the ELD and produces a difference between the original NTF and the converted NTF in the s-domain. We need to transform the converted NTF in order to recover the original NTF. In this procedure, an extra loop path is created in the loop-filter to compensate for the ELD effect of the NTF. The second step in our design procedure is behavioral modeling, which begins with the selection of a DSM structure. We must then estimate the effect of circuit-level non-idealities on the modulator's performance. CT non-idealities can be modeled as simple MATLAB Simulink blocks, which are readily expandable. Behavioral modeling helps the designer to optimize the requirements of a CTDSM such as power and area. The third step in our design procedure is Verilog-A modeling. Modeling a CTDSM structure using Verilog-A blocks helps a designer compare the operation of a circuit-level CTDSM with results from the behavioral model of its structure. Problems in the schematic design usually occur when two or more analog circuit blocks are combined. These problems can be isolated by replacing Verilog-A blocks by circuit blocks. Through this procedure, the schematic design of the analog blocks can then be modified and improved.

The rest of this paper is arranged as follows: In Section II we introduce SD Toolbox high-level design flow, and discuss its drawbacks. In Section III we present

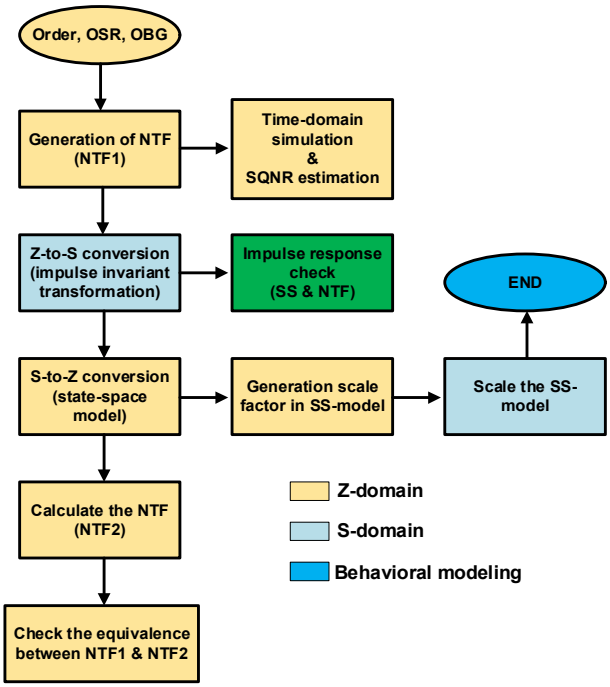

Fig. 2. Design of an CTDSM using SD Toolbox.

our proposed high-level simulation design flow. In Section IV we discuss the major non-idealities of a CTDSM and present a behavioral model to represent them. Section V concludes the paper.

II. SD TOOLBOX DESIGN FLOW

The SD Toolbox [4] is well-established open-source library for high-level design of a DSM. The synthesizeNTF function in the toolbox generates a NTF limited by order, oversampling ratio (OSR) and out-of-band gain (OBG). However, it is only applicable to the DT domain, and so a DT NTF has to be converted to an equivalent CT NTF in order to be used in circuit-level design.

The design flow within SD Toolbox is shown in figure 2. After generating a NTF in the DT domain, it is converted into an equivalent CT state-space matrix by the realizeNTF_ct function, and this this function arranges the CT state-space matrix mapped to an architecture. In this step, the conversion between the DT and CT domains is performed by the impulse-invariant transformation (IIT) [5]. The SD Toolbox compares the impulse response of NTF to CT state-space matrix for checking the equivalence. The CT state-space matrix is reconverted to the equivalent DT state-space matrix by

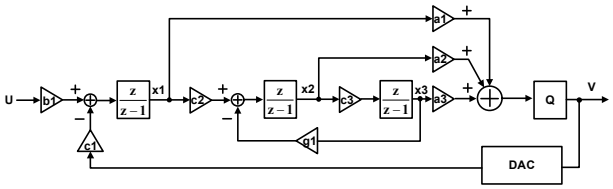

Fig. 3. Cascade integrator feedforward structure (CIFF).

the mapCtoD function. After CT-to-DT conversion, the SD Toolbox performs a dynamic scaling with the DT state-space matrix to make the system stable. The acquired scaling matrix is employed in CT state-space matrix [6].

If different methods are used for DT-to-CT conversion and CT-to-DT conversion, unexpected coefficients may well appear in the DT state-space matrix after a cycle of conversions to CT and back.

For example, the cascade integrator feedforward (CIFF) structure of DSM is shown in figure 3. Its original DT state-space matrix has the following form:

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\end{bmatrix}=\begin{bmatrix}1 & 0 & 0\\ c_2 & 1 & -g_1\\ 0 & c_3 & 1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}+\begin{bmatrix}b_1 & -c_1\\ 0 & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}u\\ v\end{bmatrix}$$
$$y=\begin{bmatrix}a_1 & a_2 & a_3\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}+\begin{bmatrix}0 & 0\end{bmatrix}\begin{bmatrix}u\\ v\end{bmatrix} \quad (1)$$

After DT-to-CT-to-DT conversion by the SD Toolbox design flow, the DT state-space matrix has the following form:

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\end{bmatrix}=\begin{bmatrix}1 & 0 & 0\\ c_2 & 1 & -g_1\\ d_1 & c_3 & 1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}+\begin{bmatrix}b_1 & -c_1\\ 0 & -d_2\\ 0 & -d_3\end{bmatrix}\begin{bmatrix}u\\ v\end{bmatrix}$$
$$y=\begin{bmatrix}a_1 & a_2 & a_3\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}+\begin{bmatrix}0 & 0\end{bmatrix}\begin{bmatrix}u\\ v\end{bmatrix} \quad (2)$$

We can observe the spurious coefficients d_1, $-d_2$, $-d_3$. This result shows that the original form of state-space matrix is not identical to the DT state-space after double conversion. Nevertheless, the NTF derived from the DT state-space after double conversion is equivalent to the original. To proceed with a circuit-level implementation, the dynamic range scaling [7] must be performed. The

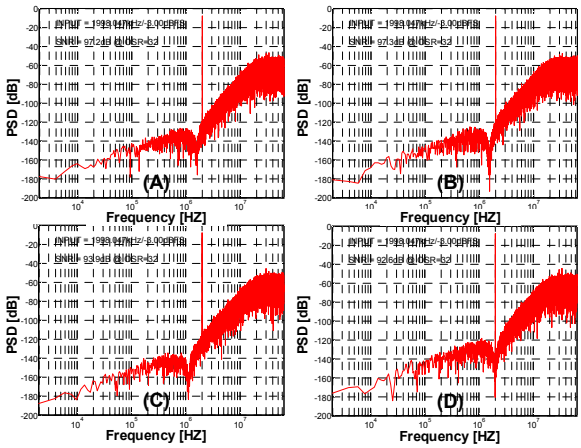

Fig. 4. Power spectral density obtained by (a) DT behavioral modeling, before scaling, (b) CT behavioral modeling, before scaling, (c) CT behavioral modeling, after scaling with S_0, (d) CT behavioral modeling, after scaling with S_1.

SD Toolbox acquires the scaling matrix S_1 from the DT state-space matrix after double conversion, and uses it to scale the CT state-space matrix as follows:

$$\mathbf{A}_s=S_1\mathbf{A}S_1^{-1},\mathbf{B}_s=S_1\mathbf{B},\mathbf{C}_s=\mathbf{C}S_1^{-1},\mathbf{D}_s=\mathbf{D}$$
$$\vec{X}_{new}(t)=\mathbf{A}_s\vec{X}_{new}(t)+\mathbf{B}_s\vec{U}(t) \quad (3)$$
$$\vec{Y}(t)=\mathbf{C}_s\vec{X}_{new}(t)+\mathbf{D}_s\vec{U}(t)$$

U(t) is the input signal, Y(t) is the input to the quantizer, and $X_{new}(t)$ is the scaled output state of the integrator.

We can also obtain a different scaling matrix S_0 from the original DT state-space matrix, which can replace S_1 in (3). After scaling, we obtain a new state-space matrix, which we can use in CT behavioral modeling to check stability and internal swing.

Power spectral density results for DT and CT behavioral modeling before and after scaling are shown in figure 4. We can see that the scaling matrixes (S_0, S_1) derived from the DT state-space moves the zero position of NTF, which modifies the noise-shaping of the DSM. Unfortunately, this scaling technique does not guarantee the stability of the CT state-space matrix. The SD Toolbox does not support dynamic range scaling in the CT domain. Scaling function supported by SD Toolbox is only available to determine the required scaling factor for a conventional structure such as a feedforward or feedback design. This motivates the development of new method of scaling the CT state-space matrix, which

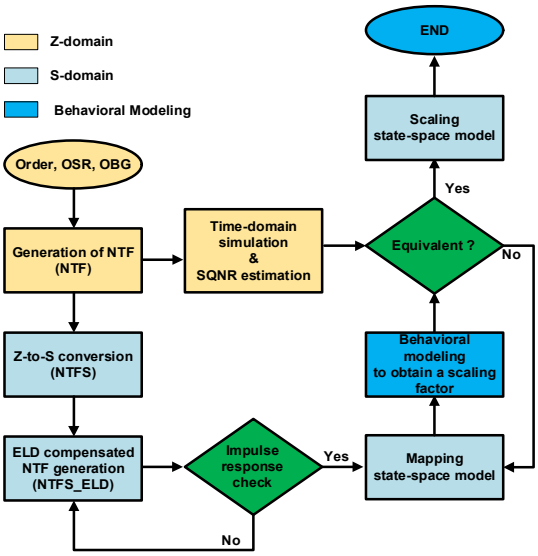

Fig. 5. Proposed high-level design flow.

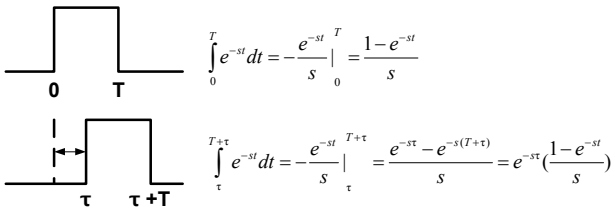

Fig. 6. Representation of ELD in the s-domain.

needs to be sufficiently adoptable to accommodate new DSM architectures.

III. Proposed Design Flow

The proposed high-level design flow is shown in figure 5. A NTF is determined in the DT domain by the NTF generation function in the SD Toolbox, and then converted to the CT domain using an IIT. We then perform the ELD compensation in s-domain [8]. ELD causes the feedback DAC pulse to be shifted into the next clock cycle, as shown in figure 6. This changes both the noise and signal transfer function (NTF & STF), increasing in-band noise and reducing the maximum stable amplitude. The ELD compensation modifies the NTF to eliminate the effect of ELD. The common ELD compensation for loop-filter is performed in the z-domain, but it involves cumbersome algebra [9].

The procedure of ELD compensation is well depicted in figure 7. In figure 7(a), ELD can also be represented by the function exp(-sτ) in the s-domain. In figure 7(b),

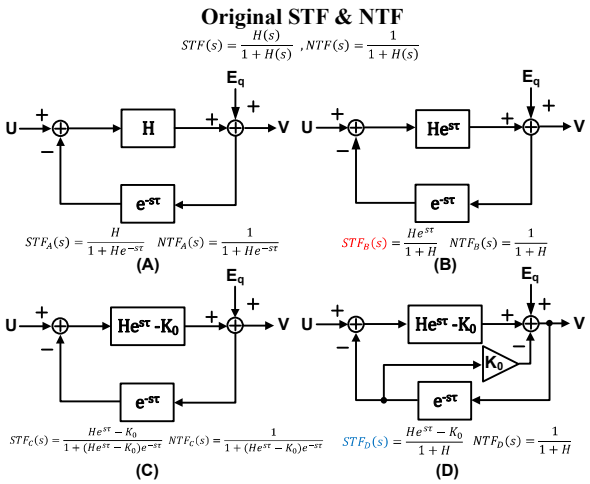

Fig. 7. Procedure of ELD compensation.

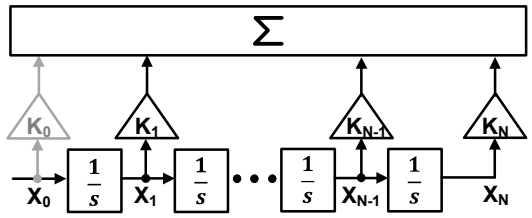

Fig. 8. Representation of ELD in the s-domain.

ELD in the feedback path can theoretically be cancelled by multiplying the loop-filter transfer function H(s) and exp(sτ). This reshapes the NTF, but it also damages the STF by increasing out-of-band peaking. The out-of-band signal compromises operation of the DSM, although this might not be important if the DSM has an OSR above 32. STF peaking issue also leads to an in-band distortion. It becomes apparent during an in-band multi-tone test. To solve this problem, it is essential to cancel out the variable K_0 in loop-filter, which causes the STF peaking.

Assuming that our CTDSM employs a non-return-to-zero (NRZ) DAC, we can derive a transfer function H(s) for the loop-filter shown in figure 8:

$$H(s) = K_1 \frac{1}{s} + K_2 \frac{1}{s^2} + \cdots + K_n \frac{1}{s^n} \tag{4}$$

To compensate the ELD for H(s), this equation can be rewritten as follows:

$$H(s)e^{s\tau} = K_1 e^{s\tau} \frac{1}{s} + K_2 e^{s\tau} \frac{1}{s^2} + \cdots + K_n e^{s\tau} \frac{1}{s^n} \tag{5}$$

Using the Taylor expansion on (5):

$$K_1\frac{e^{s\tau}}{s}\rightarrow\frac{K_1}{s}(1+\frac{s\tau}{1!})$$
$$K_2\frac{e^{s\tau}}{s^2}\rightarrow\frac{K_2}{s^2}(1+\frac{s\tau}{1!}+\frac{s^2\tau^2}{2!})$$
$$K_3\frac{e^{s\tau}}{s^3}\rightarrow\frac{K_3}{s^3}(1+\frac{s\tau}{1!}+\frac{s^2\tau^2}{2!}+\frac{s^3\tau^3}{3!})$$
$$\vdots$$
$$K_n\frac{e^{s\tau}}{s^n}\rightarrow\frac{K_n}{s^n}(1+\frac{s\tau}{1!}+\frac{s^2\tau^2}{2!}+\cdots+\frac{s^n\tau^n}{n!})$$

To rearrange the coefficient effected by the ELD and get the new coefficient about terms 1, 1/s, $1/s^2$,…, $1/s^n$:

$$K_0=K_1\frac{\tau}{1!}+K_2\frac{\tau^2}{2!}+K_3\frac{\tau^2}{3!}\cdots+K_n\frac{\tau^n}{n!}$$
$$K_1'=K_1+K_2\frac{\tau}{1!}+K_3\frac{\tau^2}{2!}+\cdots+K_n\frac{\tau^{n-1}}{n-1!}$$
$$K_2'=K_2+K_3\frac{\tau}{1!}+K_4\frac{\tau^2}{2!}+\cdots+K_n\frac{\tau^{n-2}}{n-2!}$$
$$\vdots$$
$$K_{n-1}'=K_{n-1}+K_n\frac{\tau}{1!}$$
$$K_n'=K_n$$

We can express the equation, which applies the rearranged coefficients transformed by ELD effect:

$$H(s)e^{s\tau}\approx K_0+K_1'\frac{1}{s}+K_2'\frac{1}{s^2}+\cdots+K_n'\frac{1}{s^n}\qquad(6)$$

where K_0 is the input feedforward path corresponding to ELD compensation, and K_1' to K_n' are the coefficients transformed by exp(sτ). In figure 7(c), input feedforward component (K_0) is cancelled out in the loop-filter. In Fig 7(d), adding the new compensation path ($-K_0$) in front of the quantizer restores the NTF without out-of-band peaking in STF.

Figure 9 shows the STF transformation by ELD and ELD compensation. The modified STF (STF_B), which is transformed to compensate the ELD effect, contains the input feedforward path to increase the out-of-band peaking. Eliminating the input feedforward factor in STF_B (STF_D) helps to recover the original STF. ELD compensation performed by inserting a coefficient in front of the quantizer helps to restore the NTF and STF without changing the loop-filter transfer function.

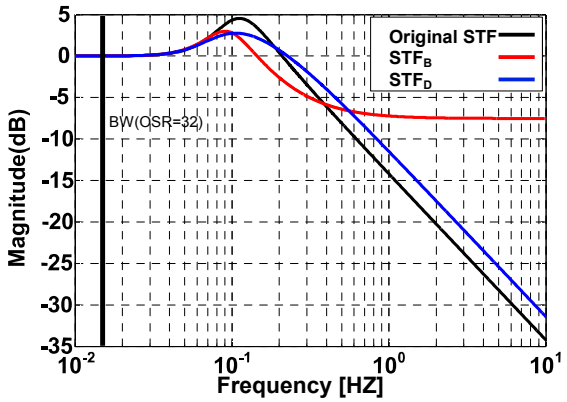

Fig 9. STF modification for ELD compensation (STF_B) and STF reconstruction by removing the input feedforward path term (STF_D).

It is now necessary to formulate the CT state-space matrix, which we will use in dynamic range scaling by (3) to ensure the stability of the system. We can obtain the scaling matrix S_1 from unscaled CT behavioral simulation,

$$S_1=\begin{bmatrix}\frac{y_{1\max}}{y_1} & 0 & 0\\ 0 & \frac{y_{2\max}}{y_2} & 0\\ 0 & 0 & \frac{y_{3\max}}{y_3}\end{bmatrix}\qquad(7)$$

where y_{1max}, y_{2max}, y_{3max} are desired values of the integrator output swings, and y_1, y_2, y_3 are the values obtained from the behavioral simulation.

We can identify the following advantages in the proposed design flow: First, there is only one DT-to-CT conversion. Second, it is capable to perform ELD compensation of the loop-filter in the s-domain. It allows the designer to build behavioral models of non-idealities in the CTDSM. Third, this method of dynamic range scaling can potentially be applied to any CTDSM architecture.

IV. BEHAVIORAL MODELING

At the behavioral modeling stage, we deal with the issues in terms of stability, power consumption and area,

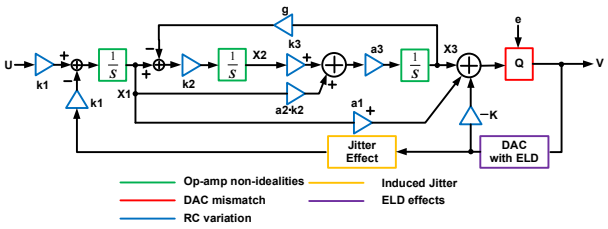

Fig. 10. FF-CTDSM topology without an active adder.

which result from a particular DSM structure. To solve these problems, many papers suggest different approaches of DSM architecture: The architecture with a feedforward ELD compensation path by residual signal can allow the specification of the feedback DAC to be relaxed [10]. A mixed CT/DT 2-1 cascaded DSM architecture is proposed to achieve both high-speed operation and stability [11]. A DSM with a semi-digital FIR filter in the feedback DAC is proposed to overcome the linearity of the feedback DAC [12]. These architectures consider the ELD effect and make a precaution in the loop-filter.

Figure 10 shows the feedforward CTDSM (FF-CTDSM) topology [13], in which the function of the active adder is merged with that of the last integrator. This integrator now requires a wider gain-bandwidth (GBW) and uses more power than the previous last integrator. Nevertheless, the total power is reduced. We add the direct ELD compensation path, which is described in Section III, in front of the last integrator. We use this topology to verify the effect of non-idealities on CTDSM. The coefficients of CTDSM are generated and mapped by the proposed high-level procedure. This topology is 3rd order 9-level CTDSM with OSR 32. We include non-ideal blocks in the DSM behavioral model, which allows us to estimate the effect of non-idealities and determine the marginal budget required to achieve the designed performance of the DSM. The main non-idealities of a CTDSM are as follows:

1) DAC shaping
2) Clock jitter in the current DAC
3) Op-amp non-idealities (finite GBW, finite slew-rate, and saturation levels in each integrator)
4) DAC mismatch and variation of RC values
5) Offset of the first integrator by the data weighted averaging (DWA) data pattern.

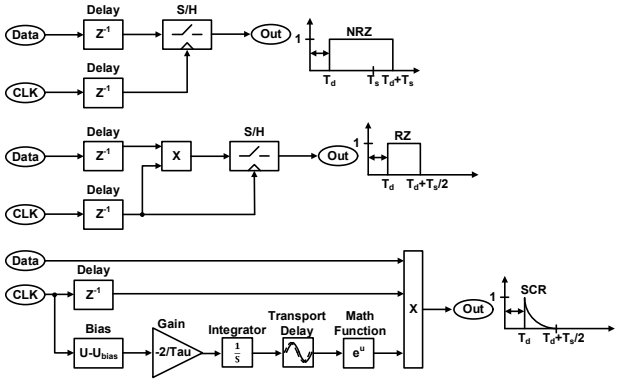

Fig. 11. Simulink models including ELD effects for DAC shaping.

We will now look how these non-idealities are modeled. The effect of each model on overall performance is evaluated in the frequency domain by the fast Fourier transformation (FFT) of output samples.

1. DAC Shaping

The CTDSM coefficients are changed by the start-time, duration and shaping of the DAC waveform. Figure 11 shows three Simulink models used to shape DAC waveforms which have been mentioned frequently in recent papers. NRZ and return-to-zero (RZ) DACs are easily implemented. A switched-capacitor resistor (SCR) DAC is relatively insensitive to clock jitter. The three models allow the start time of the DAC waveform to be varied by a delay block. The delay is much shorter than the sampling clock period and has the same effect to ELD on the data and clock signals. The shorter time duration of delay block increases the simulation time.

Using NRZ DAC modeling in behavioral structure, figure 12 shows the effectiveness of the ELD compensation technique by comparison between (a) CTDSM without ELD compensation and (b) CTDSM with ELD compensation performed on s-domain.

2. Clock Jitter

Clock jitter is the dominant noise source in a CTDSM. Switching operation in the current DAC randomly moves the edges of the sampling clock waveform, modulating the pulse-width of its output, which makes the virtual ground node at the integrator unstable. The error in the integrated charge is proportional to the jitter $\Delta t[n]$, and

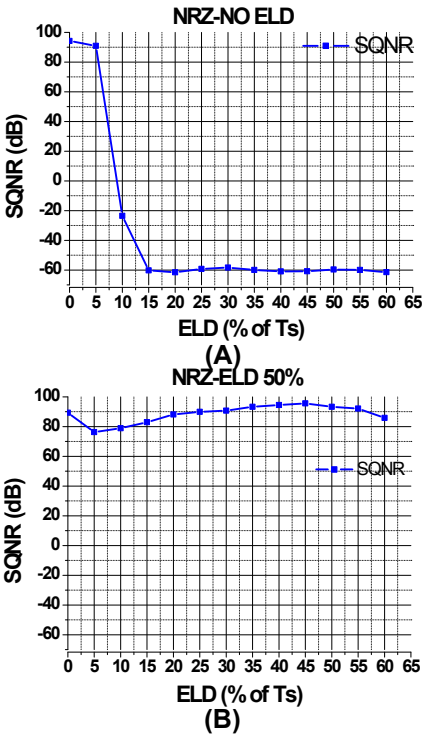

Fig. 12. ELD robustness comparison between (a) CTDSM without ELD compensation, (b) CTDSM with ELD compensation.

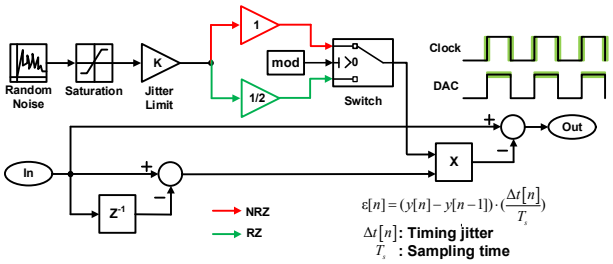

Fig. 13. Simulink model of clock jitter.

appears as pulse-width sampling noise in the ADC. The sampling error $\varepsilon_{jitter}[n]$ depends on the edge-shaping of the output of the current DAC. In a NRZ DAC, the pulse-width jitter [14] is given by

$$\varepsilon_{jitter}[n] = \{y[n] - y[n-1]\}\frac{\Delta t[n]}{T_s} \quad (8)$$

where T_s is the sampling clock period, and y[n] is the NRZ signal which is fed back into the first integrator that corresponds to the n^{th} clock cycles.

Figure 13 shows how the errors caused by clock jitter can be modeled as a pulse-width amplitude error in each

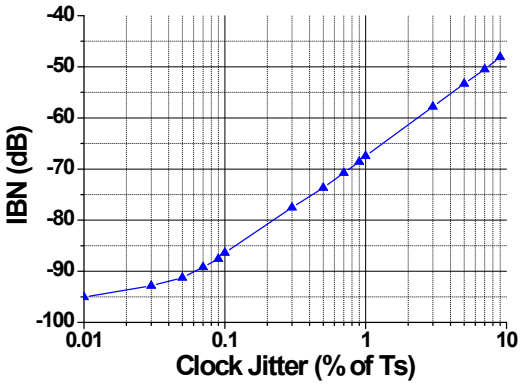

Fig. 14. Effect of clock jitter on a feedback NRZ DAC.

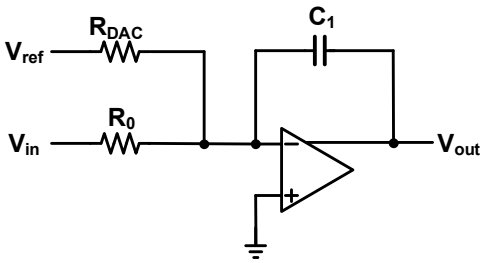

Fig. 15. Schematic of an active RC integrator.

every clock cycle. This technique does not require the simulation time-step to be shorter than jitter period. It helps to avoid excessive simulation time. In the jitter model, random noise is conveniently generated as a Gaussian with a standard deviation of unity. This clock jitter model is placed after the model of the feedback DAC. It changes the amplitude of the feedback signal.

Figure 14 shows how clock jitter affects the in-band noise (IBN). Increasing the clock jitter by a factor of 10 increases the IBN by 20 dB/dec. Our simulation of IBN produces similar results to those reported by previous publications [5, 15].

3. Integrator Non-idealities

The limitation of an op-amp include finite GBW and slew-rate, an output level at which the integrator saturates, and nonlinearity of output swing, leading to harmonic distortion (HD). Op-amp's devices also produce thermal and flicker noise.

Figure 15 is a schematic of an active RC-integrator. If the transfer function of its op-amp is A(s), then the integrator transfer function (ITF) can be expressed as follows [16]:

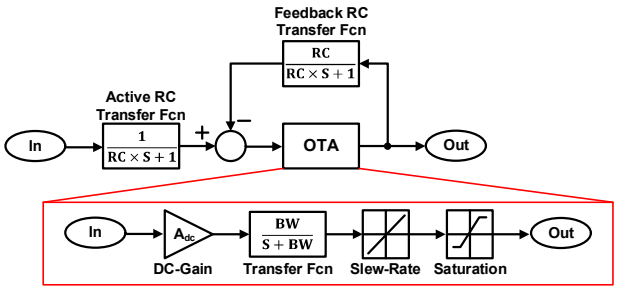

Fig. 16. Simulink model of non-ideal integrator.

$$ITF(s) = \frac{K_i f_S}{s(1+\frac{1}{A(s)})+\frac{1}{A(s)}(1+K_{DAC})f_S} \approx \frac{K_i f_S}{s}$$

$$\text{(where, } A(s) \to \infty,\ K_i f_S = \frac{1}{R_0 C_1} \text{ and } K_{DAC} f_S = \frac{1}{R_{DAC} C_1}\text{)} \quad (9)$$

K_{DAC} is the scaling coefficient of the DAC, and $K_i f_s$ is the scaling coefficient of the first integrator, which is proportional to the sampling frequency. The ITF is distorted by the active RC value and A(s). If A(s) has a single pole, then the ITF becomes the product of the amplifier transfer function and the ideal ITF. The poles of the loop-filter transfer function become the zeros of the NTF, which are all moved away from DC, reducing the in-band quantization noise and modifying the noise-shaping of the NTF. This non-ideality is called leaky integration, and it is the primary factor to be considered in assigning a power budget. The finite slew-rate of the integrator limits the current into the integrating capacitance, so that it is incompletely charged. This causes a settling error at the end of each clock cycle, leading to HD and a raising of the noise floor: this is the dominant source of oscillation in the loop-filter. Saturation of the output swing range is related to the scaling that takes place in the modulator. This non-ideality, called clipping, limits the output of the integrator, even if there is a large input signal incoming into the loop-filter. This factor also generates distortion tones and white noise. However, these effects can be overcome by marginal scaling.

The integrator which we have been discussing, is modeled by the block shown in figure 16. The separation of the op-amp transfer function and the active RC transfer function from the ITF gives the designer more choice in specifying the op-amp. The total thermal noise of the active components can be aggregated into a noise

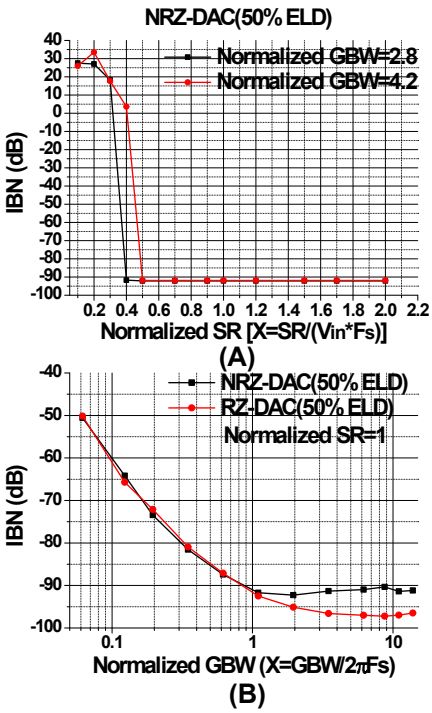

Fig. 17. IBN VS (a) normalized slew-rate, (b) normalized GBW.

power spectral density, and HD tones are expressed as a Volterra-series expansion. This model brings us close to the performance of a real circuit, but it still does not account for the effect of a specific technology and layout. We will consider these effects during Verilog-A modeling.

Figure 17(a) shows the slew-rate of an integrator versus IBN. The slew-rate is normalized by dividing it by the product of V_{in} and F_s, where V_{in} is maximum stable amplitude of input voltage, and F_s is the sampling clock frequency. A high normalized slew-rate means that more power is consumed by the CTDSM. However, our simulation shows that a normalized slew-rate below 0.5 causes the oscillation in loop-filter, whereas the normalized slew-rate above 0.5 does not affect the IBN. Figure 17(b) shows IBN against the normalized GBW, which is GBW divided by the sampling clock frequency. As normalized GBW is reduced, power consumption drops but IBN dramatically increases. Slew-rate and GBW are main determinants of power consumption that can be modified during schematic design, in a trade-off with IBN.

4. DAC Mismatch and Variation of RC values

In a multi-bit quantizer, the feedback signal from the

Table 1. Effect of DAC mismatch on SNDR

Mismatch (%)	0.1	0.2	0.5	1	2	5
DEM ON (dB)	91.7	87.2	74.2	72.6	68.4	60.3
DEM OFF (dB)	71.7	65.7	52.0	49.8	45.7	37.7

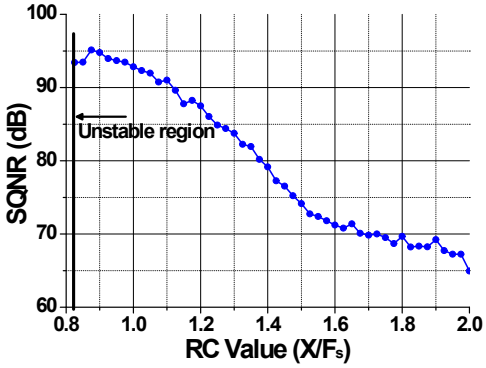

Fig. 18. SQNR degradation by RC values variation.

current DAC to the first integrator is the sum of currents from several unit-current cells. When the currents from these cells are different, a current mismatch occurs. This can be related to the process variation, topology and size of the DAC. A current mismatch reduces the linearity of the current DAC, raising the peak values of the second and third HD tones, and bringing up the noise floor. A current mismatch can be reduced by DWA, which is a type of dynamic element matching (DEM) algorithm that equalizes the usage of unit-current cells. This is effective in reducing the HD tones, and it also enhances the signal-to-noise distortion ratio (SNDR) shown in Table 1.

The variation of RC values changes the coefficients of the loop-filter, moving poles and zeroes, and hence modifying NTF shaping. In most CMOS technologies, the values of resistors can vary by ±30%. Figure 18 shows how modulator performance is degraded by variation of RC values, normalized to the sampling frequency. Normalized RC values below 0.8 make the system unstable, but values above 1 reduce the capability of the loop-filter to suppress IBN. A CTDSM needs an auto calibration circuit to compensate for these variations. The calibration circuit uses extra resistors or extra capacitances to compensate the changes in RC values.

5. Offset of the 1st Integrator by the DWA Pattern

The offset of the first integrator is generated from the switching activity of the current DAC. It is hard to

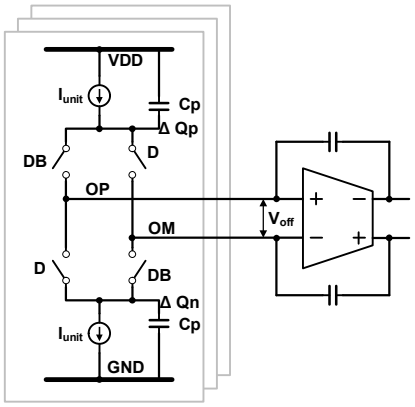

Fig. 19. Second order harmonic effects in a current DAC.

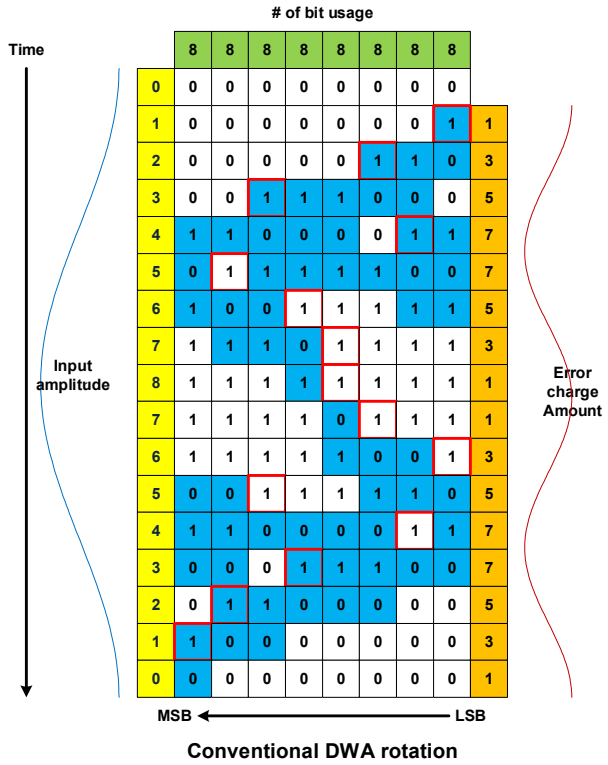

Fig. 20. Second order harmonic pattern by DWA algorithm.

represent the offset in a behavioral model, so we use the Verilog-A modeling to estimate this effect. The occurrence of the offset of the first integrator is shown in figure 19 [17]. A CTDSM usually uses a differential input integrator. So uneven data come into differential input. It changes the charges ΔQ_p and ΔQ_n that are injected into the parasitic capacitance C_p. Error in ΔQ_p and ΔQ_n produces an offset V_{off} at the input of the first integrator, with a magnitude which depends on the DWA data pattern. Figure 20 shows the data pattern produced by the DWA algorithm. The white boxes correspond to

Table 2. Simulation of the effect of parasitic capacitance on SNDR

Parasitic capacitance	0 fF	2 fF	5 fF	10 fF	20 fF
SNDR (dB)	92.33	90.47	88.64	83.97	77.93

unit current cells (0=off, 1=on) ; blue boxes indicates that it changes the state of the unit current cell. Boxes outlined in red correspond to the starting point of unit current cells which are turned on. The number of unit current cell which are turned on is determined by the input amplitude. Changing the state means the switching activity occured in the unit current cell. The amount of switching activity determines the error charge in the parasitic capacitance. The variation in error charge goes through two cycle during each cycle of the input signal, generating the second HD tones. Table 2 shows the effect of parasitic capacitance on the SNDR, implying that considerable care is needed in the layout of the current DAC.

V. CONCLUSION

We describe a methodology for the high-level simulation of the design of a CTDSM. We discuss ELD compensation for CTDSM and suggest an approach to behavioral simulation, which is suitable for any topology of CTDSM. We show how to model non-ideal effects within such a simulation by means of MATLAB Simulink blocks, which can help a designer to meet the circuit specification. These models are composed of mathematical components. We expect that the proposed techniques will make it quicker to design a CTDSM. Some forms of non-ideality have mechanisms which are too complicated to be modeled accurately, and we show how to use a Verilog-A model to mimic such circuit-level non-idealities.

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REFERENCES

[1] P. Malcovati, et al., “Behavioral modeling of switched–capacitor sigma–delta modulators”, *IEEE Trans. Circuits Syst. I*, vol. 50, no. 3, pp. 352–364, Mar. 2003.

[2] M. keller, et al., “A method for the discrete–time simulation of continuous–time Sigma–delta modulators”, *in Proc. IEEE ISCAS*, May. 2007.

[3] G. G. E. Gielen, et al., “An analytical integration method for the simulation of continuous–time ΔΣ Modulators,” *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 3. pp. 389–399, Mar. 2004.

[4] Category: Control Systems, File: SD Toolbox [Online], Available: http://www.mathworks.com/matlabcentral/fileexchange

[5] M. Ortmanns, Continuous–Time Sigma–Delta AD Conversion, Springer.

[6] R. Schreier, et al.,, “Delta–sigma modulators employing continuous–time circuitry,” *IEEE Trans. Circuits Syst. I*, vol. 43, no. 4, pp. 324–332, Apr. 1996.

[7] R. Schreier, G. C. Temes, Understanding Delta–Sigma Data Converters.

[8] S. Pavan , “Excess loop delay compensation in continuous–time delta-sigma modulators”, *IEEE TCAS-II*, vol. 55, no. 11, pp. 1119–1123, Nov. 2008.

[9] J. Cherry, et al., “Excess loop delay in continuous–time delta–sigma modulators,” *IEEE TCAS-II*, vol. 46, no. 4, pp. 376–389, Apr. 1999.

[10] C-Y. Ho, et al., “A 4.5mW CT self-coupled ΔΣ modulator with 2.2MHz BW and 90.4dB SNDR using residual ELD compensation,” *ISSCC Dig. Tech. Papers*, pp. 274–276, Feb. 2015.

[11] K. Lee, “Mixed CT/DT cascaded sigma-delta modulator”, *J. Semicond. Technol. Sci.*, vol. 9, no. 4, pp. 233–239, Dec. 2009.

[12] P. Shettigar, et al., “Design techniques for wideband single–bit Continuous–time modulators with FIR feedback DACs”, *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2865–2879, Dec. 2012.

[13] S.-J. Huang, et al., “A 1.2 V 2 MHz BW 0.084 mm2 CT ADC with 97.7 dBc THD and 80 dB DR using low-latency DEM,” *in IEEE ISSCC Dig. Tech. Papers*, pp. 172–173, Feb. 2009.

[14] X. Chen, "A Wideband low-power continuous-time delta-sigma modulator for next generation wireless applications", Ph.D. dissertation, Oregon State Univ.
[15] P. M. Chopp, et al., "Analysis of clock–jitter effects in continuous–time ΔΣ modulators using discrete–time models", *IEEE Trans. Circuits Syst. I*, vol. 56, no. 6, pp. 1134–1145, Jun. 2009.
[16] M. Ortmanns, et al., "Compensation of finte gain–bandwidth induced errors in continuous–time sigma-delta Modulators", *IEEE Trans. Circuits Syst. I*, vol. 51, no. 6, pp. 1088–1099, Jun. 2004.
[17] K. Matsukawa, et al., "A 69.8 dB SNDR 3rd-order continuous-time delta–sigma modulator with a ultimate low power tuning system for a worldwide digital TV-receiver," *in Proc. IEEE CICC*, Sep. 2010.

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