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2-6 GHz GaN HEMT Power Amplifier MMIC with Bridged-T All-Pass Filters and Output-Reactance-Compensation Shorted Stubs

Sang-Kyung Lee, Kyung-Tae Bae, and Dong-Wook Kim

Abstract—**This paper presents a 2-6 GHz GaN HEMT power amplifier monolithic microwave integrated circuit (MMIC) with bridged-T all-pass filters and output-reactance-compensation shorted stubs using the 0.25 μm GaN HEMT foundry process that is developed by WIN Semiconductors, Inc. The bridged-T filter is modified to mitigate the bandwidth degradation of impedance matching due to the inherent channel resistance of the transistor, and the shorted stub with a bypass capacitor minimizes the output reactance of the transistor to ease wideband load impedance matching for maximum output power. The fabricated power amplifier MMIC shows a flat linear gain of 20 dB or more, an average output power of 40.1 dBm and a power-added efficiency of 19-26 % in 2 to 6 GHz, which is very useful in applications such as communication jammers and electronic warfare systems.**

Index Terms—**GaN, HEMT, Power amplifier, MMIC, All-pass filter, Reactance compensation**

I. INTRODUCTION

Since remote-controlled improvised explosive devices appeared, battlefield environments have dramatically changed and the necessity has also arisen for communication jammers that require wideband operation and high output power in a frequency range of several GHz. A GaN high electron mobility transistor (HEMT) on a SiC substrate is considered as a prime candidate for the wideband high-power amplifier. GaN itself has a wide bandgap of 3.49 eV, which is associated with a high breakdown electric field of 3.3 MV/cm and high saturated electron velocity of 2.5×10^7 cm/s. The high saturated electron velocity results in high current density and, therefore, high output power. The GaN HEMT on the SiC substrate also benefits from a high thermal conductivity of 4.5 W/cm-K of its substrate in addition to a thermal conductivity of more than 1.5 W/cm-K of itself [1]. The SiC substrate helps the GaN HEMT to operate in a high-power mode by effectively removing heat generated from the inside of the transistor. The high breakdown electric field increases the output power per unit gate width by allowing high operating voltage, which makes us use a smaller-sized transistor for the same output power. Compared with conventional Si- and GaAs-based transistors, a high supply voltage due to the material property and large output impedance due to the smaller-sized transistor are advantageous in terms of high-power operation and wideband impedance matching. Therefore, the GaN transistor is optimal for a wideband power amplifier that can be utilized in the applications of communication jammers and electronic warfare systems.

For wideband high-power amplifiers, many matching techniques have been used in previously published studies. They include reactive filter synthesis [2, 3], distributed configurations [4, 5] and resistive matching circuits [6, 7]. Reactive filter synthesis has a limitation in extending the bandwidth of a power amplifier, and a

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distributed power amplifier has clear advantages in terms of its return loss and bandwidth but has disadvantages in requiring a large chip area for high gain and phase velocity tuning between input and output artificial transmission lines.

This paper presents a 2-6 GHz GaN HEMT power amplifier MMIC with bridged-T all-pass filters for wideband input matching and output-reactance-compensation shorted stubs for wideband optimum load impedance matching for maximum output power. In this paper, the bridged-T all-pass filter, a kind of resistive matching circuit, at the gate of a power amplifying stage (second-stage) in the power amplifier is modified to consider the channel resistance effect, and the shorted stub reduces the output reactance of the transistor to move the output impedance of the transistor to the impedance with a low-Q value. The presented GaN power amplifier MMIC is fabricated using the 0.25 μm GaN HEMT process of WIN Semiconductors, Inc. [8].

II. CIRCUIT DESIGN

1. Wideband Impedance Matching Using a Bridged-T All-Pass Filter in a Power Amplifying Stage

Design specifications for the wideband GaN power amplifier MMIC, which include a linear gain of at least 20 dB, an output power of more than 40 dBm and an input return loss of 10 dB or more from 2 to 6 GHz, are summarized in Table 1. A 0.25 μm GaN HEMT (NP2500MS) having 10 fingers with 125-μm unit gate width is used at a bias condition of 28 V drain-source voltage and 100 mA drain-source current per transistor. The HEMT uses a source-coupled field plate and has a typical power density of 4.0 W/mm at 10 GHz under the continuous-wave mode. Under the given bias condition, the HEMT has a maximum oscillation frequency f_{max} of 45.6 GHz, a cutoff frequency f_T of 23.5 GHz, and a maximum stable gain of 23.5 dB at 4 GHz.

Fig. 1 shows a bridged-T all-pass filter that can be used as a wideband matching circuit at a gate of the GaN HEMT. As a kind of resistive matching technique, the impedance matching scheme using the bridged-T all-pass filter is advantageous in terms of a low standing wave ratio at the input port and a flat transfer function. When the ratio of $R_L : 1/\omega C_1 : 1/\omega C_2 : \omega L_1 : \omega L_2$ is 1 : 2 : 1/2 : 1 : 1 under the same R_L and R_s, the filter's transfer function (v_{out}/v_{in}) has pole and zero locations at the same frequency, so v_{out} has the same characteristic as v_{in} regardless of the operating frequency, as shown in Fig. 2 [9]. When an equivalent circuit of the HEMT at the gate node is simply described as a gate-source capacitor C_{gs}, if the capacitor C_2 of Fig. 1 is replaced with C_{gs}, it is possible to match the gate impedance of the transistor to R_s in a wideband frequency range, and the transfer function of v_{out}/v_{in} has an all-pass characteristic. In a real matching circuit, it is desirable that the gate voltage of the transistor v_{tr}, which corresponds to the voltage across C_2 in Fig. 1, exactly follows the input voltage v_{in}. However, v_{tr} approximately imitates v_{in} and achieves the desired matching performance only up to the frequency f_c where v_{tr} has 180° phase shift, compared with v_{in}. The frequency f_c is determined by the R_s (or R_L) and C_2 of Fig. 1 and can be expressed as $2/R_sC_2$ (or $2/R_LC_2$). The transfer responses of the node voltages of Fig. 1 are shown in Fig. 2, and v_{tr} has a peaking response near f_c, which is about 6.5 GHz. Because the transistor's gain typically decreases with the frequency, the peaking characteristic has a positive effect on the matching circuit for flat gain performance in a wide frequency region.

In an ideal case, the transistor can be equivalently described as C_{gs} at the gate side and replaces C_2 in Fig. 1.

Table 1. Design specifications of the wideband power amplifier MMIC

Items	Specifications
Frequency	2-6 GHz
Saturated output power	≥ 40 dBm
Efficiency	≥ 20 %
Linear gain	≥ 20 dB
Input return loss	≥ 10 dB
1. 0.25 μm GaN HEMT NP2500MS (W_g = 10×125 μm) of Win Semiconductors Inc. 2. Bias condition: V_{DS} = 28 V, I_{DS} = 100 mA per transistor	

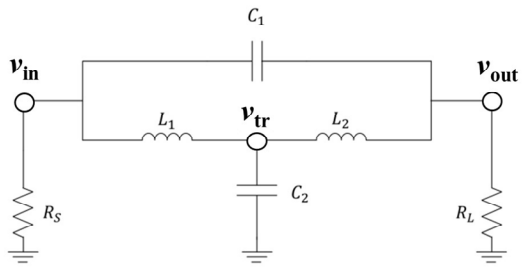

Fig. 1. A bridged-T all-pass filter.

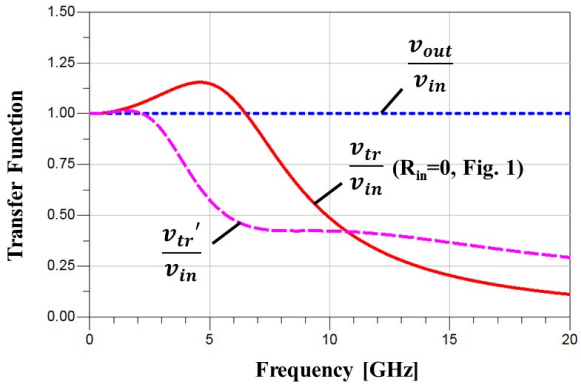

Fig. 2. Transfer responses of node voltages in the bridged-T all-pass filter.

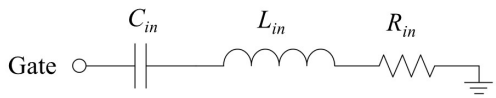

Fig. 3. Simplified input small-signal model at the gate of a transistor.

However, in a real transistor (in this case, NP2500MS), its input equivalent circuit at the gate node also has a series parasitic inductor L_{in} and a channel resistor R_{in} as shown in Fig. 3. Here, C_{in} includes C_{gs} and the Miller capacitance of a gate-drain capacitor C_{gd}. When the input equivalent circuit of Fig. 3 is used instead of C_2 in Fig. 1, the node voltage at the gate v_{tr}', which is differently designated to distinguish it from the v_{tr} of Fig. 1, where only C_2 exists, is also shown in Fig. 2. L_{in} has a very minor effect on the v_{tr}' response and can be ignored, but R_{in}, even though its value is small, for example only several Ω, degrades the node voltage's response as shown in the figure. In this paper, we modify the values of the inductors L_1 and L_2 to make the response of v_{tr}' similar to that of v_{tr} at the condition of $R_{in} = 0$, while maintaining the input matching condition at the v_{in} port. As R_{in} increases, the frequency f_c tends to decrease and the frequency bandwidth narrows. By adjusting an impedance ratio of L_1 and L_2, we can control the voltage division ratio across L_1 and L_2. Using different L_1 and L_2 values, we obtain one more degree of freedom to resolve the bandwidth reduction of the filter due to the parasitic input resistance of the GaN transistor. In this work, by increasing L_2 by about 20 % over L_1, we improve the frequency response of the gate voltage as shown in Fig. 4 where the responses of v_{tr} ($R_{in} = 0$) and v_{tr}' ($R_{in} \neq 0$) are very similar, compared with those of Fig. 2.

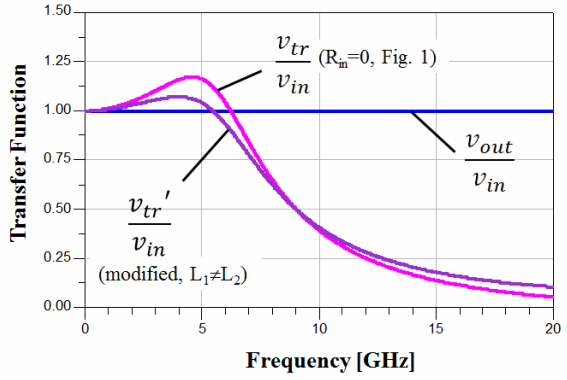

Fig. 4. Improved transfer response of the gate node voltage in the modified bridged-T all-pass filter when $R_{in} \neq 0$.

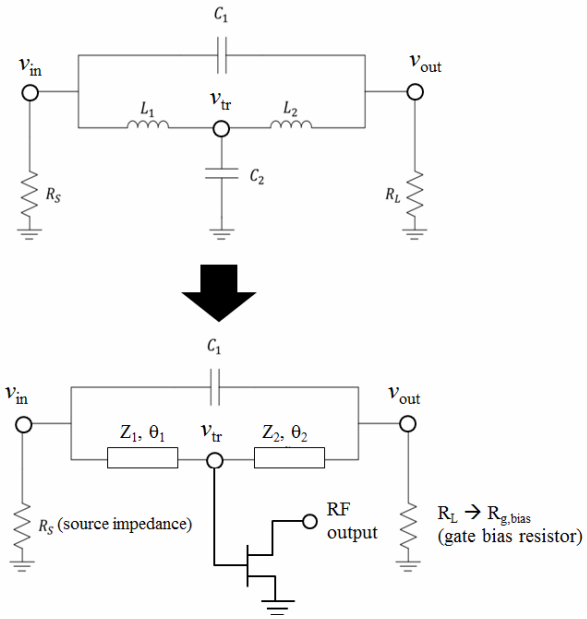

Fig. 5. The bridged-T all-pass filter applied to the gate side of the GaN transistor as an impedance matching circuit.

The bridged-T all-pass filter of Fig. 1 is applied to the gate node of the GaN HEMT as an impedance matching circuit, as shown in Fig. 5. L_1 and L_2 are changed to two microstrip lines with the characteristic impedances of Z_1 and Z_2 and the electrical length of θ_1 and θ_2, respectively. As previously mentioned, C_2 is replaced with the GaN transistor. The node voltage v_{tr} between two microstrip lines is applied to the gate of the transistor and is amplified. R_s of Fig. 1 corresponds to source impedance and R_L is substituted with the gate bias resistor $R_{g,bias}$ in Fig. 5.

For the output power of 40 dBm, four 10 × 125 μm HEMTs are used in the second power-amplifying stage of the two-stage power amplifier and the above mentioned

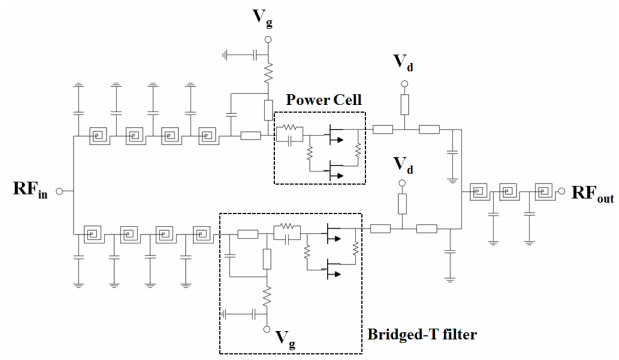

Fig. 6. A schematic circuit diagram of the power amplifying stage in the two-stage power amplifier.

all-pass matching scheme is applied to a power cell with two 10 × 125 μm transistors in parallel. The power cell is stabilized with a parallel resistor-capacitor circuit, which is inserted in series between the gate and the all-pass matching circuit and plays a role in dampening the large low-frequency gain of the transistor. The schematic circuit for the power-amplifying stage is shown in Fig. 6. The power cell is first matched to 10 Ω using the bridged-T all-pass filter and then to 50 Ω through a ladder network of multiple series inductors and shunt capacitors. Two power cells are combined and matched to 25 Ω with a return loss of larger than 10 dB for direct connection to the first driving stage with the output impedance of 25 Ω.

2. Wideband Load Impedance Matching for Maximum Output Power Using an Output-Reactance-Compensation Shorted Stub in the Power Amplifying Stage

An output equivalent circuit of the power cell with two GaN HEMTs can be represented as a combination of a series parasitic drain inductor L_d and a parallel circuit of a drain-source resistor R_{ds} and a drain-source capacitor C_{ds}, as shown in Fig. 7 [10]. The output impedance Z_d tends to be capacitive at a low frequency region and inductive at a high frequency region. For wideband matching, the output impedance with a low-Q value is required, which is obtained through the reactance compensation for Z_d. The reactance compensation can be achieved using a shorted stub that is inductive at a lower frequency region and capacitive at a higher frequency region than the resonant frequency, where the electrical length of the shorted stub is 90°.

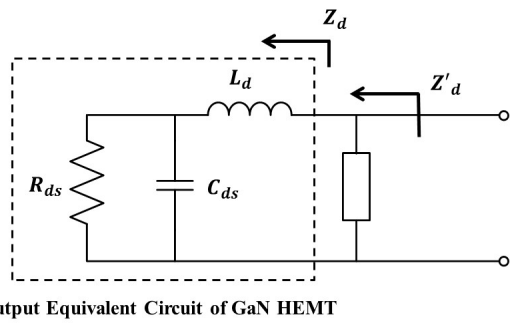

Fig. 7. An output equivalent circuit of the power cell and a shorted stub to compensate its output reactance.

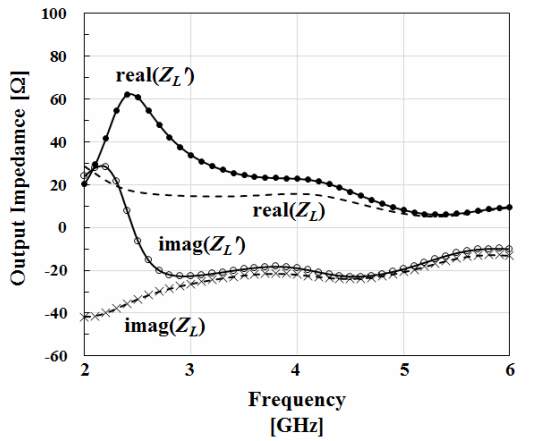

Fig. 8. Reactance-compensation results for the power cell's output impedance using the shorted stub.

Fig. 8 shows the reactance compensation results by the shorted stub, which is added to the power cell to reduce the reactance term of the cell's output impedance Z_d. The resultant output reactance, the imaginary part of Z_d', is smaller than that of Z_d due to the shorted stub, while the real part of Z_d' increases, compared with that of Z_d. This leads to a low-Q impedance, which facilitates wideband load impedance matching for maximum output power. It is noticeable that the imaginary part of Z_d is negative because of a relatively low operating frequency.

The power cell with two 10 × 125 μm transistors in parallel is simulated in 2 to 6 GHz using a load-pull test in the Keysight ADS software, and the results are shown in Fig. 9. Under the load impedance condition for maximum output power, the power cell shows the output power of 38.8 to 40.1 dBm from 2 to 6 GHz. The designed load impedance of the power cell, which is obtained from the shorted stub and the additional LC low-pass ladder matching circuit, overlaps on the contour

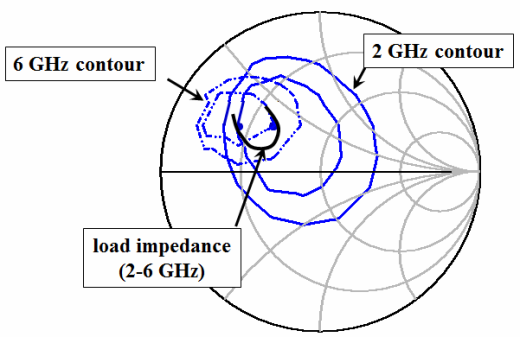

Fig. 9. Load-pull simulation results of the power cell in 2-6 GHz under the maximum output power condition and the locus of designed output load impedance (power step for the contour plot = 1.5 dB).

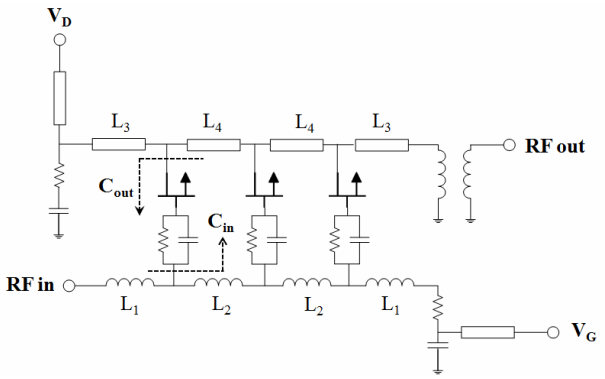

Fig. 10. A schematic circuit of the distributed driving amplifier.

plot with the power step of 1.5 dB, as shown in Fig. 9. The power cell's output load impedance is well-matched to the optimum load impedance from the load-pull simulation as shown in the figure.

3. Distributed Amplifier for the First Driving Stage

A distributed amplifier with good input/output return loss in a wide frequency range is used as the first-stage driving amplifier for the second power stage [11]. An input port of the circuit is matched to 50 Ω for system compatibility, and an output port is matched to 25 Ω because the input port of the second power stage is also matched to the same 25 Ω, which makes it possible to directly connect two stages in cascade. Fig. 10 shows a schematic circuit diagram of the designed distributed driving amplifier. To obtain the balance of phase velocity between input and output artificial transmission lines, the product of L_1C_{in} is designed to be equal to the product of L_3C_{out} under the conditions of $L_2 = 2 \times L_1$ and $L_4 = 2 \times L_3$.

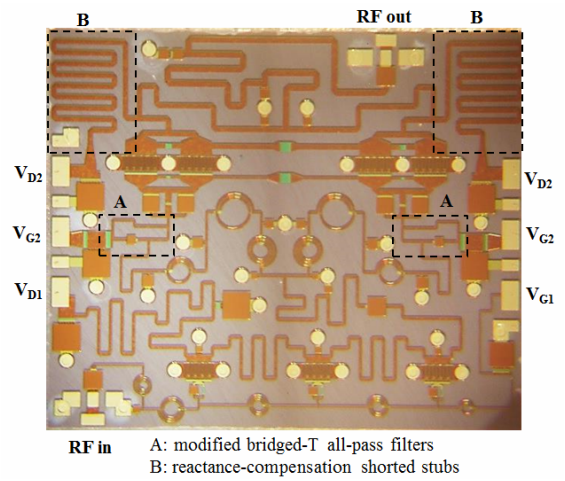

Fig. 11. A chip photograph of the fabricated 2-6 GHz GaN power amplifier MMIC with modified bridged-T all-pass filters and shorted stubs for reactance compensation of the transistor's output impedance.

III. Fabrication and Measurement

A chip photograph of the fabricated power amplifier MMIC is shown in Fig. 11, and its size is 4.0 mm × 3.4 mm. Input transmission lines of the first-stage distributed amplifier are realized using circular spiral inductors, and for its output transmission lines, microstrip lines are used to withstand high DC drain current at a saturated power condition. Two bridged-T all-pass filters (A in Fig. 11) are applied to the gates of two power cells of the second-stage power amplifier. An LC ladder low-pass circuit, which consists of microstrip lines, circular spiral inductors and shunt capacitors, is used for inter-stage matching. Two symmetrically feeding microstrip lines (B in Fig. 11) at the drain nodes of the second power stage that are terminated by high-value bypass capacitors are used to compensate the output reactance of the GaN HEMTs and also play a role in supplying bias voltage and current.

Fig. 12 compares measured S-parameter results of the fabricated 2-6 GHz GaN power amplifier MMIC with its simulated results from 1 to 7 GHz at the drain bias voltage of 28 V and total drain current of 810 mA. The measured data shows good agreement with the simulation data. The measured linear gain S_{21} is flat and maintains 20 dB or slightly higher up to 6 GHz, and input return loss is greater than 10 dB from 1 to 7 GHz. Good output return loss is also obtained with some ripples.

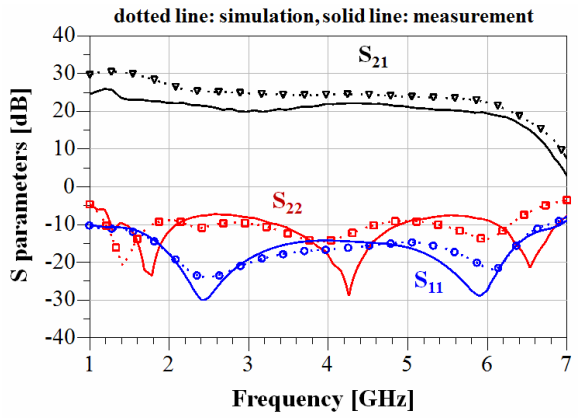

Fig. 12. Comparison of simulated and measured S-parameter results of the fabricated two-stage GaN power amplifier MMIC.

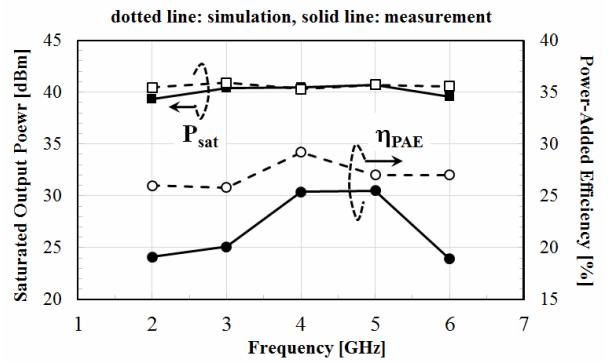

Fig. 13. Measured and simulated continuous-wave output power and power-added efficiency of the fabricated GaN power amplifier MMIC at the saturated power condition (V_{ds} = 28 V and $I_{ds,idle}$ = 810 mA).

Fig. 13 shows the measured continuous-wave output power and the power-added efficiency (PAE) at the saturated power condition in 2 to 6 GHz and compares them with simulated ones. The amount of gain compression at the power saturation ranges from 3.6 to 5.0 dB, and an average value of the saturated output power is about 40.1 dBm across the designed frequency range. The power-added efficiency is measured to be 18.9~25.5%, and the linear and power measurement results are in very good agreement with their counterparts from the simulation.

Comparison of this work and previously published wideband power amplifiers with state-of-the-art results is summarized in Table 2. Compared with the previous MMIC results, this work provides good input return loss, sufficient linear gain, and a reasonable PAE using simple techniques for input and output impedance matching while maintaining sufficient output power. When only the second power amplifying stage is considered, the PAE of this work is estimated to be 27-39 %, which is slightly higher than the PAE of Ref. [5].

Table 2. Comparison of the fabricated GaN power amplifier MMIC and previously published wideband power amplifiers with state-of-the-art results

Items	This work	Ref. [2]	Ref. [5]
Frequency [GHz]	2-6	2-6	2-6
Number of stages	2	2	1
Saturated output power [W]	10	7-10	12-14
Linear gain [dB]	20-23	14-20	13-14
Power added efficiency [%]	19-26	25-30	27-34
Input return loss [dB]	≥ 10	≥ 7	≥ 10
Matching technique	resistive	reactive	distributed
Size [mm^2]	13.6	23.0	7.6

V. CONCLUSIONS

The 10 W GaN power amplifier MMIC operating from 2 to 6 GHz is demonstrated using the 0.25 μm GaN HEMT foundry process of WIN Semiconductors, Inc. We apply the bridged-T all-pass filter configuration to the gate of the transistor in the second power stage for wideband impedance matching, and a shorted stub to the drain of the transistor in the second stage to achieve the low-Q output impedance by reducing the transistor's output reactance, which facilitates wideband load impedance matching for maximum output power. These matching techniques work well and make the desired performance obtainable. The measured flat gain of 20-23 dB, good input return loss of larger than 10 dB, average saturated output power of 40.1 dBm, and power-added efficiency of 19-26 % are measured in 2 to 6 GHz. The fabricated power amplifier MMIC will be used for the wideband applications such as communication jammers and electronic warfare systems.

ACKNOWLEDGMENTS

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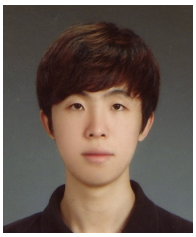

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Dong-Wook Kim received the B.S. degree in electronic communications from Hanyang University, Seoul, Korea, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1992 and 1996, respectively. In 1996, he joined the LG Electronics Research Center, where he developed high-power devices and monolithic microwave integrated circuits until 2000. From 2000 to 2002, he led research teams and developed RF integrated passive devices on a thick-oxidized Si substrate as a director of the research center in Telephus Inc. From 2002 to 2004, he was also involved with the development of wireless security systems in S1 Corporation, a company of Samsung Group. In 2004, he joined the faculty of Chungnam National University, Daejeon, Korea and is currently with it. In 2009, he was also with the Electronics and Telecommunications Research Institute (ETRI), as an invited researcher. In 2010, he was a visiting professor with the University of California at San Diego, La Jolla. His research interests are monolithic microwave integrated circuits and their applications, short-range radar modules, and ultra-wideband circuits and systems.