Design and Control Method for Sub-module DC Voltage Ripple of HVDC-MMC

Jin-Su Gwon*, Jung-Woo Park**, Dea-Wook Kang** and Sungshin Kim†

Abstract – This paper proposes a design and control method for a high-voltage direction current modular multilevel converter (HVDC-MMC) considering the capacitor voltage ripple of the sub-module (SM). The capacitor voltage ripple consists of the line frequency and double-line-frequency components. The double line- frequency component does not fluctuate according to the active power, whereas the line-frequency component is highly influenced by the grid-side voltage and current. If the grid voltage drops, a conventional converter increases the current to maintain the active power. A grid voltage drops, current increment, or both occur with a capacitor voltage ripple higher than the limit value. In order to reliably control an MMC within a limit value, the SM capacitor should be designed on the basis of the capacitor voltage ripple. In this paper, the capacitor voltage ripple according to the grid voltage and current are analyzed, and the proposed control method includes a current limitation method considering the capacitor voltage ripple. The proposed design and control method are verified through simulation using PSCAD/EMTDC.

Keywords: Capacitor voltage ripple, Capacitor design method, Current limit method, Double-line frequency, Modular multilevel converter (MMC).

1. Introduction

High-voltage direct current (HVDC) systems have several advantages: these systems are cheaper than an AC network for long-distance power transmission, do not affect the ac grid for AC/DC power conversion, are able to handle high-capacity power transmission, and are able to connect with other grid systems that have different frequencies. HVDC systems can be classified into current source converter-based HVDC (CSC-HVDC) with a thyristor and voltage source converter-based HVDC (VSC-HVDC) with an insulated-gate bipolar transistor (IGBT). CSS-HVDC systems were used in the majority of systems prior to 2010. However, recent VSC-HVDC systems have been actively studying the connection of offshore wind form systems as well as long-distance power transmission. A multilevel converter is widely used to configure VSC-HVDC systems [1, 2].

Multilevel converters are classified into diode-clamped multilevel converters (DCMCs), flying-capacitor multilevel converters (FCMCs), cascaded H-bridge converters (CHBCs), and modular multilevel converters (MMCs). MMCs have been widely adopted in VSC-HVDC systems. Fig. 1 shows the structure of an MMC consisting of six arms. Each arm is composed of an inductor and a series of connected half-

bridge sub-modules (SMs). HVDC-MMC systems require several design techniques. (1) System parameter design includes inductance and capacitance design and switching device current capacity design. (2) System control design includes power (DC-link voltage) control, AC-side current control, circulating current control, and SM voltage balancing [2-6].

A design method for the SM capacitance of the MMC was introduced in [7]. This design method calculated the difference in input energy according to the amplitude of the grid voltage and the active power. The SM capacitance is designed by the input energy and the SM capacitor voltage ripple on the basis of the limit value. The SM capacitor voltage ripple has line-frequency and double-line-frequency components. However, this design method did not separate line-frequency and double-line-frequency components; the capacitor voltage ripple was only calculated using integrated components.

Reference [8] introduced the design method of the arm inductors. An MMC possesses a voltage difference between the dc link and each arm with SMs, which leads to a problem in the circulating current in each arm. Therefore, reference [8] proposed a design method for the arm inductors considering the amplitude of the circulating current.

Reference [9] proposed a control method for an MMC under unbalanced voltage conditions. This control method proposed a dual-vector current control (DVCC) for the ac-side current controller in order to eliminate circulating currents and the dc-link voltage ripple. However, this control method has the disadvantage of the inclusion of a

† Corresponding Author: Dept. of Electrical Engineering, Pusan National University, Korea. (sskim@pusan.ac.kr)
* Dept. of Electrical Engineering, Pusan National University, Korea. (limpnirvana@gmail.com,)
** Power Conversion and Control Research Center, KERI, Korea. ({jwpark, dwkang}@keri.re.kr)

double-line-frequency ripple in ac-side active power by controlling ac-side negative-sequence currents to zero under unbalanced voltage conditions, and increasing the SM capacitor voltage ripple because it did not consider the capacitor voltage ripple.

Reference [10] proposed a control method for the circulating current and inner unbalanced current for an MMC under unbalanced voltage conditions. This control method consisted of DVCC for the ac-side current controller and had an advantage in that the active power did not fluctuate under the unbalanced voltage conditions. This method can also simultaneously control with positive-, negative-, and zero-sequence circulating currents. However, this method has the disadvantage of increasing the SM capacitor voltage ripple because of injection of the ac-side negative-sequence current.

A conventional design method of the SM capacitor was created by considering only the steady state, and a control method was designed by not considering the SM capacitor voltage ripple. Therefore, this paper proposes a design and control method for the SM capacitor for HVDC-MMCs considering the SM capacitor voltage ripple. For the design of the SM capacitor, it calculates the energy according to the ac-side rated voltage and current. The input energy has DC, line-frequency, and double-line-frequency components. The input energy is calculated. Among these, the input energy is calculated, the injected energy into the SM capacitor is extracted, and the SM capacitance is designed within the limit value of the capacitor voltage ripple according to the difference in the SM voltage by the energy variation.

The SM capacitor voltage ripple has line-frequency and double-line-frequency components. The double-line-frequency component corresponds with the amount of active power. Even if the line-frequency component is equal to the amount of active power, however, the line-frequency component has a different value because of the amplitude of the ac-side voltage and current. When the converter is maintained at a constant value, the active power is less than the undervoltage condition, and consequently, the double-line-frequency component is equal to the amplitude of the normal voltage condition, but the line-frequency component exceeds the capacitor voltage limit value. An SM capacitor voltage ripple higher than the rated value places stress on the switching elements and the SM capacitor, and a large overload can lead to destruction of the switching elements and SM capacitor. Accordingly, the HVDC-MMC must control the system while considering the SM capacitor voltage ripple in undervoltage conditions. Therefore, this paper configures the maximum current limit value considering the grid voltage and the maximum voltage limit value. The converter restricts SM capacitor voltage ripple to be less than the ac-side current limit in the undervoltage conditions. The proposed methods are simulated using PSCAD/EMTDC.
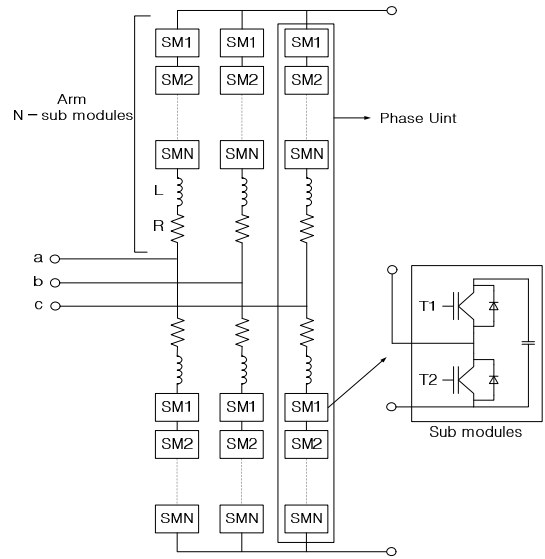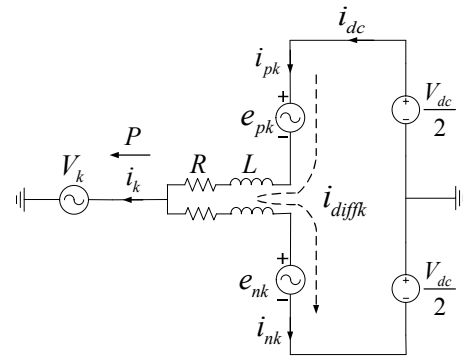
Fig. 1. Basic structure of MMC.

Fig. 2. Single-phase equivalent circuit of the three-phase MMC.

2. Basic Structure of the MMC

Fig. 2 shows a single-phase equivalent circuit of a grid-connected three-phase MMC. V_k is the grid voltage. i_{pk} and ink are the upper and lower arm currents, respectively. i_{diffk} is the inner unbalanced current. e_k is the converter output voltage. e_{pk} and e_{nk} (k = a, b, c) are the upper and lower arm voltages, respectively, where the subscripts p and n denote the upper and lower arms, respectively. According to Fig. 2 and [11], the corresponding ac-side voltage equation can be expressed as:

$$V_k = e_k - \frac{L}{2}\frac{di_k}{dt} - \frac{R}{2}i_k \tag{1}$$

$$L\frac{di_{diffk}}{dt} + Ri_{diffk} = \frac{V_{dc}}{2} - \frac{e_{pk}+e_{nk}}{2} \tag{2}$$

$$e_k = \frac{e_{nk}-e_{pk}}{2} \tag{3}$$

where V_{dc} is the dc bus voltage. L and R are the arm

inductance and equivalent arm resistance, respectively.

As shown in Fig. 2, the voltages of the upper arm and lower arm are expressed as:

$$e_{pk} = \frac{V_{dc}}{2} - V_k - Ri_{pk} - L\frac{di_{pk}}{dt} \tag{4}$$

$$e_{nk} = \frac{V_{dc}}{2} + V_k - Ri_{nk} - L\frac{di_{nk}}{dt} \tag{5}$$

The currents of the upper arm and lower arm are expressed in (6) and (7), respectively, and the inner unbalanced current is expressed in (8).

$$i_{pk} = i_{diffk} + \frac{i_k}{2} \tag{6}$$

$$i_{nk} = i_{diffk} - \frac{i_k}{2} \tag{7}$$

$$i_{diffk} = \frac{i_{dc}}{3} + i_{zk} \tag{8}$$

where i_{zk} is the circulating current.

3. SM Capacitor Parameter Design

From (4) and (5), R can be neglected because it is very small, and L can be neglected because it is designed by the amplitude of the SM capacitor and the circulating current and is smaller than the grid voltage. Eqs. (4) and (5) may be simplified to (9) and (10), respectively.

$$e_{pk} = \frac{V_{dc}}{2} - V_k = \frac{V_{dc}}{2} - V_m \sin\omega t \tag{9}$$

$$e_{nk} = \frac{V_{dc}}{2} + V_k = \frac{V_{dc}}{2} + V_m \sin\omega t \tag{10}$$

where V_m is the peak value of grid-side phase voltage.

The current equations of the arm (6)-(8) include the circulating current. However, the circulating current is neglected for simplification. Eqs. (6)-(8) may be simplified to (11) and (12).

$$i_{pk} = \frac{i_{dc}}{3} + \frac{i_k}{2} = \frac{i_{dc}}{3} + \frac{1}{2}I_m \sin(\omega t + \alpha) \tag{11}$$

$$i_{nk} = \frac{i_{dc}}{3} - \frac{i_k}{2} = \frac{i_{dc}}{3} - \frac{1}{2}I_m \sin(\omega t + \alpha) \tag{12}$$

where I_m is the peak value of the phase current.

The SM capacitor voltage ripple is determined by the input energy into the SM capacitor according to the amount of ac-side power. Instantaneous power of the arm can be expressed by multiplication of the voltage and current as follows:

$$p_{pk} = e_{pk}i_{pk}$$
$$= \frac{V_{dc}i_{dc}}{6} - \frac{V_m I_m}{4}\cos(\alpha) + \frac{V_m I_m}{4}\cos(2\omega t + \alpha)$$
$$- \frac{V_m i_{dc}}{3}\sin\omega t + \frac{V_{dc}I_m}{4}\sin(\omega t + \alpha) \tag{13}$$

The instantaneous power has dc and ac components. Among these components, only the ac component is stored in the arm [9]; hence, only the ac component in (13) is represented as (14). In (14), α is zero because in the MMC, assuming a unit power factor control, the grid-side voltage and current have identical phase. Therefore, (14) may be rearranged to (15). In (15), the first term is the line-frequency component, and second term is the double-line-frequency component. The stored energy in the arm, which is calculated by (15), may be expressed as (16), and the peak value may be expressed as (17).

$$p_{pk\_AC} = \frac{V_{dc}I_m}{4}\sin(\omega t + \alpha)$$
$$+ \frac{V_m I_m}{4}\cos(2\omega t + \alpha) - \frac{V_m i_{dc}}{3}\sin\omega t \tag{14}$$

$$p_{pk\_AC} = \left(\frac{V_{dc}I_m}{4} - \frac{V_m i_{dc}}{3}\right)\sin(\omega t)$$
$$+ \frac{V_m I_m}{4}\cos(2\omega t) \tag{15}$$

$$W_{pk\_AC} = \int p_{pk\_AC}dt$$
$$= \frac{1}{\omega}\left(\frac{V_{dc}I_m}{4} - \frac{V_m i_{dc}}{3}\right)\cos(\omega t)$$
$$- \frac{V_m I_m}{4*2\omega}\sin(2\omega t) \tag{16}$$

$$\left|\Delta W_{pk\_AC\_peak}\right|$$
$$= \frac{1}{\omega}\left(\frac{V_{dc}I_m}{4} - \frac{V_m i_{dc}}{3}\right) + \frac{V_m I_m}{4*2\omega} \tag{17}$$

The stored energy in the SM capacitor is expressed in (18), and difference in the SM capacitor energy is equal to the stored energy in the arm. Eq. (18) can replace the difference in the capacitor energy with the difference in the SM capacitor voltage; thereby, (18) can be expressed as (19):

$$W_{SM\_Total} = W_{pk\_AC}$$
$$= \frac{1}{2}\frac{C_{Arm}}{N}V_{SM\_total}^2 \tag{18}$$

$$\Delta W_{SM\_Total} = \Delta W_{pk\_AC\_peak}$$
$$= \frac{1}{2}\frac{C_{SM}}{N}\left[-2V_{total}\Delta V_{total} - (\Delta V_{total})^2\right] \tag{19}$$

where C_{Arm} is the SM capacitance, N is the number of SMs, V_{SM_total} is the sum of the SM capacitor voltage, V_{total} is the
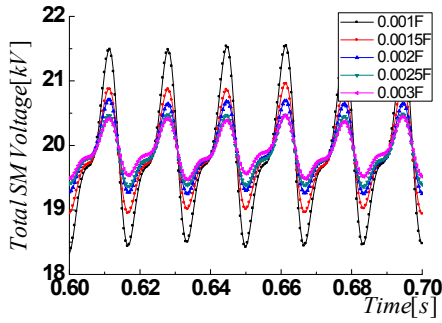
Fig. 3. Simulation results of the arm capacitor voltage ripple varying the SM capacitance.

Table 1. Main circuit parameters

Parameter	Value
DC-link Voltage($V_{total}=V_{dc}$)	20,000[V]
Rated Power	4[MW]
SMs	10[EA]
Grid Frequency	60[Hz]
Rated Grid Voltage (Line to Line)	11,500[V]
Arm Voltage Ripple Limit(ΔV_{total}) 5%	1000 [V]

Table 2. Arm capacitor voltage ripple varying the SM capacitance.

Capacitance	ΔV_{total}(Calculation)	ΔV_{total}(Simulation)
0.001 F	1442 V	1529 V
0.0015 F	972 V	949 V
0.002 F	734 V	702 V
0.0025 F	589 V	546 V
0.003 F	492 V	449 V

sum of the SM capacitor voltage per arm at steady state, which is equal to the dc bus voltage, and ΔV_{total} is the difference in the total SM capacitor voltage.

The difference in the arm capacitor voltage can be expressed as (20) from (19), and the capacitance of the SM capacitor can be also expressed as (21) from (19). Therefore, the SM capacitance is calculated by substituting the main circuit parameters (standard design specification) of the MMC in (21). The main circuit parameters and operating condition are listed in Table 1.

Fig. 3 shows the simulation results of the difference in the arm capacitor voltage according to the SM capacitance. Table 2 shows the result of both the calculated difference in the arm capacitor voltage and the simulated difference in the arm capacitor voltage. In order to restrict the arm voltage ripple to less than 1000 V under the rated power condition, a value of more than 0.0015 F must be chosen for the SM capacitor. Therefore, a value of 0.002 F for the SM capacitance considering the voltage ripple margin is selected.

$$\Delta V_{total} = \frac{1}{2}\left[\begin{array}{c} -2V_{total} \\ +\sqrt{\left(-2V_{total}\right)^2 + \dfrac{8NW_{pk\_AC}}{C_{SM}}} \end{array} \right] \quad (20)$$
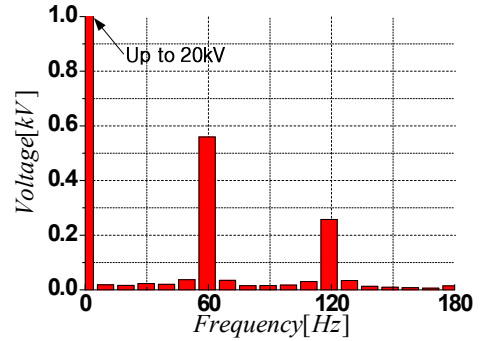
Fig. 4. FFT analysis of the arm capacitor voltage ripple.

Table 3. Arm capacitor voltage ripple component of line frequency and double-line frequency.

0.002 F	Calculation	Simulation
Line frequency	520 V	559 V
Double line frequency	220 V	257 V

$$C_{SM} = \left| \frac{2NW_{pk\_AC}}{-2V_{total}\Delta V_{total} - \left(\Delta V_{total}\right)^2} \right| \quad (21)$$

Fig. 4 shows the result of a fast Fourier transform (FFT) of the arm voltage when the SM capacitance is 0.002 F. The amplitude of the calculated capacitor voltage ripples and the results of the FFT in the simulation of the ripple components are shown in Table 3. There are similar results which compare the calculated capacitor voltage ripple and the result of the FFT in the simulation. Therefore, not only the total arm capacitor voltage ripple but also the line-frequency and double-line-frequency components can be calculated.

4. Current Limit Method

4.1 AC-side current reference

If the grid voltage is at steady state, the grid-side voltage and current have only positive sequences. The ac-side active power and reactive power can be expressed as (22) and (23).

$$P_{AC} = \frac{3}{2}\left(V_d^p i_d^p + V_q^p i_q^p\right) \quad (22)$$

$$Q_{AC} = \frac{3}{2}\left(V_q^p i_d^p - V_d^p i_q^p\right) \quad (23)$$

where P_{AC} is the ac-side active power, Q_{AC} is the ac-side reactive power, superscript p is the positive sequence component, and subscripts d and q are the rotational reference frame d- and q-axes, respectively.

If the positive-sequence d-axis voltage is determined to

be zero through the phase-locked loop (PLL), the ac-side current reference according to the active power and reactive power reference can be expressed as (24) and (25).

$$i_q^{p*} = \frac{2}{3}\frac{P_g^*}{V_q^p} \qquad (24)$$

$$i_d^{p*} = \frac{2}{3}\frac{Q_g^*}{V_q^p} \qquad (25)$$

4.2 Current limit method considering current capacity of switching elements

In the case of the two-level converter, the injected current into the switching device is equal to the ac-side current. However, in the MMC, the current is injected into the switching elements, not only the ac component but also the dc component into the switching device, because this current is equal to the arm current. Hence, we have to restrict the current considering the dc component. The arm current of the MMC is expressed as (6) to (8), and if the circulating current is controlled to zero, the ac-side current can be expressed as (26) and (27).

$$i_k = 2\left(i_{pk} - \frac{i_{dc}}{3}\right) \qquad (26)$$

$$i_k = -2\left(i_{nk} - \frac{i_{dc}}{3}\right) \qquad (27)$$

In (26) and (27), if the arm current is restricted to the current capacity of the switching device, the allowed ac-side maximum current can be expressed as (28).

$$I_{k\_peak} = 2\left(i_{SM\_peak} - \left|\frac{i_{dc}}{3}\right|\right) \qquad (28)$$

4.3 Current limit method considering SM capacitor voltage ripple

The SM capacitor voltage ripple in (14) to (20) is determined according to the amplitude of the grid-side voltage, current, and dc-link current. In (15), the double-line-frequency component is multiplied by the grid-side voltage and current. If the active power does not fluctuate, the double-line-frequency component has constant amplitude. However, the fundamental frequency component fluctuates depending on the grid-side voltage and current, even though the active power does not fluctuate. Hence, the control method considering the SM capacitor voltage ripple under the undervoltage conditions is needed because the SM capacitor voltage ripple increases in the undervoltage conditions.

The SM capacitor voltage ripple is determined by the

input energy. Therefore, it has to restrict the injected energy into the SM capacitor within the acceptable range to restrict the ripple of the SM capacitor voltage. The injected energy into the SM capacitor consists of the function of the grid-side voltage, current, and dc-link current as in (17). The grid-side voltage is determined by external factors, and the dc-link current is determined by the grid-side voltage and current. Hence, the grid-side current must be restricted to limit the ripple of the SM capacitor voltage because the controllable variable is the grid-side current. Because (17) includes the dc-link current component, this is converted to the grid-side current component and may be simplified. If no regard is given to the loss of the MMC, then the active power of the ac-side and dc-side of the MMC may be expressed as (29).

$$\begin{aligned} P_{AC} &= P_{dc} \\ &= V_{dc}i_{dc} \\ &= 1.5\left(V_d i_d + V_q i_q\right) \end{aligned} \qquad (29)$$

where subscripts d and q denote the d- and q-axis components in the rotational reference frame, respectively.

If the positive-sequence d-axis voltage is determined to be zero through the PLL, the amplitude of the q-axis current that is equal to the peak value of the phase current may be defined as in (30).

$$i_{dc} = \frac{1.5\left(V_d i_d + V_q i_q\right)}{V_{dc}} = \frac{1.5\left(V_m I_m\right)}{V_{dc}} \qquad (30)$$

Hence, the peak value of the energy is derived by a function of the grid-side voltage, current, and the dc-link voltage by substituting (30) into (17). The peak of the phase current may be expressed as (32) with respect to the grid-side current in (31). Therefore, when the ac-side current reference is restricted to the current limitation value, the SM capacitor voltage ripple can be restricted within the limit value.

$$\left|W_{p\_AC\_peak}\right| = \frac{\left(\frac{V_{dc}I_m}{4} - \frac{1.5V_m^2 I_m}{3V_{dc}}\right)}{\omega} + \frac{V_m I_m}{4*2\omega} \qquad (31)$$

$$I_{m\_peak} = \frac{\left|W_{p\_AC\_peak}\right|}{\frac{V_{dc}}{4\omega} - \frac{1.5V_m^2}{3\omega V_{dc}} + \frac{V_m}{4*2\omega}} \qquad (32)$$

Fig. 5 shows the rated current of the switching elements and the current limitation method considering the arm capacitor voltage ripple. The d- and q-axis current references are determined by the initial values of the active power and reactive power, respectively, and the control
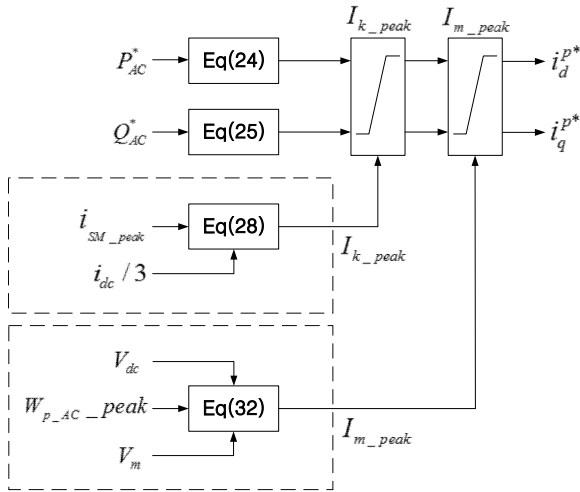
Fig. 5. Proposed current limitation method scheme considering the current capacity and the arm capacitor voltage ripple.
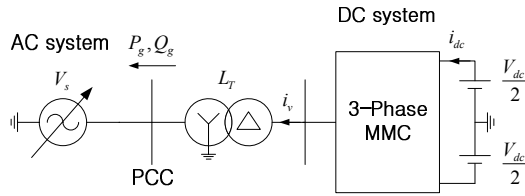

Fig. 6. System structure of simulations.

method consists of part of the current limit considering the restriction of the current reference and the arm capacitor voltage ripple.

5. Simulation Results

Fig. 6 shows the system structure of the simulations using PSCAD/EMTDC. The parameters used in the simulation are listed in Table 1. The PWM method and balancing algorithm of the SM capacitor voltage are used in the modified PSC-PWM method in [11].

Fig. 7 shows the simulation results, which show the rated current of the switching elements and the ripple of the arm capacitor voltage considering the current limitation method. The simulation conditions are as follows:

(1) **Mode 1** (0.3–0.4 s): zero power control under the rated voltage condition.

(2) **Mode 2** (0.4–0.7 s): active power is 4-MW load, and reactive power is 0-MVA load under the rated voltage condition.

(3) **Mode 3** (0.7–0.9 s): reactive power is 0 MVA, and active power is limited by current limit considering the voltage ripple of the arm capacitor under the low-voltage condition in which the voltage is reduced by 50%.

Fig. 7(a) and (b) shows the grid-side voltage and current. The grid-side current is increased to maintain the active
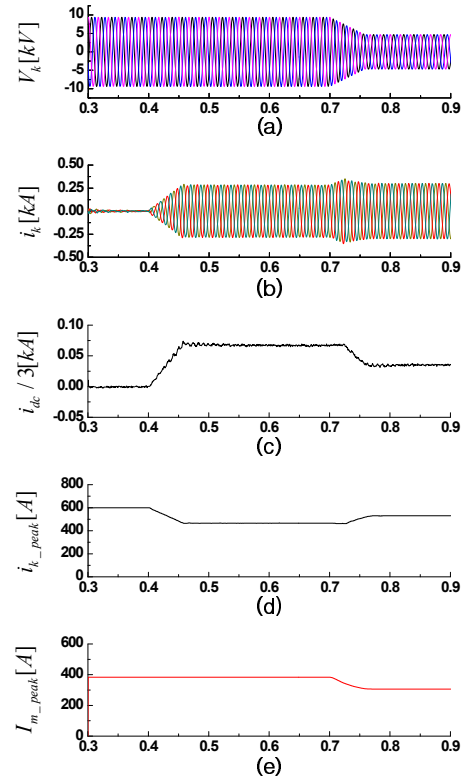

Fig. 7. Simulation results of the proposed control method under the low-voltage condition: (a) grid-side voltage; (b) grid-side current; (c) $i_{dc}/3$ component; (d) current limit value considering the current capacity of the switching element, and (e) current limit value considering the arm capacitor voltage ripple.

power at 0.7 s in undervoltage conditions. However, in order to restrict the switching element ripple and arm capacitor voltage, the grid-side current is confirmed to have a constant value by the current limit value. Fig. 7(c) shows the $i_{dc}/3$ component. It can be confirmed that the dc-link current is reduced by the current limit condition to restrict the active power at 0.7 s. Fig. 7(d) shows the limited current value considering the rated current of the switching elements. According to the increase in the dc-link current in the mode-2 section to increase the active power, it can be confirmed that the peak of the ac-side current reference is reduced by the current limit condition of (23). In the case of the mode-3 section to the grid-side undervoltage conditions, the active power is reduced by the current limitation condition considering the arm capacitor voltage ripple. It can be confirmed that the current limit value is increased by the reduced amplitude of dc-link current. Fig. 7(e) shows the current limit value considering the arm capacitor voltage ripple. The current limit value is constant under the rated voltage condition. However, in case of the mode-3 section for the grid-side undervoltage conditions, it can be confirmed that the current limit value is reduced in order to restrict the ripple of the arm capacitor

voltage.

Fig. 8 shows results of simulation according to the current limit control method. Fig. 8(A) shows the results of the simulation of the conventional control method without the current limit control method, Fig. 8(B) shows the results of the simulation of the current limit control method considering the current capacity of the switching device, and Fig. 8(C) shows the results of the simulation of the current limit control method considering the current capacity of the switching device and the arm capacitor voltage ripple. At first, the active power reference is 4 MV, and reactive power reference is 0 MVA. The ac-side voltage in the undervoltage condition is reduced from 1.0 to 0.5 pu for 0.05 s at 0.7 s. Fig. 8(a), (b), and (c) show the ac-side voltage, current, and q-axis current. As shown in Fig. 8(A), it can be confirmed that the ac-side current is increased to maintain a 4-MW active power during the undervoltage conditions. As shown in Fig. 8(B), the ac-side current is increased by the undervoltage conditions, but this ac-side current is less than that in Fig. 8(A) because the

controlled current is restricted within the current capacity range of the switching elements. As shown in Fig. 8(C), the ac-side current is increased by the undervoltage conditions, but when compared with other methods, this ac-side current is less than the other current because of the current limit condition to restrict the arm capacitor voltage ripple. Fig. 8(d) shows the flowing arm current in the switching elements and the rated current of system. As shown in Fig. 8(A), the arm current exceeds the current capacity of the switching elements because it does not contain the current limit method. As shown in Fig. 8(B), however, the flowing arm current in the switching element is controlled to the same amplitude of the current capacity of the switching elements because this arm current has been restricted to the current limit value of the current capacity of the switching elements. As shown in Fig. 8(C), the arm current is controlled to be less than the current capacity of the switching elements because this arm current is restricted to be within the arm capacitor voltage ripple that is less than the current capacity of the switching elements. Fig. 8(e)
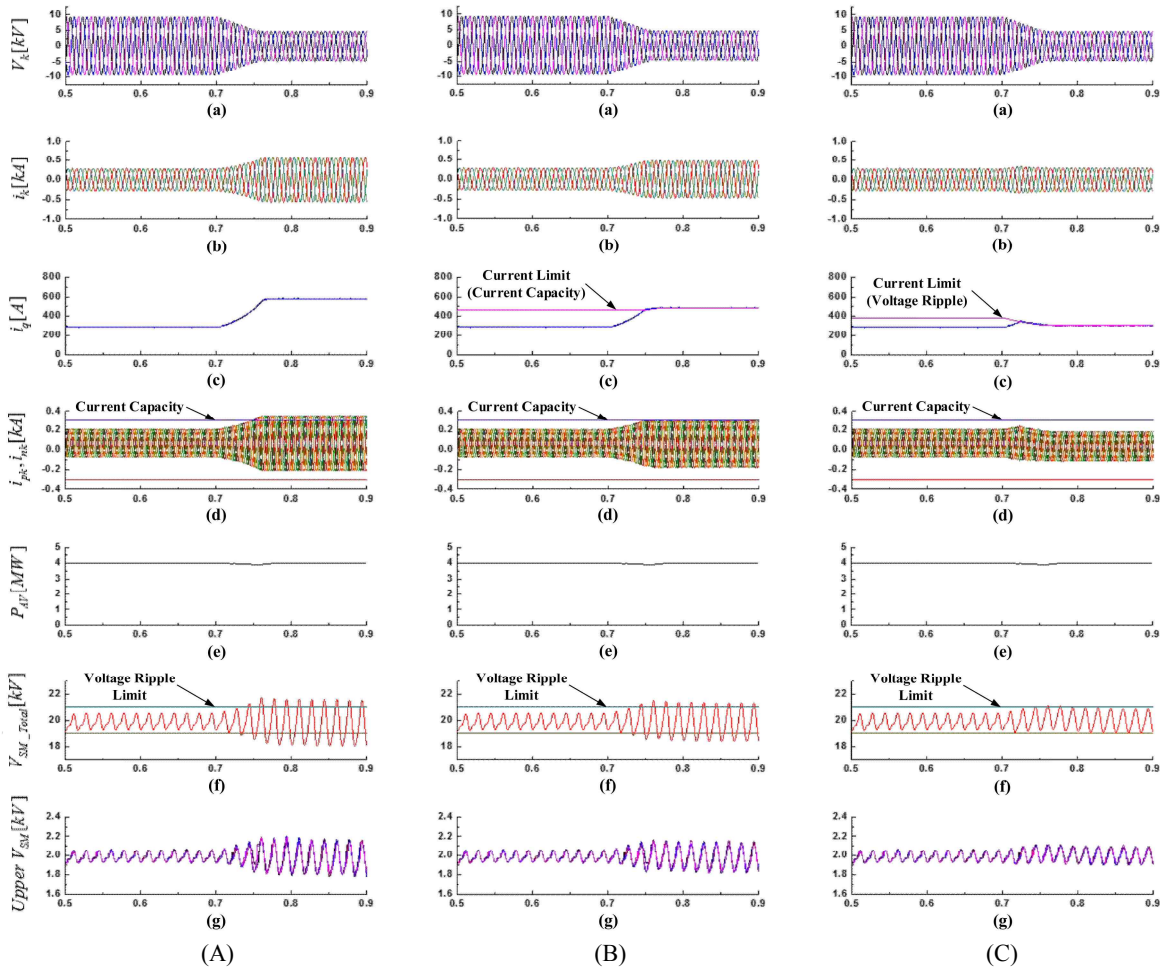

Fig. 8. Simulation results of various control methods under the low-voltage condition: (a) grid-side voltage; (b) grid-side current; (c) ac-side q-axis current; (d) arm current; (e) ac-side active power; (f) SM capacitor voltage ripple limit value; (g) upper arm SM capacitor voltage; (h) lower arm SM capacitor voltage. (A) Conventional method [9], (B) conventional method [10], and (C) proposed method.

shows the ac-side active power: As shown in Fig. 8(A), the ac-side active power is controlled to 4 MW because there is no current limit method. As shown in Fig. 8(B), however, the active power is reduced because this arm current is restricted to be less than the current limit value considering the current capacity of the switching elements. As shown in Fig. 8(C), the active power is similarly reduced because this arm current is restricted to less than the current limit values considering both the current capacity of the switching elements and the arm capacitor voltage ripple. Fig. 8(f) and (g) shows the arm capacitor voltage and the upper arm SM voltage. As shown in Fig. 8(A), the arm capacitor voltage exceeds the limit value of 1000 V because it does not contain the current limit method. As shown in Fig. 8(B), the arm current is restricted to be within the current capacity of the switching elements, but the arm capacitor voltage ripple still exceeds the limit value of 1000 V. As shown in Fig. 8(C), the arm capacitor voltage ripple does not exceed the limit value of 1000 V. Therefore, in order to restrict the arm capacitor voltage ripple and the ac-side current to within the limit values, it can be confirmed that the current limit method must consider not only the current capacity of switching elements but also the arm capacitor voltage ripple.
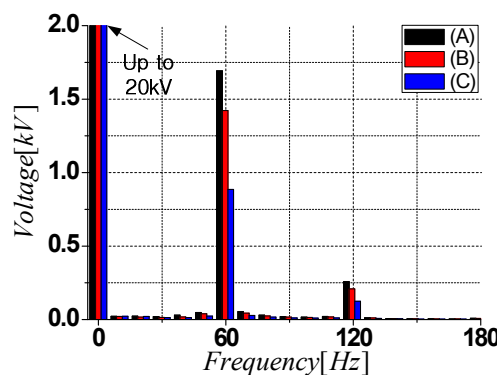

Fig. 9. FFT analysis of the arm capacitor voltage ripple under the low-voltage condition.

Table 4. Arm Capacitor Voltage Ripple Component of Various Control Methods Under the Low-voltage Condition.

(A)	Calculation	Simulation
Line Frequency	1611 V	1692 V
Double Line Frequency	220 V	258 V
Total	1815 V	1735 V

(B)	Calculation	Simulation
Line Frequency	1339 V	1421 V
Double Line Frequency	182 V	208 V
Total	1510 V	1460 V

(C)	Calculation	Simulation
Line Frequency	885 V	885 V
Double Line Frequency	119 V	125 V
Total	999 V	914 V

Fig. 9 shows the result of Fourier transform of the arm capacitor voltage in Fig. 8. Table IV shows the calculated respective components using (20) and the results of the simulation. The double-line-frequency component is proportional to the product of the ac-side voltage and current in (20). As shown in Fig. 9(A), in order to maintain the active power, the amplitude of the ac-side current was increased proportionally to the reduction ratio, and thereby, the amplitude of the double-line-frequency component is equal to that in Table 3, whereas the fundamental frequency component was increased three times compared with the value in Table 3. As shown in Fig. 9(B), the total voltage ripple is reduced by the current limit method considering the current capacity of the switching elements, but the voltage ripple exceeds the tolerance. As shown in Fig. 9(C), however, the total voltage ripple is restricted to less than 1000 V by the current limit method considering both the current capacity of the switching elements and the arm capacitor voltage ripple. Therefore, the proposed control method can control the arm capacitor voltage ripple within the limit value in undervoltage conditions, and when designing the arm capacitor of the MMC, this method has advantages for the estimated arm capacitor voltage ripple that can be considered in a design.

5. Conclusion

In this paper, a design method for the SM capacitance and a control method considering the SM capacitance and voltage ripple are proposed for an MMC. In order to design the SM capacitance, the arm capacitor voltage ripple is calculated and analyzed according to the ac-side voltage and current. In order to restrict the arm capacitor voltage ripple to within the limit value, we have proposed a current limit method considering the arm capacitor voltage ripple. The proposed control method can stably control an HVDC-MMC in undervoltage conditions. The arm capacitor voltage ripple was restricted to be within a constant value, which was verified through simulation, and was compared with the control method considering the current capacity of the switching element.

## References

[1] N. Flourentzou, V.G. Agelidis, and G.D. Demetriades, "VSC-based HVDC power transmission systems: An

overview," IEEE Trans. Power Electron., vol. 24, no. 3, pp. 592-602, Mar. 2009.

[2] B. Andersen, L. Xu, P. J. Horton, and P. Cartwright, "Topologies for VSC transmission," Power Eng. J., vol. 16, no. 3, pp. 142-150, Jun. 2002.

[3] Elisabeth N. Abildgaard, Marta Molinas, "Modelling and Control of the Modular Multilevel Converter (MMC)," Energy Procedia, Volume 20, 2012, Pages 227-236.

[4] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular Multilevel Converter With Different Submodule Concepts — Part II: Experimental Validation and Comparison for HVDC Application," Industrial Electronics, IEEE Transactions on , vol. 60, no. 10, pp. 4536, 4545, Oct. 2013.

[5] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A Steady-State Analysis Method for a Modular Multilevel Converter," Power Electronics, IEEE Transactions on , vol. 28, no. 8, pp. 3702, 3713, Aug. 2013.

[6] A. Antonopoulos, L. Angquist, and H. P. Nee, "On dynamics and voltage control of the modular multilevel converter," in Proc. Eur. Conf. Power Electron. Appl., Barcelona, Spain, 2009, pp. 1-10.

[7] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in Proc. Int. Conf. Power Electron. Appl., Lille, France, 2013, pp.1-10.

[8] Q. Tu, Z. Xu, H. Huang, and J. Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based HVDC," in Proc. Int. Conf. Power Syst. Technol., Hangzhou, China, 2010, pp. 1-6.

[9] Q. Tu, Z. Xu, Y. Chang, and L. Guan, "Suppressing DC voltage ripples of MMC-HVDC under unbalanced grid conditions," IEEE Trans. Power Del., vol. 27, no. 3, pp. 1332-1338, Jul. 2012.

[10] M. Ji-Woo, K. Chun-Sung, P. Jung-Woo, K. Dea-Wook, and K. Jang-Mok, "Circulating Current Control in MMC Under the Unbalanced Voltage," IEEE Trans. Power Del., vol. 28, no. 3, pp. 1952, 1959, July 2013.

[11] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," IEEE Trans. Power Del., vol. 26, no. 3, pp. 2009-2017, Jul. 2011.

[12] S. Li, T. Haskew, and L. Xu, "Control of HVDC light system using conventional and direct current vector control approaches," IEEE Trans. Power Electron., vol. 25, no. 12, pp. 3106-3118, Dec. 2010.

[13] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," IEEE Trans. Power Del., vol. 25, no. 4, pp. 2903-2912, Oct. 2011.

[14] M. Ji-Woo, G. Jin-Su, P. Jung-Woo, K. Dea-Wook, and K. Jang-Mok, "Model Predictive Control With a Reduced Number of Considered States in a Modular Multilevel Converter for HVDC System," IEEE Trans. Power Del., vol. PP, no. 99, pp. 1,1.

[15] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion formodular multilevel converter," IEEE Trans. PowerDel., vol. 26, no. 1, pp. 298-306, Jan. 2011.

[16] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modelling, simulation and analysis of a modular multilevel converter for medium voltage applications," in Proc. IEEE Int. Conf. Ind. Technol., Vina del Mar, Chile, 2010, pp. 775-782.

[17] J. Xu, C. Zhao, W. Liu, and C. Guo, "Accelerated Model of Modular Multilevel Converters in PSCAD/EMTDC," IEEE Trans. Power Del., vol. 28, no. 1, pp. 129,136, Jan. 2013.

[18] Z. Yuebin, J. Daozhuo, G. Jie, H. Pengfei, and L. Zhiyong, "Control of modular multilevel converter based on stationary frame under unbalanced AC system," in Proc. 3rd Int. Conf. ICDMA., 2012, pp. 293-296.

[19] M. Saeedifard, R. Iravani, and J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 452-466, Feb. 2009.

[20] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J. C. Vannier, and M. Molinas, "An Energy-Based Controller for HVDC Modular Multilevel Converter in Decoupled Double Synchronous Reference Frame for Voltage Oscillation Reduction," Industrial Electronics, IEEE Transactions on, vol. 60, no. 6, pp. 2360, 2371, June 2013.

[21] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A Steady-State Analysis Method for a Modular Multilevel Converter," Power Electronics, IEEE Transactions on , vol. 28, no. 8, pp. 3702,3713, Aug. 2013.

[22] Cho, H., M. Sami Fadali, and K. Lee., "Online Parameter Estimation and Convergence Property of Dynamic Bayesian Networks." International Journal of Fuzzy Logic and Intelligent Systems 7.4 (2007): 285-294.

[23] Kim, Y., H. Song, and B. Lee. "Identification of Dynamic Load Model Parameters Using Particle Swarm Optimization." International Journal of Fuzzy Logic and Intelligent Systems 10.2 (2010): 128-133.

[24] Hur, Don. "Economic considerations underlying the adoption of HVDC and HVAC for the connection of an offshore wind farm in Korea." Journal of Electrical Engineering & Technology 7.2 (2012): 157-162.

[25] Quach, Ngoc-Thinh, et al. "An Application of Proportional-Resonant Controller in MMC-HVDC System under Unbalanced Voltage Conditions." Journal of Electrical Engineering & Technology 9.5

(2014): 1746-1752.

[26] Son, Gum Tae, Soo Hyoung Lee, and Jung-Wook Park. "Power Loss Modeling of Individual IGBT and Advanced Voltage Balancing Scheme for MMC in VSC-HVDC System." Journal of Electrical Engineering & Technology 9.5 (2014): 1471-1481.
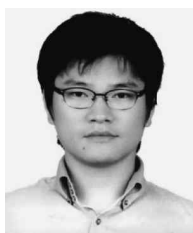
Jin-Su Gwon He received the B.S. and M.S. degrees in Information and Communication Engineering from Kyung-nam University, Masan, Korea, in 2009 and 2011, respectively, and is currently pursuing the Ph.D. degree in electrical engineering at Pusan National University, Busan, Korea. From 2009 to 2015, he was a Researcher in KERI, Changwon, Korea. Since 2015, he has been with Hyundai Elevator, Icheon, Korea. His present interests include control of HVDC, multilevel converters, renewable energy, Motor Drive and control.

Jung-Woo Park He received the B.S. and M.S. degrees in electronic engineering from Chungnam National University, Chungnam, Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from Kyungpook National University, Kyungpook, Korea. Since 1998, he has been a Principal Researcher with KERI, Changwon, Korea. His present interests include control of HVDC, multilevel converters, wind energy generation, and renewable energy.

Dae-Wook Kang He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Hanyang University, Seoul, Korea, in 1998, 2000, and 2004, respectively. Since 2004, he has been a Senior Researcher with KERI, Changwon, Korea. His interests include control of HVDC, multilevel converters, renewable energy, and the application of power electronics to power systems.

Sungshin Kim He received the B.S. and M.S degrees in electrical engineering from Yonsei University, Seoul, Korea, in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, in 1996. He is currently a Professor in the School of Electrical Engineering, Pusan National University, Busan, Korea. His research interests include intelligent control, intelligent robot, hierarchical learning structures, and fault diagnosis and prognosis.