Trade-Off Strategies in Designing Capacitor Voltage Balancing Schemes for Modular Multilevel Converter HVDC

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Abstract – This paper focuses on the engineering trade-offs in designing capacitor voltage balancing schemes for modular multilevel converters (MMC) HVDC: regulation performance and switching loss. MMC is driven by the on/off switch operation of numerous submodules and the key design concern is balancing submodule capacitor voltages minimizing switching transition among submodules because it represents the voltage regulation performance and system loss. This paper first introduces the state-of-the-art MMC-HVDC submodule capacitor voltage balancing methods reported in the literatures and discusses the trade-offs in designing these methods for HVDC application. This paper further proposes a submodule capacitor balancing scheme exploiting a control signal to flexibly interchange between the on-state and the off-state submodules. The proposed scheme enables desired performance-based voltage regulation and avoids unnecessary switching transitions among submodules, consequently reducing the switching loss. The flexibility and controllability particularly fit in high-level MMC HVDC applications where the aforementioned design trade-offs become more crucial. Simulation studies for MMC HVDC are performed to demonstrate the validity and effectiveness of the proposed capacitor voltage balancing algorithm.

Keywords: Modular multilevel converter (MMC), High voltage direct current (HVDC), Capacitor voltage balancing

1. Introduction

This paper investigates a crucial engineering trade-off in designing capacitor voltage balancing schemes for a modular multilevel converter (MMC) HVDC: voltage regulation performance and switching loss. The MMC has numerous stacks of identical converters called submodules [1-5]. For the half bridge configuration, a submodule has two switching devices implemented by antiparallel connections of a fully controllable insulated-gate bipolar transistor (IGBT) and capacitor to generate the output voltage [6] (See Fig. 1(b)). As the level of the MMC or the number of submodules increases to enable higher power transmission, the capacitor voltage balancing task becomes the primary technical challenge because the balancing scheme may adversely impact on system loss, device ratings as well as control performance, if not properly designed [7]. As conceptually illustrated in Fig. 1(a), there is a trade-off between voltage regulation performance and loss. The higher switching frequency generates the lower voltage ripple (ΔV) leading to better capacitor voltage

regulation for a given capacitance notwithstanding the higher switching loss. Large capacitance should allow for small voltage ripple and reduced loss due to reduced switching needs among submodules for the purpose of voltage balancing. It is worth noting that an ideal point in Fig. 1(a) provides the perfect voltage regulation and minimum loss comprising inherent conduction loss dominantly. However, the ideal point is prohibitively uneconomical for the high voltage applications because the ideal point can be achieved in extremely large submodule capacitance. The trade-off between voltage regulation and loss is balanced on the dotted line in practice. Ranking and switching all submodules by their capacitor voltages, often named 'Full Sorting' at every switching instant should provide the highest voltage regulation for the designed number of submodules and capacitance at the cost of highest switching loss. Thus, an operating point should be determined in technically and economically feasible operation range.

Because the capacitor voltage balancing should be the most basic yet critical functionality of the MMC, various balancing techniques of the capacitor voltage have been discussed in [1-18]. Reference [1] deals with two types of pulse width modulated MMC (PWM-MMC), focusing on their circuit configurations and voltage balancing control. Combining both averaging and balancing controls enables the PWM-MMC to achieve voltage balancing and the results are verified by simulation and experiment. In [2],
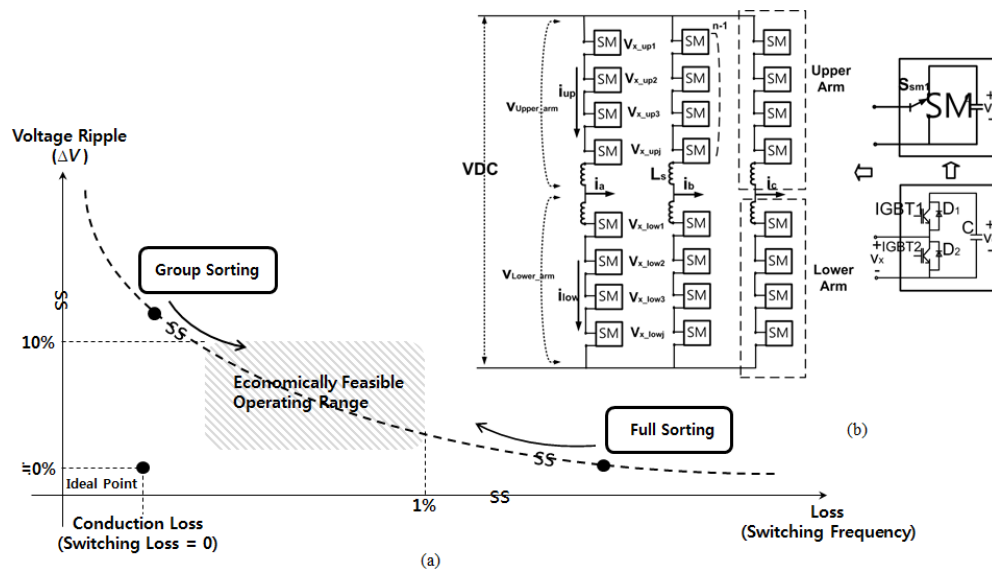
Fig. 1. (a) Engineering Trade-off in Designing MMC System. (b) MMC Topology

three capacitor voltage balancing strategies are proposed and investigated: 1) a slow-rate balancing strategy based on the conventional sorting method; 2) a hybrid balancing strategy that combines a predictive method with the conventional sorting method; and 3) a fundamental frequency balancing strategy. A computationally efficient voltage balancing algorithm without arm current measurements has been proposed [3]. The method reduces the number of the sensors and decreases the costs. A reduced switching frequency voltage balancing algorithm is developed for MMC, and a circulating current-suppressing controller is proposed for the three-phase MMC in [6]. This voltage balancing algorithm reduces the average device switching frequency and distributes the energy equally among the submodule capacitors. The combination of Nearest Level Modulation (NLM) and optimized capacitor voltage balancing control using a maintaining factor reduces the switching frequency as well as the switching losses of semiconductors in [7]. Closed loop control for the submodule voltage balancing is introduced with Carrier Phase Shifted Pulse Width Modulation (CPSPWM) in [8] and [9]. The submodule capacitor voltage balancing with phase disposition PWM (PDPWM) for MMC is used in [10-13]. The submodule capacitor voltages within each arm are measured and sorted, and the number of submodules to be switched on/off is determined. These methods have to be executed at the equivalent switching frequency of one arm, posing a heavy computational burden as the number of submodules becomes increasing to a real high voltage system. The balancing methods in [14-16] are based on a sorting method and individual measurement of submodule capacitor voltages, selecting the process based on the direction of the arm current for charging/discharging the selected submodule. It is obvious, however that the heavy computational intensity may hamper their applications to

high voltage (or level) systems. It is also interesting to note methods of using extra switching devices and capacitors for the self-balancing of voltages among modules in [17] and the prediction of each capacitor voltage as a function of the arm current and the states of the submodule switches [18]. A reduced the switching frequency based on the full sorting are proposed [6, 7]. The methods help reduce the system loss as illustrated in Fig. 1(a) while possibly compromising the voltage regulation.

The voltage balancing performance, however, has been investigated and validated for MMC with a small number of levels using high switching frequency modulation schemes. Higher switching frequency allows for better regulation at the cost of higher loss, which becomes the critical constraint for a high voltage application requiring a large number of levels. Therefore, a modulation method should be designed to generate a waveform with a large number of levels with minimal switching frequency that still guarantees the desired balancing performance. This research develops an effective balancing scheme based on the Group Sorting where submodules are grouped and sorted by prior switching states (on or off) [19] with supplementary ad-hoc switchings. These 'ad-hoc' switchings are commanded to interchange the highest voltage capacitor with the lowest voltage capacitor based on the current direction in order to maintain the desired voltage regulation performance. The low switching frequency modulation such as NLM is set as a basis to minimize system loss and it changes the on/off state of submodules based on the current direction that overrides the charge and discharge condition of the submodule to keep the desired voltage regulation. As the qualifier, ad-hoc implies, the method can adjust the switching frequency and should bring significant benefits of system controllability and flexibility to comply with dynamically changing grid condition. The paper comprehensively addresses the

design trade-offs encountered in designing the high-level MMC with desired low switching frequency modulation, and further presents the advantages of the proposed voltage balancing method with numerous simulation studies in terms of total harmonic distortion (THD), switching frequency and submodule voltage waveforms. Understanding of these trade-offs should be highly beneficial for system planners.

This paper is organized as follows: Section 2 presents theoretical background on the design trade-off between the desired voltage regulation and switching loss. Section 3 describes balancing schemes based on the namely, Full Sorting, Advanced Full Sorting, and Group Sorting methods for MMC in respect to the design trade-off followed by an effective capacitor voltage balancing control method proposed in Section 4. Section 5 demonstrates the validity and effectiveness of the proposed method through simulation studies for MMC, in particular for HVDC based on PSCAD/EMTDC. Finally, conclusions are provided in Section 6.

2. Design Trade-off between the Voltage Regulation and Switching Loss

This section briefly provides a theoretical overview on the switching frequency and its impacts on the converter loss and voltage regulation performance, i.e. voltage ripple.

Semiconductor switching devices such as MOSFETs, and IGBTs inherently dissipate power during the switchings. Fig. 2 illustrates the switching characteristics of the generic
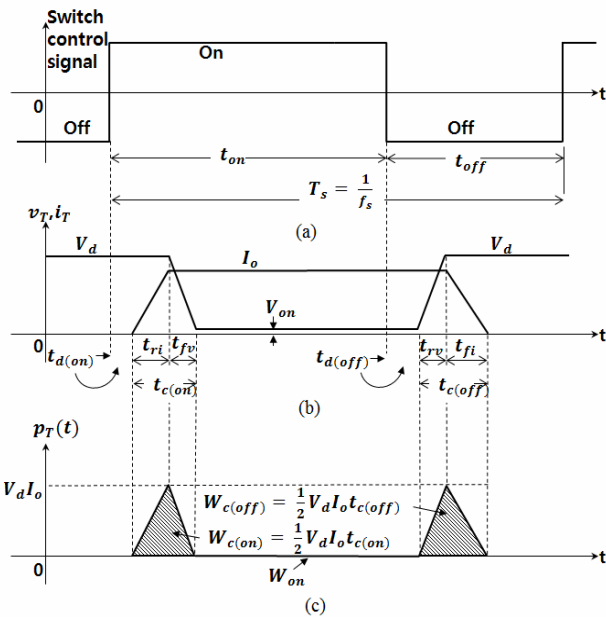
Fig. 2. Generic-switch switching characteristics: (a) switch waveforms; (b) voltage and current waveforms according to switch; (c) instantaneous switch power loss (adapted from [20]).

switching device and the switching loss due to voltage and current present simultaneously during the turn-on crossover interval $t_{c(on)}$, where

$$t_{c(on)} = t_{ri} + t_{fv} \tag{1}$$

and $t_{c(off)}$, where

$$t_{c(off)} = t_{rv} + t_{fi} \tag{2}$$

The energy dissipated in the switch during this turn-on and off transition can be approximated from Fig. 2(c) as

$$W_{c(on)} = \frac{1}{2} V_d I_o t_{c(on)} \tag{3}$$

$$W_{c(off)} = \frac{1}{2} V_d I_o t_{c(off)} \tag{4}$$

where any energy dissipation during the turn-on and turn-off delay interval $t_{c(on)}$ and $t_{c(off)}$ are ignored since they are much smaller than $W_{c(on)}$ and $W_{c(off)}$. It should also be noted that there are f_s such turn-on and turn-off transitions per second. Hence, the average switching power loss P_s in the switch due to these transitions can be approximated from (3) and (4) as

$$P_s = \frac{1}{2} V_d I_o f_s (t_{c(on)} + t_{c(off)}) \tag{5}$$

This fundamental relationship between the loss and the switching frequency surely indicates that the average switching loss can be controlled by the switching frequency [20].

Further, the dissipated energy by a submodule capacitor as its voltage drops from V_{peak} to V_{min} is expressed as follows [21]:

$$\frac{1}{2} C_{sm} V_{peak}^2 - \frac{1}{2} C_{sm} V_{min}^2 = P \Delta t \tag{6}$$

where C_{sm} is submodule capacitance and $P\Delta t$ is energy consumed (based on the assumption of constant power at P) during that time interval. Eq. (6) can be described the voltage term by

$$V_{peak}^2 - V_{min}^2 = \frac{2P\Delta t}{C_{sm}} \tag{7}$$

$$(V_{peak} - V_{min})(V_{peak} + V_{min}) = \frac{2P\Delta t}{C_{sm}} \tag{8}$$

$$(V_{peak} - V_{min}) = \frac{2P\Delta t}{C_{sm}(V_{peak} + V_{min})} \tag{9}$$

Small ripple approximation allows for the expression of voltage term on the right side as below:

$$V_{peak} + V_{min} \approx 2V_{peak} \qquad (10)$$

Δt can also be expressed as $\Delta t \approx T/2$. Since T is $1/f_s$, Eq. (9) can further be arranged as in the following:

$$(V_{peak} - V_{min}) = V_{peak-to-peak-ripple} \approx \frac{P}{2f_s C_{sm} V_{peak}} \qquad (11)$$

It is obvious that the lower the switching interval, the lower the $V_{peak-to-peak-ripple}$ as concisely presented below:

$$f_s \propto \frac{1}{V_{peak-to-peak-ripple}} \qquad (12)$$

Combining the observations above in (5) and (12), the relationship among frequency, voltage variation, and the loss can be summarized below:

$$f_s \propto \frac{P_s}{V_{peak-to-peak-ripple}} \qquad (13)$$

3. Capacitor Voltage Balancing Control

This section discusses three well reported methods for balancing the submodule capacitor voltage balancing control: Full Sorting, Advanced Full Sorting and Group Sorting. It then presents an effective balancing based on Group Sorting with a supplementary ad-hoc switching signal incorporating the design trade-off of voltage regulation and loss for each balancing method.

3.1 Full sorting

Full Sorting may be the most basic but intuitive method for ranking all the measured voltages of the submodule capacitors at every switching instant and sequencing an order for turning on or off switches. The governing law states that the on-state submodules charge the corresponding capacitors for positive arm current and discharge the capacitors for negative arm current. The off-state submodules are bypassed regardless of the current direction. If the arm current is in the positive direction, then the on-state submodules in an upper or lower arm with the lowest voltages are selected to be turned on. The corresponding capacitor voltages then increase due to the charging process. If the arm current is negative, then the on-state submodules with the highest voltages are selected to be turned off and the corresponding capacitor voltages decrease. The balancing control using this Full Sorting scheme is shown in Fig. 3. In order to reduce the sensing cost, the current direction information can be derived from the voltage difference of two subsequently measured voltage samples [22].

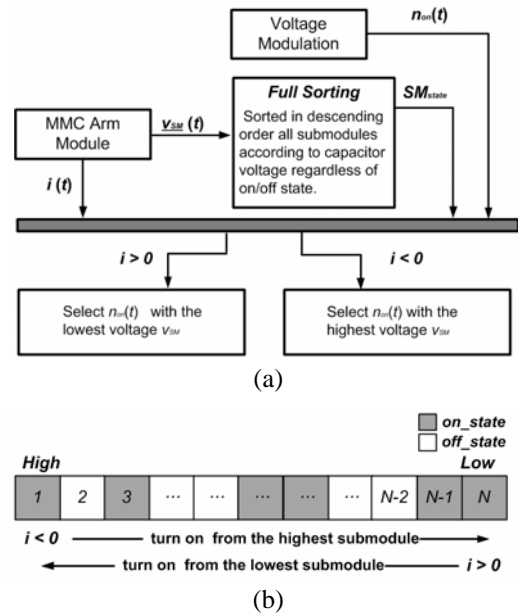Since it determines the on-state by checking the voltage

(a)

(b)

Fig. 3. The Full Sorting: (a) Schematic of Full Sorting; (b) Arrangement and operation of each submodule.

of each submodule capacitor at each sampling time, on/off switching of the submodule occurs frequently.

Therefore, voltage regulation of the capacitor performs best and harmonics of the generated voltage waveforms could be minimal; a method focusing on the improvement of voltage regulation performance represented on the y-axis in Fig. 1(a). However, the undesired high loss due to frequent switching is a critical constraint for high voltage applications as detailed with numerical data and graphs in Section 5.

3.2 Advanced full sorting

The Advanced Full Sorting optimizes the designing capacitor voltage balancing schemes by adjusting the measured submodule capacitor voltages before the next sorting process. At each sampling time, if the off-state (on-state) submodule capacitor voltage is smaller (greater) than the on-state (off-state) submodule capacitor voltage with the current direction, the submodule of the on/off state exchanges. Multiplying the actual capacitor voltage of the on-state submodule by a maintaining factor (greater than one) increases the likelihood of maintaining the present state and thus avoids the unnecessary switching [7] as illustrated in Fig. 4. The Advanced Full Sorting method may be understood as a way to move towards less loss on the x-axis of Fig. 1(a) while not compromising the voltage regulation too much; balancing a trade-off between the voltage regulation and the switching loss.
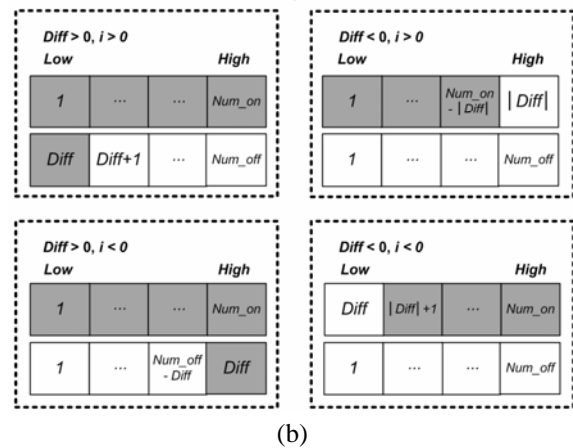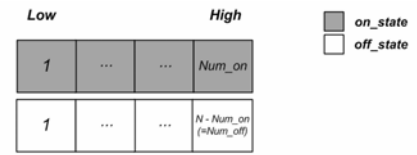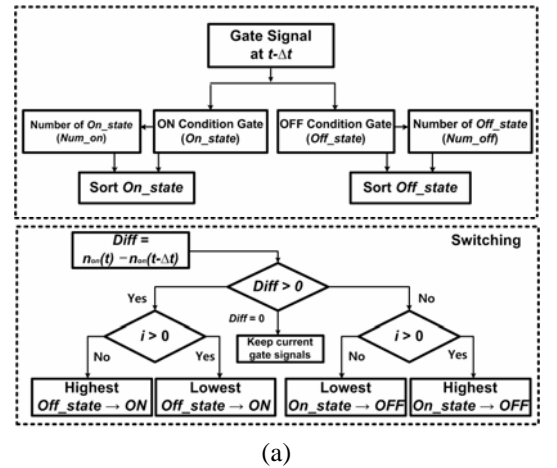
3.3 Group sorting

In order to avoid successive switching of the same
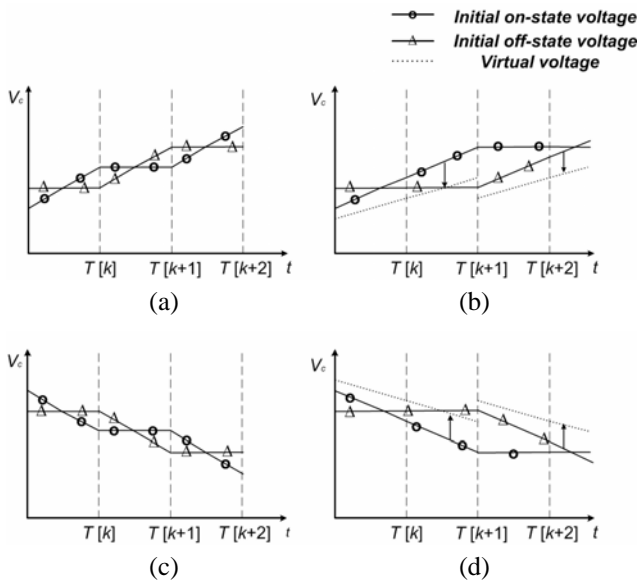
Fig. 4. Diagram of the switching state changes: (a) Positive arm current without virtual voltage; (b) Positive arm current with virtual voltage; (c) Negative arm current without virtual voltage; (d) Negative arm current with virtual voltage.

submodule, the previous gate signal of the submodule can be considered. The first step of the Group Sorting scheme is classification of the groups by the previous state (on-state and off-state) of the submodules at the switching instant. Each group is sorted independently by its submodule capacitor voltages. Also, the $n_{on}(t)$, which is the number of submodules, must be turned on at the current time step (See Fig. 3), and the arm current is then used to determine the individual gate signals at the current time step. As shown in Fig. 5, the number of difference on-state submodules in an arm (*Diff*) at the previous time step (*t-Δt*) and that of the current time step (*t*) is positive, one of the off-group submodules is commanded to be turned on. A submodule with the highest (lowest) voltage value in the off-group is selected to discharge (charge) the submodule when the arm current is flowing negative (positive). When the sign of the *Diff* is negative, one of the on-state group submodules has to be turned off. Depending on the arm current direction, either the highest or lowest submodule is selected. In order to deal with numerous *Diff* in a single time step, the above process is repeated for each *Diff*. This scheme produces equally distributed capacitor voltage and switching commutation, which increases the mechanical reliability of power devices and reduces the power losses for the installed device [23].

Group Sorting focuses on reducing the switching loss. By switching the highest or lowest submodule depending on the current direction at each sampling time, successive on/off switching of the same submodule occurs rarely. Therefore, the switching frequency of the submodule device and switching loss is the lowest compared with the

Fig. 5. The group sorting: (a) Schematic of group sorting [5]; (b) Arrangement and operation of each submodule.

above algorithms. However, the performance of the capacitor voltage can be compromised as detailed in Section 5.

4. Proposed AD-HOC Switching Method for Voltage Balancing

The aforementioned Group Sorting complements the disadvantages of the Full Sorting method and improves the converter efficiency remarkably. As discussed in the previous Section 3.3, by dividing into two groups from the gate signal at previous time step (*t-Δt*) and operating only the submodules in one group depending on *Diff*, all submodules can have one or less than one time state change denoted as *N* during the half period of the output waveform. Since the output waveform is synthesized by

switching in or out submodule capacitor, the output voltage step transition is mostly one submodule capacitor voltage in the steady-state operation. The submodule that maintains each on or off state at the current time step does not participate in the switching until state variation of the total switching number occurs, which may adversely impact on the capacitor voltage balancing. The proposed method is designed to overcome these weaknesses.

The balancing is improved by augmenting the switching of the submodules determined from the Group Sorting. Additional switching is fired by actuating a signal whose frequency is determined according to the external variable as distinct from firing due to N change. The frequency of the actuating signal in this paper is calculated as (14).

(a)

(b)

Fig. 6. Proposed balancing method: (a) Schematic of additional switching method; (b) Arrangement and operation of each submodule.
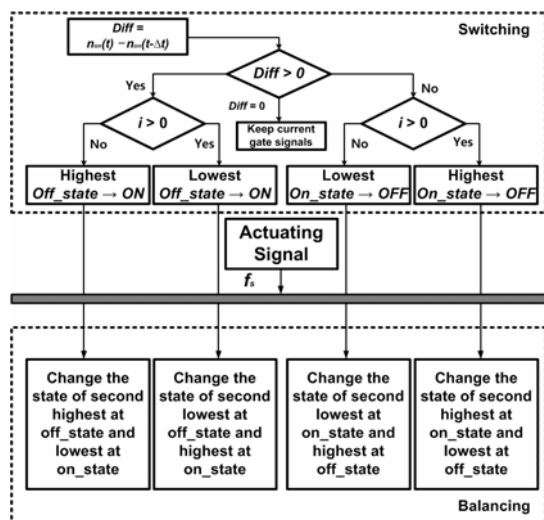
$$f_{as} = 2k \cdot N \cdot f_s \tag{14}$$

where f_{as} is the actuating signal frequency, k is the number of exchange submodules for balancing, N is the number of submodules in an arm and f_s is the system frequency.
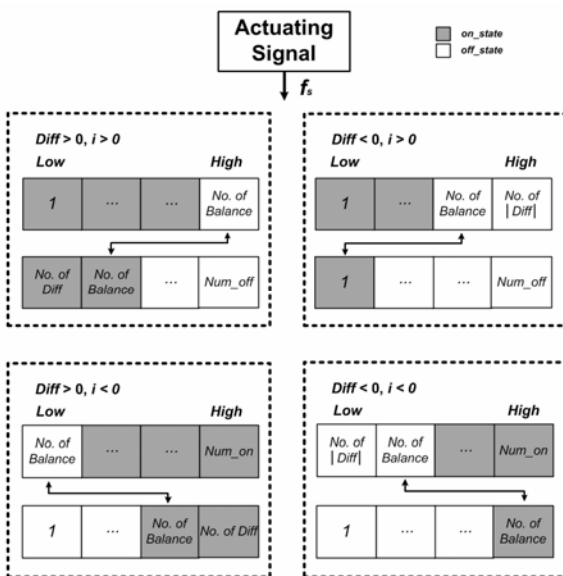
The basic operating strategy is illustrated in Fig. 6 and is described as follows:

• Under positive *Diff* condition, the second lowest (second highest) module in off-state is turned on if the current direction is positive (negative) because the highest (lowest) module is already turned on. Then, in order to synchronize the number of on-state submodules with N change, the highest (lowest) submodule in on-state is turned off.

• Under negative *Diff* condition, the second highest (second lowest) module in on-state is turned on if the current direction is positive (negative) because the highest (lowest) module is already turned on. Then, in order to synchronize the number of off-state submodules with state variation, the lowest (highest) submodule in off-state is turned.

• In all cases, the number of on/off submodule for improving the voltage balance can be flexibly set or adjusted in either direction by an external command as needed.

Compared with the Group Sorting method, the proposed balancing algorithm may remarkably reduce the THD by reducing the voltage ripple. As described in [19], this method brings the desired computational efficiency for high voltage applications and flexibility in providing additional switching signal adaptive to the changing grid condition.

5. Simulation Results

The performance of proposed capacitor voltage balancing method is evaluated for an MMC-HVDC using PSACD/ EMTDC. As depicted in Fig. 7, the HVDC transmission system benchmarked the Trans Bay Cable project [24] designed as a mono-polar structure with DC voltage of ± 200 kV and submodule capacitance of 4.5 mF [25], and number of submodules per arm of 200. The system is designed to transmit 400 MW from MMC 1 to MMC 2. The main circuit parameters are listed in Table 1. The NLM and desired system control functionalities (P control and V_{dc} control, etc.) are commonly implemented in the
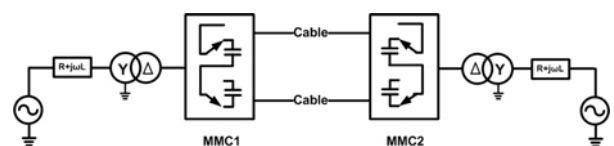

Fig. 7. Schematic diagram of MMC-HVDC system.

Table 1. Main Circuit Parameters of the Simulation System

| Items	Values	Comments
Active power P	400 MW	1.0 pu
AC system voltage at rectifier U_r	230 kV	L-L, rms
AC system voltage at inverter U_i	115 kV	L-L, rms
Short Circuit Ratio (SCR) at the PCC	3.5	
Transformer ratio at rectifier U_r/U_v	230 kV/ 180.5 kV	Y_o / Δ
Transformer ratio at inverter U_i/U_v	115 kV/ 180.5 kV	Y_o / Δ
DC bus voltage $U_{dc}/2$	200 kV	$U_{dc} = \pm200$ kV
Number of submodules per Arm N	200	
submodule capacitance C_o	4.5 mF	
Arm inductance L_o	15 mH	
submodule capacitor voltage U_c	2 kV	
Modulation index k	0.75	
Sampling frequency f_s	10 kHz	
DC cables	88 km	

simulation system. In order to evaluate the performance of the proposed capacitor voltage balancing scheme, the capacitor voltages of 20-submodules among the 200-submodules in the upper arm of phase A are selected and compared with those of three conventional voltage balance methods.

For the convenience of presenting the results, Full Sorting, Advanced Full Sorting, Group Sorting and finally the proposed ad-hoc switching method are referred to be Methods I – IV, respectively in the following.

Figs. 8 and 9 illustrate the capacitor voltage waveforms and corresponding gate signals to the switching submodules. Fig. 8 compares the submodule capacitor voltages of the upper arm in phase-A during 6-cycles of period for four different balancing methods (Full Sorting, Advanced Full Sorting, Group Sorting and proposed Ad-hoc switching method are referred to Method I – IV in this section). Fig. 8(a) shows that the capacitor voltages become perfectly balanced with the Method I: the voltages performance should be the best among four different methods.

However, the switching loss is the highest compared with the others due to the higher average switching frequency. Fig. 8(b) is presented for the result of Method II with a switching frequency of 169 Hz. Fig. 8(b) shows that the capacitor voltages are well balanced, but the capacitor voltage ripple is larger than Method I because the average switching frequency is lower than Method I. Fig. 8(c) is the result employing the Method III. The switching frequency is calculated to be 50 Hz, which is the lowest among four methods. However, the submodule capacitor voltages are not well balanced and the peak-to-peak voltages are remarkable. In comparison with Fig. 8(a), this figure shows that the capacitor voltages become unstable and the magnitude of the capacitor ripple is very large because of the low switching frequency.

Fig. 8(d) illustrates the result of Method IV, similar to Fig. 8(b). This resulted in the same 169 Hz switching frequency as the Method II and the proposed ad-hoc
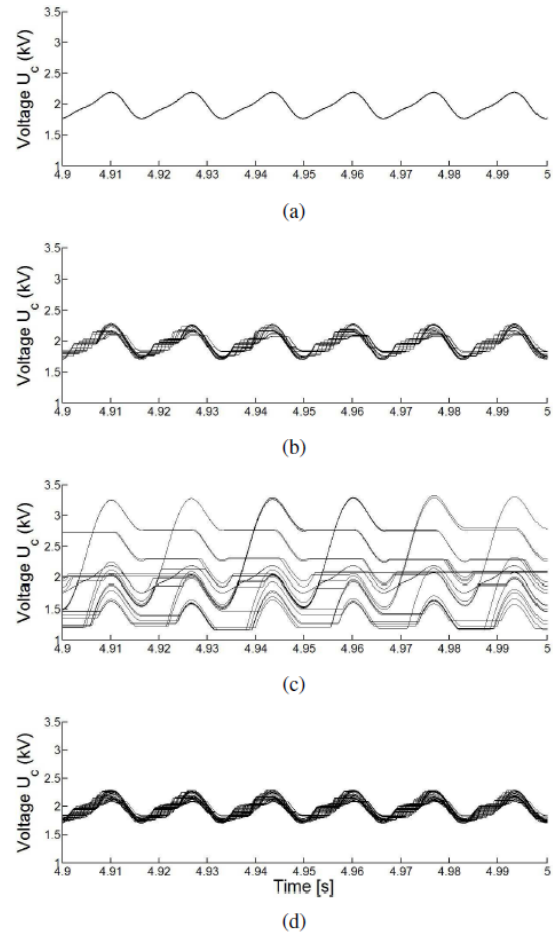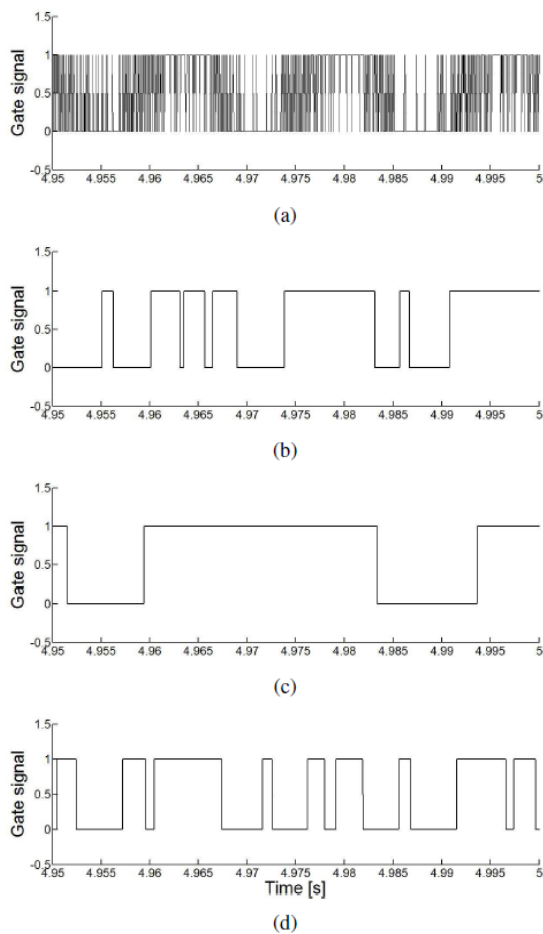

Fig. 8. Comparison of submodule capacitor voltage with each balancing method: (a) Method I; (b) Method II; (c) Method III; (d) Method IV.

Table 2. Characteristic of each Balancing Method

Balancing Method	f_{sw} (HZ)	THD% of v_{ac}	P_{Loss}^{sw} %	P_{Loss}^{cond} %	P_{Loss}^{total} %
Method I	9140	0.25	8.11	0.45	8.56
Method II	169	1.03	0.15	0.45	0.60
Method III	50	1.59	0.04	0.45	0.49
Method IV	169	0.61	0.15	0.45	0.60

switching method successfully balances the capacitor voltages and the peak-to-peak capacitor voltage ripples are compared to Fig. 8(c). Fig. 9(a)-(d) compare the gate signals of one phase on the upper arm submodules under the four different modulation during 3-cycles to illustrate the switching operation or switching frequency mentioned above.

Table 2 summarizes the study results in terms of the switching frequency, THD, switching, conduction and total losses for mentioned voltage balancing methods. The estimated switching and conduction losses are calculated as the percentage of transferred active power based on the datasheet of 5SNA1200G330100 insulated-gate bipolar transistors (IGBTs) [26-28]. For accurate

Fig. 9. Gating signal of one switching device in submodule with each balancing method: (a) Method I; (b) Method II; (c) Method III; (d) Method IV.

comparison, we set the same switching frequency to the proposed ad-hoc switching method (Method IV) and the Advanced Full Sorting (Method II). As presented in Table 2, the same switching frequency leads to the same loss: Compare Methods II and IV. However, the THD of Method II is higher than that of the Method IV because the use of virtual voltage does not allow for uniformly distributed switchings. The Method IV is computationally efficient as mentioned in the previous Section 4.

6. Conclusions

This paper has presented a key design trade-off in designing capacitor voltage balancing schemes for MMC-HVDC: voltage regulation performance vs. converter switching loss. We have presented theoretical basis on these coupled attributes and further investigated the performance of three well-reported submodule capacitor voltage balancing methods (Full Sorting, Advanced Full Sorting and Group Sorting) from the perspective of design trade-off. We have then proposed a new balancing scheme designed for balancing the design trade-off flexibly in

operations as well.

The method allows for additional switching of the submodules adaptive to changing grid condition and reinforces the benefit (minimal loss) of using the Group Sorting while not compromising the voltage regulation performance. We have demonstrated the flexibility and effectiveness of the proposed balancing scheme through simulation studies for a practical system using PSCAD/ EMTDC with reference to the selected conventional schemes. The study presents that the proposed balancing method can significantly reduce the switching loss (as compared with the Full Sorting), THD (as compared with the Advanced Full Sorting and Group Sorting schemes), and submodule capacitor ripple (as compared with the Group Sorting). The flexibility built upon the high efficiency of the proposed method should help relieve the aforementioned design concerns and maximize the performance of the MMC-HVDC.

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