JPE 16-3-11

http://dx.doi.org/10.6113/JPE.2016.16.3.925
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A New Interleaved Double-Input Three-Level Boost Converter

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Abstract

This paper proposes a new interleaved double-input three-level Boost (DITLB) converter, which is composed of two boost converters indirectly in series. Thus, a high voltage gain, together with a low component stress and a small input current ripple due to the interleaved control scheme, is achieved. The operating principle of the DITLB converter under the individual supplying power (ISP) and simultaneous supplying power (SSP) mode is analyzed. In addition, closed-loop control strategies composed of a voltage-current loop and a voltage-balance loop, have been researched to make the converter operate steadily and to alleviate the neutral-point imbalance issue. Experimental results verify correctness and feasibility of the proposed topology and control strategies.

Key words: Boost, Double-input, Interleaved scheme, Three-level, Voltage-balance

I. INTRODUCTION

In a renewable power generation system with many different input sources, many individual dc-dc converters together with independent control schemes are necessary, which are both complex and increase the cost of the system. Integrating different input sources with distinct electrical characteristics into a common system while still achieving a high efficiency and good performance is an important topic. To attain the goal of integration, a multi-input converter (MIC) is a perfect choice, which may integrate diverse power sources and provide power to a common load in a single conversion stage [1].

Many papers related to a variety of MIC topologies have been published. In [2], a systematic approach to synthesizing MICs by introducing pulsating voltage source cells and pulsating current source cells into six basic PWM converters is proposed. Four rules that must be observed in order to realize a MIC from its single-input version are listed in [3]. In renewable power generation systems, MIC topologies are usually integrated with a dc link. However, most of these MICs do not take the high voltage gain into consideration, since the outputs of photovoltaic cells, fuel cells and battery cells are typically unregulated low-level dc voltages that need to be stepped up to regulated, high-level voltages for practical applications.

At present, the conventional Boost converter is usually used because of its simple circuit. Unfortunately, practical considerations limit its output voltage to about four times its input voltage [4]. To increase the voltage gain and achieve other performances, many high step-up converter topologies have been proposed. A high step-up active-clamp converter composed of an input current doubler and a symmetrical switched-capacitor circuit is proposed in [5]. Although a high voltage gain is achieved, many switches are needed. Several high set-up converter topologies that use coupled inductors have been proposed for the fuel cell generation systems [6], [7]. Although a high voltage gain is obtained, their efficiencies are degraded due to the losses associated with leakage inductances. In addition, coupled inductors may introduce high switch voltage stress and EMI problems.

Recently, some step-up dc–dc converters have been studied. However, but they are limited to single-input-single-output systems [8]-[10]. The system structure of a conventional three-level Boost converter (CTLB) combined with a three-level diode-clamped inverter has been proposed to achieve a high medium voltage and a high power. In addition, a small input current ripple and a neutral-point voltage control can be achieved [11]-[13]. However, the step-up capacity of the systems is limited due to the CTLB converter, which is only 1/(1-D). A novel hybrid three-level Boost

Manuscript received Nov. 9, 2015; accepted Jan. 26, 2016
Recommended for publication by Associate Editor Chun-An Cheng.
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(HTLB) converter had been proposed to achieve a high voltage gain at the expense of increasing the number of components and the addition of a complex modulation strategy [14]. [15], [16] propose a series of multilevel boost converters based on switched-capacitor networks, which have high voltage gains and a self-balance function for capacitor voltages. In addition, the self-balance function is highly advantageous for balancing the dc link capacitor voltages of diode-clamped multilevel inverters [17], [18]. However, since no interleaved scheme is adopted, the input current ripple and the current stress of a single switch are both very large, which are great disadvantages for FC and BC systems. [19] proposes a three-level Boost converter with a flying-capacitor (FCTLB) and [20] transforms this converter into a multi-input converter. Although a high voltage gain and small ripples are achieved, the voltage stresses across the output diode are high. In addition, two double-input converters operating in the ISP mode and in the SSP mode are proposed with a high voltage gain and small component stresses [21]. However, it is difficult to integrate the two converters, and many capacitors are necessary.

On the whole, multi-input step-up converters are essential for integrating different energy sources with low voltage levels. The development of multi-input step-up converter topologies goes through three stages, as shown in Fig.1. In Fig. 1(a), a MIC structure is constructed by placing several step-up converters in parallel with all of the output terminals. However, the output voltage gain is limited due to its parallel structure. Then, the MIC structure shown in Fig. 1(b) is proposed by placing the output terminals in series. However, the input terminals and output terminals usually do not share the same ground, which may introduce an electro-magnetic interference (EMI) problem and increase the quantity of isolated power drivers. Therefore, the MIC structure shown in Fig. 1(c) should be the best choice to alleviate the above mentioned problems. This structure has a high voltage gain since the output terminals are directly or indirectly connected in series. In addition, the input terminals and output terminals have a common ground, which helps reduce EMI and cost of driver circuits. Additionally, an interleaved control scheme can be easily adopted to decrease the input current ripple.

In this paper, a new DITLB converter is proposed that can operate under the individual supplying power (ISP) mode and the simultaneous supplying power (SSP) mode. A small input current ripple, low current stresses and low voltage stresses across all of the power devices are achieved. Additionally, the self-balance function for capacitor voltages is included. This paper is organized as follows: Section II introduces the operation principle of the proposed converter. A performance analysis is subsequently presented in Section III. A closed-loop control strategy for the proposed DITLB converter under different operating modes has been presented in Section IV, and experimental verification is presented in Section V. Finally, some conclusion have been drawn in Section VI.

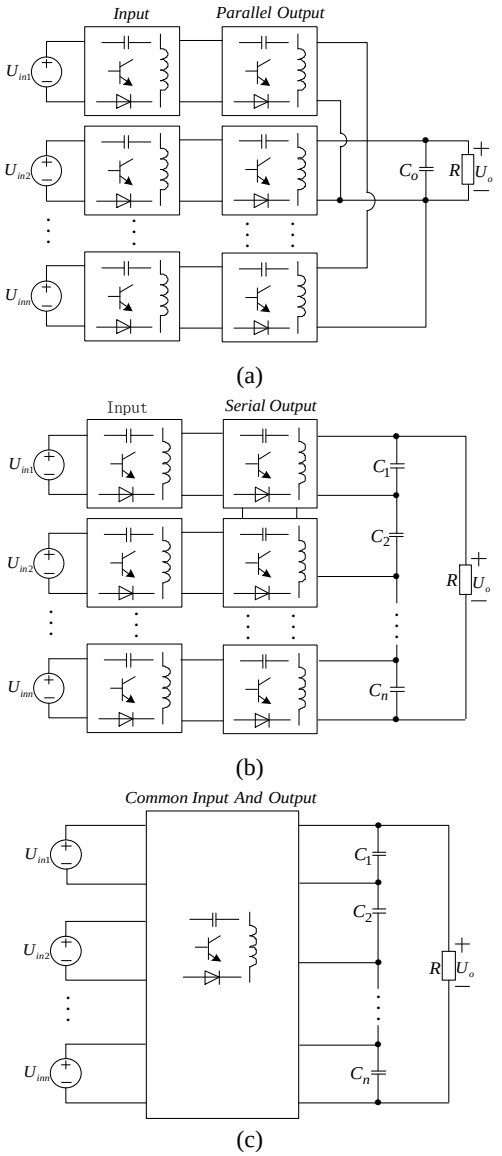


Fig. 1. The development of multi-input step-up converters.

II. THE PROPOSED DITLB CONVERTER

The proposed DITLB converter is presented in Fig. 2. To analyze the converter, the converter is divided into three cells: cell 1, cell 2, and cell 3. Cell 1 (including L_1, S_1, D_1, and C_1) and cell 2 (including L_2, S_2, D_3, and C_2) are Boost converters. Cell 3 is composed of C_3 and D_2, and connects the two Boost converters in series. Therefore, the operating principle of the DITLB under the continuous conduction mode (CCM) is different from that of two Boost converters directly in series. The proposed converter is controlled by the interleaved operation scheme of S_1 and S_2, where the two carrier signals C_{a1} and C_{a2} have a phase shift of 180 degrees. To simplify the analysis process, some assumptions are made as follows:

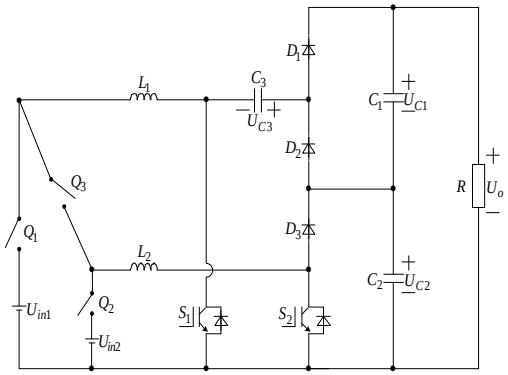


Fig. 2. The proposed DITLB converter.

1) The inductor currents i_{L1} and i_{L2} and the input current i_{in} are continuous, and their average values are labelled as I_{L1}, I_{L2}, and I_{in}.

2) u_{L1} and u_{L2} represent the voltages across L_1 and L_2, and U_{C1}, U_{C2}, and U_{C3} represent the capacitor voltages of C_1, C_2, and C_3.

3) All of the components are ideal without considering any parasitic parameters.

According to the definition of a MIC, the proposed converter works under both the ISP mode and the SSP mode. In Fig. 2, the turn-on and turn-off of Q_1, Q_2, and Q_3 determine the operating mode. When Q_1, and Q_3 are turned on while Q_2 is turned off, the DITLB converter operates under the ISP mode with input source 1 supplying power. In addition, when Q_2 and Q_3 are turned on while Q_1 is turned off, the DITLB converter operates under the ISP mode with input source 2 supplying power. However, when Q_1 and Q_2 are turned on while Q_3 is turned off, the DITLB converter operates under the SSP mode with the two input sources supplying power simultaneously.

A. Operating Principle under ISP Mode

Under the ISP mode, the two switches S_1 and S_2 in the DITLB converter are controlled by an interleaved operation scheme with the same duty cycle D. Since the converter operates under the same operating principle regardless of which input source is used, the ISP mode with input source 1 is taken as an example for the theoretical analysis. Equivalent circuits of the converter under this mode are shown in Fig.3 and typical waveforms are given in Fig.4. The basic operating principle is presented as follows.

Stage I: during this period, L_1 and L_2 are both charged by U_{in1}. The conduction of S_1 and D_2 provides a pathway for C_2 and C_3 to be connected in parallel. Thus, the following expressions can be achieved:

$$u_{L1} = U_{in1} \tag{1}$$

$$u_{L2} = U_{in1} \tag{2}$$

$$U_{C2} = U_{C3} \tag{3}$$

Stage II: during this period, L_1 is still charged by U_{in1}.

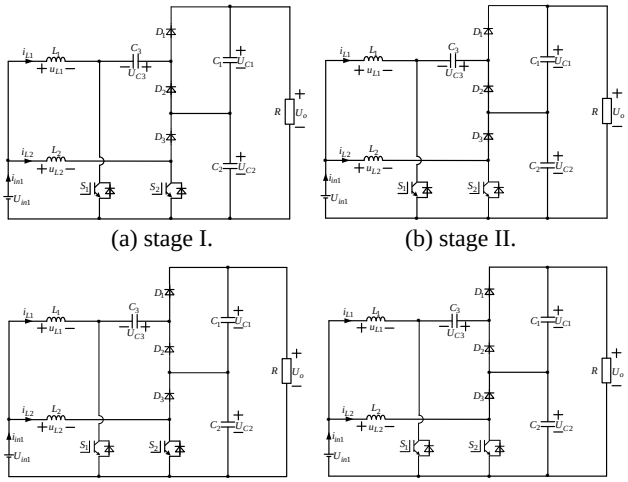


Fig. 3. Equivalent circuits of the DITLB converter under ISP mode with input source 1 supplying power:

Additionally, C_2 is still in parallel with C_3, which is charged by L_2 and U_{in1}. Thus, the voltage across L_2 is changed by:

$$u_{L2} = U_{in1} - U_{C2} \tag{4}$$

Stage III: during this period, L_2 is charged by U_{in1} and the same formula (2) can be obtained. However, the voltage across L_1 is described by:

$$U_{C3} - u_{L1} + U_{in1} = U_{C1} + U_{C2} \tag{5}$$

(5) can be simplified by combining (3):

$$u_{L1} = U_{in1} - U_{C1} \tag{6}$$

Stage IV: during this period, the voltage across L_1 is the same as (6). In addition, C_3 is charged by L_2 and U_{in1}. Thus, the voltage across L_2 is the same as (4).

In all four stages, the output voltage of the converter is the sum of U_{C1} and U_{C2}. Since the two Boost converters are indirectly in series, i.e.:

$$U_o = U_{C1} + U_{C2} \tag{7}$$

According to the interleaved operation scheme, the converter can operate under two conditions: D>0.5 and D<0.5. When the duty cycle D is bigger than 0.5, it operates at the periodic stages of I, II, I, and III. Accoding to (1)-(5) and (7), voltage gain and capacitor voltages can be achieved:

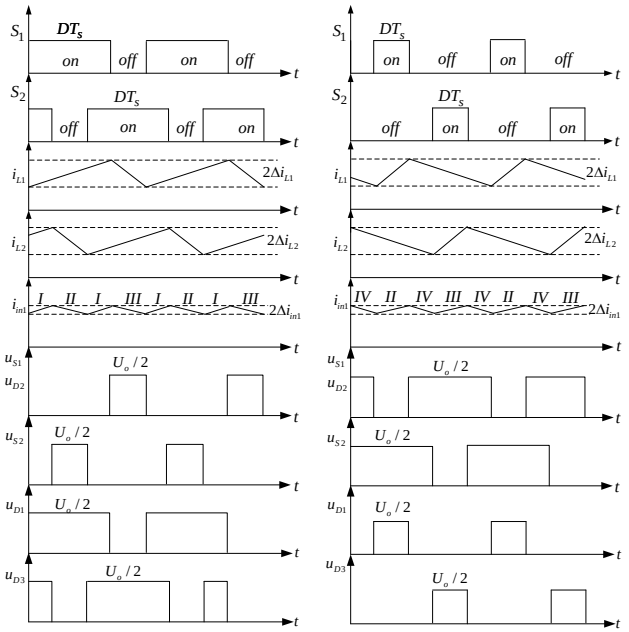
$$G = \frac{U_o}{U_{in1}} = \frac{2}{1-D} \tag{8}$$

$$U_{C1} = U_{C2} = U_{C3} = \frac{1}{1-D} U_{in1} \tag{9}$$

It can be seen from (9) that the three capacitor voltages are equal. It should be noted that U_{C2} and U_{C3} are self-balanced due to the switched-capacitor network, while U_{C1} and U_{C2} are balanced since they have the same duty cycle D. On the whole, it is called self-voltage-balance function.

Additionally, the current ripples of L_1 and L_2 shown in Fig. 4, can be obtained as follows:

$$\Delta i_{L1} = \Delta i_{L2} = \frac{U_{in1}}{2L_1} D T_s = \frac{U_{in1}}{2L_1} \frac{D}{f_s} \tag{10}$$



(a) D>0.5. (b) D<0.5.

Fig. 4. Typical waveforms.

At the same time, it is easy to obtain the input current ripple:

$$\Delta i_{in1} = \frac{U_{in1}}{2L_1}(2D-1)\frac{T_s}{2} = \frac{U_{in1}}{2L_1}\frac{2D-1}{2f_s} \tag{11}$$

When the duty cycle D is smaller than 0.5, the proposed converter operates at the periodic stages of IV, II, IV, and III; and the same results shown in (8)-(10) can be achieved. Under this operating state, the input current ripple is changed by:

$$\Delta i_{in1} = \frac{U_{in}}{2L_1}\frac{D(1-2D)}{2(1-D)f_s} \tag{12}$$

Regardless of the duty cycle D, stages II and III have the same operating time. At stage II, the capacitor C_3 is charged by U_{in1} and L_2 with the current I_{L2}. Meanwhile, at stage III, C_3 discharges energy to the load with the current I_{L1}. According to the Ampere-Second Balance Principle for C_3, it is not difficult to conclude that I_{L1} is equal to I_{L2}. This is called self-current-balance function. Then, based on the Power Conservation Principle, there is:

$$I_{L1}U_{in1} = I_{L2}U_{in1} = \frac{1}{2}I_{in}U_{in1} = \frac{U_o^2}{2R} \tag{13}$$

(13) can be simplified by combining (8):

$$I_{L1} = I_{L2} = \frac{1}{2}I_{in1} = \frac{U_o}{(1-D)R} \tag{14}$$

It should be note that similar results can be achieved when the converter operates under the ISP mode with input source 2.

It is well known that the discontinuous conduction mode (DCM) occurs when the inductor current ripple becomes greater than the average inductor current. Since cell 1 and cell 2 have the same inductance, the inductor L_2 is taken as an example:

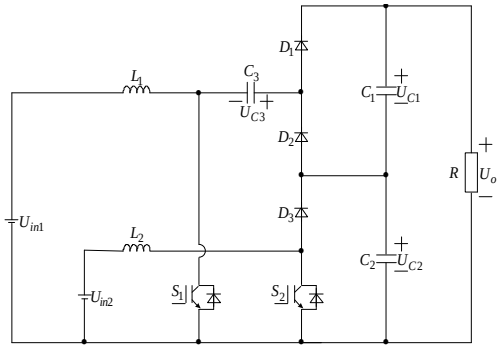


Fig. 5. The DITLB converter operates under SSP mode.

$$\Delta i_{L2} > I_{L2} \tag{15}$$

The integration of (8), (10) and (14) into (15) yields the following condition for the DCM mode:

$$K < K_{crit}(\mathrm{D}) \tag{16}$$

Where K is equal to $2Lf_s/R$, and K_{crit}(D) is the critical value of K at the boundary between the CCM and DCM modes:

$$K_{\mathrm{crit}}(D) = \frac{D(1\text{-}D)^2}{2} \tag{17}$$

The maximum value of K_{crit}(D) can be easily achieved at D = 1/3.

$$K_{\mathrm{crit}}(D)_{\max} = \frac{2}{27} \tag{18}$$

If K is greater than 2/27, the converter operates under the CCM mode for all values of D. If K is smaller than 2/27, the converter operates under the DCM mode for some intermediate range values of D near D=1/3. Thus, the minimum inductance $L_{\min}$ should be:

$$\frac{2L_{\min}f_s}{R} = \frac{2}{27} \tag{19}$$

(19) is simplified to achieve $L_{\min}$ as follows:

$$L_{\min} = \frac{R}{27f_s} \tag{20}$$

B. Operating Principle under SSP Mode

When Q_1 and Q_2 turn on while Q_3 turns off, the proposed DITLB converter operating under the SSP mode is shown in Fig. 5. Under this mode, cell 1 and cell 2 operate independently, i.e. cell 1 does not affect cell 2. In addition, the two cells are controlled by two independent closed-loop control strategies. It should be noted that the converter does not need to operate with an interleaved operation scheme, since the two input sources feed the load simultaneously. Thus, it is not difficult to obtain the output voltage and capacitor voltages as follows:

$$U_o = \frac{1}{1-D_1}U_{in1} + \frac{1}{1-D_2}U_{in2} \tag{21}$$

$$U_{C1}=\frac{1}{1-D_1}U_{in1} \tag{22}$$

$$U_{C2}=U_{C3}=\frac{1}{1-D_2}U_{in2} \tag{23}$$

The two average inductor currents can be described by:

$$I_{L1}=\frac{U_o}{(1-D_1)R} \tag{24}$$

$$I_{L2}=\frac{U_o}{(1-D_2)R} \tag{25}$$

III. Closed-loop Control Strategy

As analyzed in section II, the proposed DITLB converter under the ISP mode has a voltage-balance function for the capacitor voltages. However, like three-level Boost converters, the converter also has a neutral-point balancing problem due to the interleaved operation scheme. In addition, the IGBTs and power diodes usually have some voltage drops, which should be considered in practical circuit design. If U_d is assumed to be the voltage drops, two voltage-second equations can be rewritten by:

$$DT_s(U_{in}-U_d)+(1-D)T_s(U_{in}-U_{C1}-3U_d)=0 \tag{26}$$

$$DT_s(U_{in}-U_d)+(1-D)T_s(U_{in}-U_{C2}-U_d)=0 \tag{27}$$

Then, the output voltage and capacitor voltages can be achieved based on (26) and (27):

$$U_o=\frac{2}{1-D}U_{in}-\frac{4-2D}{1-D}U_d \tag{28}$$

$$U_{C1}=U_{C3}=\frac{1}{1-D}U_{in}-\frac{3-2D}{1-D}U_d \tag{29}$$

$$U_{C2}=\frac{1}{1-D}U_{in}-\frac{1}{1-D}U_d \tag{30}$$

The voltage difference between C_1 and C_2 can be obtained based on (29) and (30)

$$U_{C2}-U_{C1}=2U_d \tag{31}$$

It can be seen from (31) that there is a voltage difference $2U_d$ between C_1 and C_2 due to the voltage drops. Although it is small, the voltage drops may result in a neutral-point balancing problem.

A Closed-loop Control under ISP Mode

To alleviate the neutral-point problem of the proposed converter under the ISP mode, a voltage-current loop together with a simple voltage-balance loop is presented in Fig. 6.

As analyzed in section II, cell 1 and cell 2 represent two Boost converters, whose output terminals are connected in series. In addition, the two Boost converters are controlled by an interleaved scheme with the same duty cycle *D*. Thus, the same average inductor current and output capacitor voltage can be achieved. By only controlling one of the Boost converters, the input current and output voltage of the converter can be easily controlled to be stable. In Fig. 6, cell 2 is taken as the target to be controlled by voltage-current loop 2. By controlling the capacitor voltage U_{C2} and the inductor current I_{L2}, it is easy to get the duty cycle d_2 of S_2.

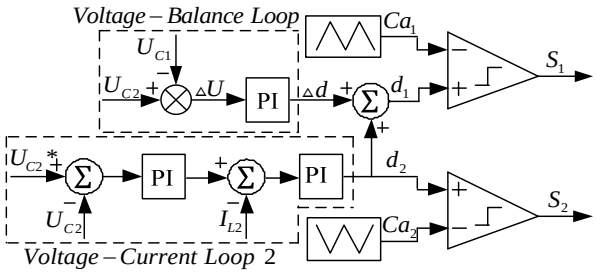


Fig. 6. Closed-loop control strategy under ISP mode.

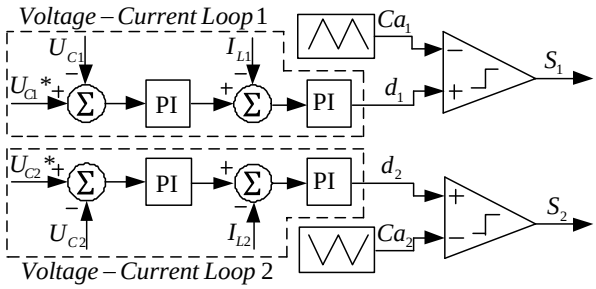


Fig. 7. Closed-loop control strategy under SSP mode.

The voltage-balance loop aims at reducing the voltage difference between C_1 and C_2. In the voltage-balance loop, the difference duty cycle $\triangle d$ is achieved through a simple PI controller by the difference voltage $\triangle U$. Then, the duty cycle d_1 of the switch S_1 can be easily obtained by:

$$d_1=d_2+\triangle d \tag{32}$$

From (32), the voltage-balance process is: when U_{C2} is bigger than U_{C1}, $\triangle d$ becomes positive, which makes d_1 a little bigger than d_2. Then, U_{C1} increases to follow U_{C2}, and is finally equal to U_{C2} after several switching periods. It should be noted that $\triangle d$ is very small, since the voltage difference is very small. Thus, voltage-current loop 2 cannot be greatly affected.

B Closed-loop Control under SSP Mode

Under the SSP mode, the two Boost converters are controlled independently by voltage-current loop 1 and voltage-current loop 2, as shown in Fig. 7. The capacitor voltages are controlled to be equal by setting the same referring voltage for the two Boost converters, i.e. U_{C1}* is equal to U_{C2}*. Thus, there is no need to use a voltage-balance loop under this mode.

IV. Performance Analysis

A. Comparative Analysis

For both the ISP and SSP modes, the voltage stresses across the two switches are equal and the voltage stresses across all of the diodes are also equal. They are given as follows:

TABLE I
COMPARATIVE ANALYSIS AMONG CTLB, HTLB, FCTLB, SCTLB CONVERTERS AND PROPOSED TLB CONVERTER

Topology	L	S	D	C	G	U_{VPS}	U_{VPD}	U_{VPC}	I_{VPS}	Interleaved Scheme	Voltage Balance	Current Balance	Common Ground
CTLB	2	2	2	2	1/(1-D)	$0.5U_o$	$0.5U_o$	$0.5U_o$	DI_{in}	Yes	No	No	No
HTLB	1	4	8	2	$1/(m_b-m_a)$	$0.5U_o$	$0.5U_o$	$0.5U_o$	I_{in}	Yes	Yes	No	No
FCTLB	2	2	2	2	2/(1-D)	$0.5U_o$	U_o	U_o	DI_{in}	Yes	No	Yes	Yes
SCTLB	1	1	3	3	2/(1-D)	$0.5U_o$	$0.5U_o$	$0.5U_o$	$0.5DI_{in}$	No	Yes	No	Yes
Proposed TLB	2	2	3	3	2/(1-D)	$0.5U_o$	$0.5U_o$	$0.5U_o$	$0.5DI_{in}$	Yes	Yes	Yes	Yes

$$U_{VPS} = U_{VPD} = \frac{1}{2}U_o \tag{33}$$

U_{VPS} and U_{VPD} represent the voltage stresses across the switches and diodes, respectively.

Under the ISP mode, the average current stress across all of the diodes and two switches are equal, shown in (34) and (35):

$$I_{VPD} = I_o \tag{34}$$

$$I_{VPS} = \frac{D}{2}I_{ink} \quad (k = 1, 2) \tag{35}$$

I_{VPS} and I_{VPD} represents the current stresses across switches and diodes, respectively.

As given in Section I, the CTLB, HTLB, FCTLB, and SCTLB converters are conventional three-level Boost, hybrid three-level Boost, three-level Boost with a flying-capacitor, and three-level Boost with a switched-capacitor network, respectively. It should be noted that the SCTLB converter is one version of the multilevel Boost converters in [15-18]. Table I shows comparative results among the CTLB, HTLB, FCTLB, SCTLB, and the proposed TLB converters.

In the four three-level Boost converters, the HTLB has the highest voltage gain when the modulation indexes m_a and m_b are set well. However, so many components are necessary and the modulation strategy is complex. The SCTLB has a high voltage gain and a self-voltage-balance function with its input and output sharing a common ground. However, the input current and current stress across only one switch is very large, since it cannot use an interleaved scheme. Although interleaved schemes are adopted, the CTLB has no self-voltage-balance or current-balance functions. More importantly, its input and output do not share the same ground and its voltage gain is limited to 1/(1-D). Compared with CTLB, HTLB, SCTLB converters, the converter FCTLB presents relatively good performances. However, the output diode and output capacitor have very high voltage stresses, which are equal to the output voltage. Furthermore, since the output capacitor of the FCTLB is not composed of two split capacitors and is independent from its input, it cannot achieve the self-voltage-balance function or the voltage-balance control. However, all of these issues in the CTLB, HTLB, FCTLB and SCTLB, can be mostly avoided in the proposed TLB. Firstly, small voltage stresses for all of the components are achieved because cell 1 and cell 2 are in series. Secondly, small current stresses for these components are also achieved due to the interleaved operation scheme. Moreover, the self-voltage-balance function and the self-current-balance function help make cell 1 and cell 2 have the same performances. Lastly, the input source and output terminal share a common ground. Thus, the driver circuit of S_1 and S_2 can share the same power supply, reducing the design cost of the drive circuits. On the whole, the proposed TLB is the best converter.

B. The Key Function of Cell 3

As analyzed in Section II, cell 1 and cell 2 in the proposed converter, are two Boost converters, which share the same input source with the outputs in series. This is similar to an input-serial-output-parallel (IPOS) dc/dc system, which is usually composed of isolated dc/dc converters. However, unlike an IPOS dc/dc system, the proposed converter is composed of non-isolated dc/dc converters owing to cell 3. Because of cell 3 and S_1, C_2 constructs a switched-capacitor network that has the self-voltage-balance function. Therefore, the two capacitor voltages of C_2 and C_3 are easy to self-balanced when S_1 is turned on, as shown in Fig. 3(a) and Fig. 3(b). In addition, this voltage-balance mechanism has been reported in [15]-[18]. Thus, a high voltage gain and a small input current ripple can be easily achieved. The voltage-balance mechanism for a converter under the ISP mode with U_{in1} is: the energy of C_3 comes from L_1 and U_{in1}, and the energy of C_2 comes from L_2 and U_{in1}. Cell 1 and cell 2 can easily output the same capacitor voltage, since they are controlled by an interleaved scheme with the same duty cycle. Furthermore, the voltages of C_3 and C_2 are self-balanced due to the switched-capacitor network. Therefore, the voltages of C_1, C_2, and C_3 are equal.

The voltage-balance mechanism for the converter under the ISP mode with U_{in2} is the same as the above mentioned mechanism. On the whole, it is the key function of cell 3 that makes the proposed converter have a high voltage gain and the other good performances mentioned above.

C. Extension

Multi-input converters with more input sources and more output levels can be extended from the proposed DITLB converter. Fig. 8 shows the topology of an extended three-input four-level Boost converter, where there are three

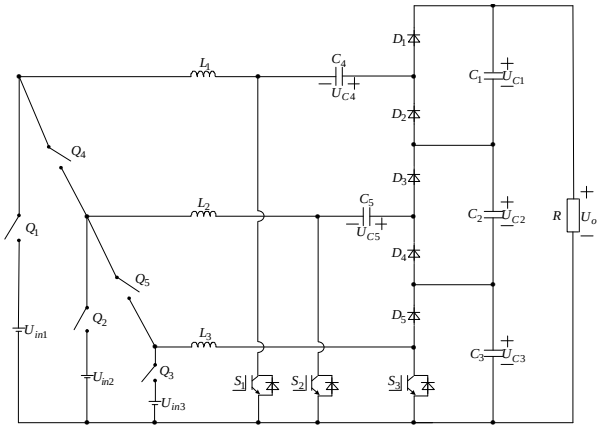


Fig. 8. The three-input four-level Boost converter.

Boost converters: U_{in1}, S_1, L_1, D_1, C_1; U_{in2}, S_2, L_2, D_3, C_2; and U_{in3}, S_3, L_3, D_5, C_3.

A small input current and little current stress across every switch can be achieved. In addition, small voltage stresses $1/3U_o$ across all of the components besides C_4, can be achieved. In the extended converter, besides the switched-capacitor network, is composed of S_2 and C_5. D_4 and C_3, are the components S_1 and C_4. D_2, C_2, and C_3 form another switched-capacitor network. Thus, the voltage stress across C_4 is $2/3U_o$, which is the sum of U_{C2} and U_{C3}.

When Q_1, Q_2, and Q_3 are turned on and Q_4 and Q_5 are turned off, the converter operates under the SSP mode with all three input sources supplying power simultaneously. The output voltage under this mode can be given as follows:

$$U_o = \frac{1}{1-D}(U_{in1} + U_{in2} + U_{in3}) \tag{36}$$

In addition, the converter can also operate under the ISP mode with any two input sources. For instance, when Q_2, Q_3, and Q_4 are turned on and Q_1 and Q_5 are turned off, the input sources U_{in2} and U_{in3} feed the load simultaneously. Under this mode, the output voltage is:

$$U_o = \frac{1}{1-D}(2U_{in2} + U_{in3}) \tag{37}$$

Under the ISP mode with only one input source supplying power, all three of the switches can be controlled by three interleaved drive signals, which are phase shifted 120 degrees. For example, when Q_3 is turned on and Q_1, Q_2, Q_4, and Q_5 are turned off, the converter operates under the ISP mode with the input source U_{in3}. In addition, the output voltage under this mode can be descripted by:

$$U_o = \frac{3}{1-D}U_{in3} \tag{38}$$

As shown in Fig. 2 and Fig. 8, the proposed DITLB converter and the extended converter are a good choice to connect with Neutral-Point-Clamped (NPC) multilevel inverters to achieve a medium voltage and a high power. With this configuration, the capacitor voltages of the dc link can be controlled with the voltage-balance control strategy in multi-input dc/dc converters, which gives control flexibility to the NPC multilevel inverters to effectively track the grid current references. It is greatly different from the voltage-balance control strategies used in multilevel inverters to solve the neutral point imbalance issue.

TABLE II
EXPERIMENTAL PARAMETERS

Components	Rated Values
Output power P_o	320W
Input sources U_{in1}, U_{in2}	48V-80V
Switching frequency f_s	25kHz
Referenced capacitor voltage U_{C2}^*, U_{C3}^*	200V
Inductors L_1, L_2	780uH
Capacitors C_1, C_2, C_3	470uF/400V
IGBTs S_1, S_2	G80N60
Diodes D_1, D_2, D_3	DSEP30-06B

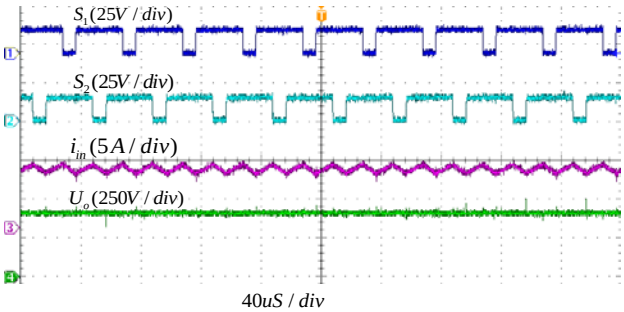
V. EXPERIMENTAL VERIFICATION

To verify the correctness and feasibility of the proposed DITLB converter, a small power prototype based on Dspace1006 has been built with the experimental parameters given in Table II. In addition, the drive circuits are designed based on a photocoupler HCPL-3120. For the sake of simplicity, the two input voltages are set to have the same voltage range 48V-80V. To get the output voltage 400V, the referenced capacitor voltages U_{C2}* and U_{C3}* are both set to 200V. Both steady state and dynamic experimental results have been given. In addition, an efficiency analysis for the proposed DITLB converter under both the ISP and SSP modes is presented.

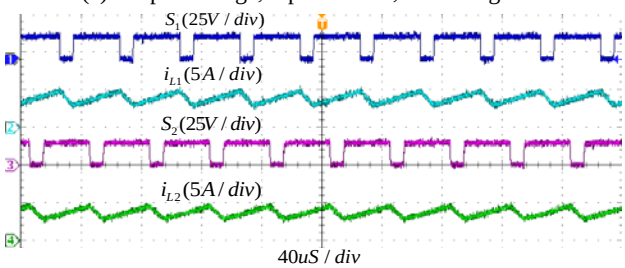
A. Steady State Experiments

According to the analysis in Section III, the converter under the ISP mode with different input sources operate at the same main circuit. Thus, experimental results of the converter, when U_{in1} with 48V supplies energy to the load independently, are given in Fig. 9. In addition, experimental results, when U_{in2} with 80V feeds the load independently, are presented in Fig. 10.

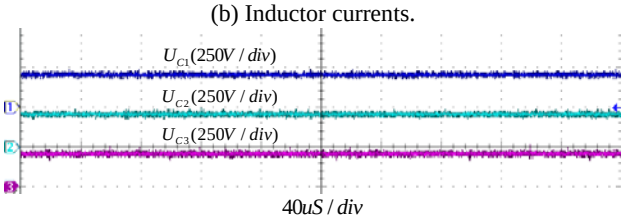
As can be seen from Fig. 9 and Fig. 10, the output voltage is stable with 400V no matter which input source is used. The duty cycles of S_1 and S_2 decrease when the input voltage changes from 48V to 80V. The inductor current ripple and input current ripples are given to compare with their theoretical values, as shown in Table III. The theoretical values are calculated based on (10), (11) and the tested duty cycle D. In TABLE III, Δi_L^* means the theoretical value of the two same inductor current ripples, and Δi_{in1}^* means the theoretical value of the input current ripple. The experimental values are in good agreement with theoretical values. In addition, the input current ripple is small due to the interleaved scheme. More importantly, the ripple frequency of



(a) Output voltage, input current, driven signals.

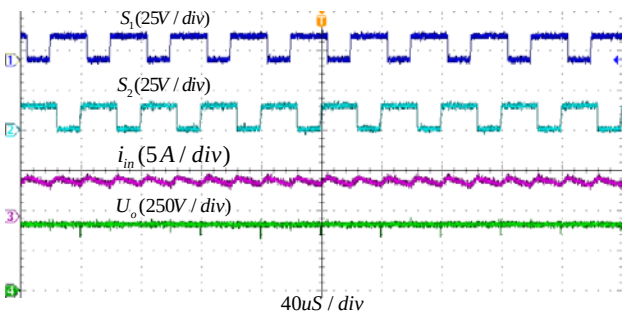


(b) Inductor currents.

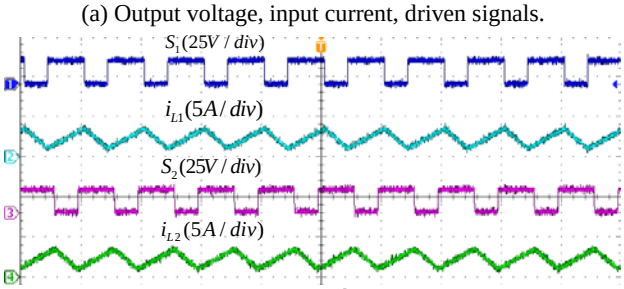


(c) Capacitor voltages.

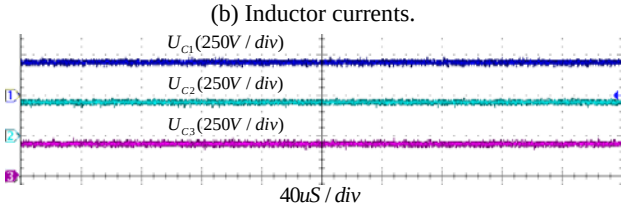
Fig. 9. Under ISP mode with U_{in1} 48V.



(a) Output voltage, input current, driven signals.



(b) Inductor currents.



(c) Capacitor voltages.

Fig.10. Under ISP mode with U_{in2} 80V.

TABLE III
COMPARATIVE ANALYSIS

Input	D	Δi_L^*	Δi_{in1}^*	Δi_L	Δi_{in1}
48V	0.785	0.97A	0.35A	1.00A	0.50A
80V	0.625	1.28A	0.26A	1.35A	0.35A

the input current 50kHz is two times the switching frequency 25kHz, which helps design an input filter with a smaller size.

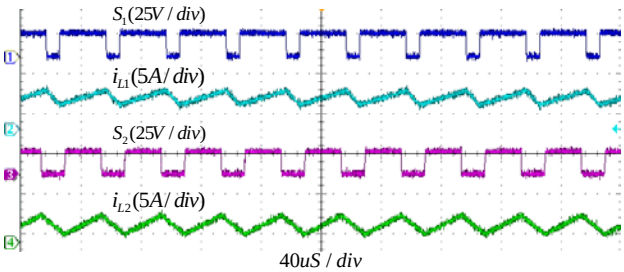
Under the SSP mode, key experimental waveforms with different input voltages are presented in Fig. 11 and Fig. 12. With two different input voltages, the converter can still operate with a stable output voltage 400V. In addition, the capacitor voltages are all 200V, which is half of the output voltage. According to (24) and (25), the theoretical values for I_{L1} and I_{L2} when U_{in1} is 48V and U_{in2} is 80V, are 3.33A and 2.00A, respectively. In addition, in the experiment test, I_{L1} is 3.68A and I_{L2} is 2.10A, which basically agrees with the theoretical values. Furthermore, when U_{in1} is 80V and U_{in2} is 48V, I_{L1} is 2.12A and I_{L2} is 3.66A, which also agrees with the theoretical values of 2.10A and 3.68A.

Terminal voltage waveforms of S_1, S_2, D_1, D_2, and D_3 under the ISP mode when U_{in1} is 48V are taken as an example to be presented in Fig. 13. It should be noted that u_{S1} and u_{S2} are defined to describe the voltage difference between the collector terminal and the emitter terminal of the IGBTs S_1 and S_2. In addition, u_{D1}, u_{D2}, and u_{D3} are given to define the voltage difference between the cathode and the anode of the power diodes D_1, D_2, and D_3. It is clear from Fig. 13 that the top voltages of all of the switches and diodes in the converter are 200V, which is half of the output voltage 400V. In addition, it is not difficult to know that the conduction and shutdown of D_1 is complementary to that of D_2, and that the conduction and shutdown of D_1 has a phase shift of 180 degrees with D_3. Furthermore, the conduction and shutdown of S_1 also has a phase shift of 180 degrees with S_2. All these results verify correctness and feasibility of the proposed converter.

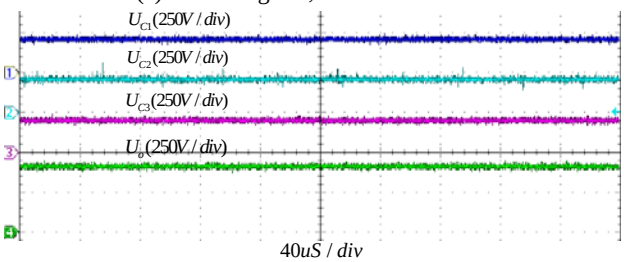
B. Dynamic Experiments

Dynamic researches on the proposed DITLB converter have also been carried out. Dynamic experimental waveforms of the DITLB under the ISP mode with different jump conditions are presented in Fig. 14. Dynamic results of the DITLB under the SSP mode when U_{in1} jumps from 48V to 70V and U_{in2} jumps from 48V to 80V simultaneously, are presented in Fig. 15.

As shown in Fig. 14(a), when U_{in1} with 48V jumps to U_{in2} with 80V, I_{L2} drops from 3.68A to 2.10A and I_{in} drops from 7.40A to 4.24A. In addition, U_o increases and then drops to be stable with 400V. In Fig. 14(b), when U_{in1} with 80V jumps to U_{in2} with 48V, I_{L2} increases from 2.12A to 3.66 and I_{in} increases from 4.21A to 7.39A. In addition, U_o drops a little and then increases to be stable with 400V. The dynamic process in Fig. 14 is quick with about a 0.3 second response

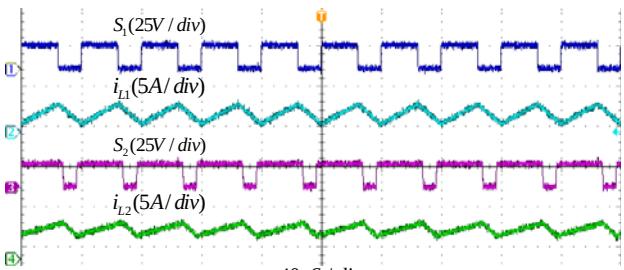


(a) Driven signals, inductor currents.

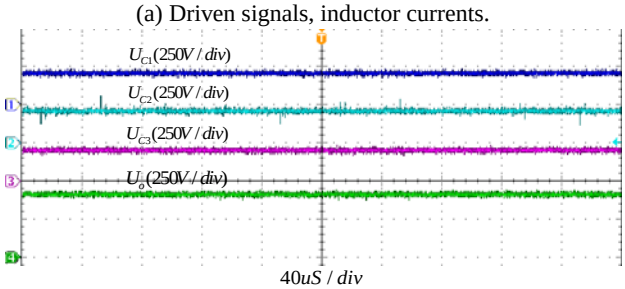


(b) Capacitor voltages and output voltage.

Fig. 11. Under SSP mode with U_{in1} 48V and U_{in2} 80V.

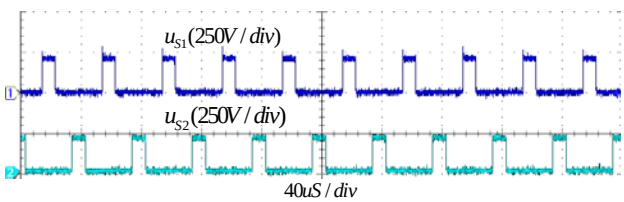


(a) Driven signals, inductor currents.

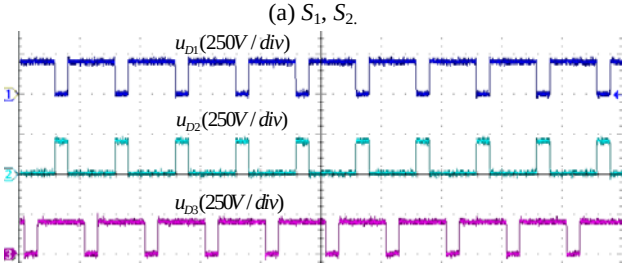


(b) Capacitor voltages and output voltage.

Fig.12. Under SSP mode with U_{in1} 80V and U_{in2} 48V.

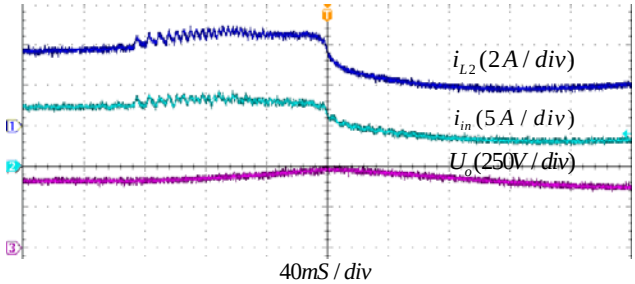


(a) S_1, S_2.

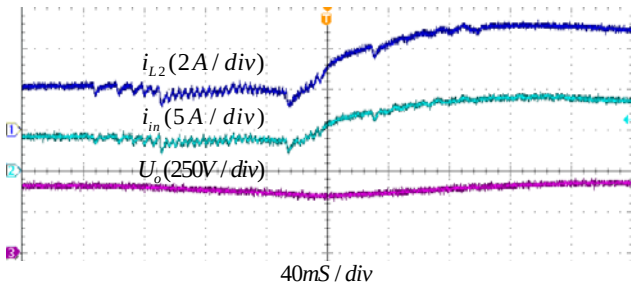


(b) D_1, D_2, D_3.

Fig. 13. Under ISP mode with U_{in1} 48V.



(a) U_{in1} with 48V jumps to U_{in2} with 80V.



(b) U_{in1} with 80V jumps to U_{in2} with 48V.

Fig.14. Dynamic experimental waveforms under ISP mode.

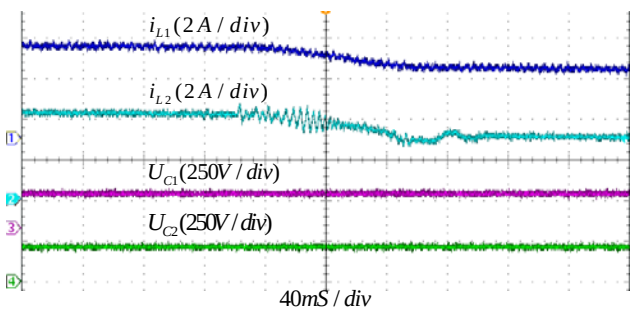


Fig.15. Dynamic experimental waveforms under SSP mode: U_{in1} jumps from 48V to 70V and U_{in2} jumps from 48V to 80V.

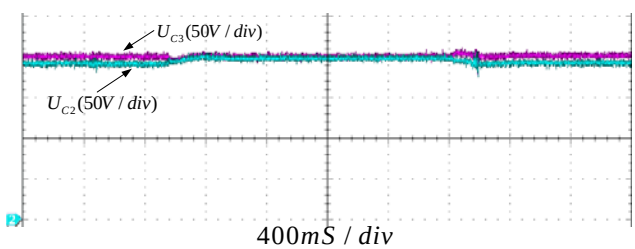


Fig.16. Dynamic voltage-balance process between C_1 and C_2 under ISP mode with U_{in1} 48V.

time under the two jump conditions. Under the SSP mode as shown in Fig.15, the two inductor currents become stable again after about a 0.2 second response time. During this period, the two output capacitor voltages do not change greatly.

Additionally, the dynamic voltage-balance process between C_1 and C_2 when the converter operates under the ISP mode when U_{in1} with 48V, is presented in Fig.16, in which the voltage-balance loop shown in Fig.6 is first not added and then added, and finally removed. It can be seen from Fig.16 that when the voltage-balance loop is not added, there is about a 5V voltage difference between U_{C1} and U_{C2}, where U_{C1} is 195V and U_{C2} is 200V. In addition, d_1 is equal to d_2

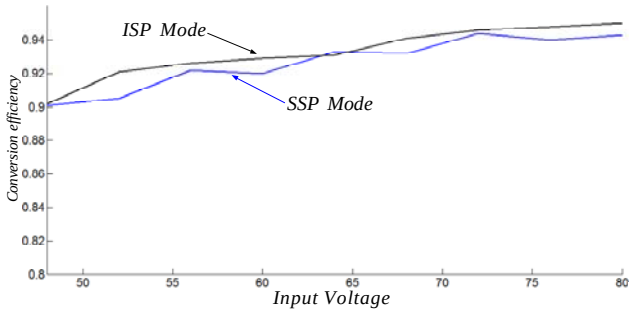


Fig. 17. Efficiency curves under ISP and SSP modes.

with the value 0.788. However, when the voltage-balance loop is added, U_{C1} and U_{C2} are both balanced with the same voltage 200V. In addition, d_1 is 0.797 and d_2 is 0.789 with a very small duty-cycle difference 0.008, which strongly supports (26). Furthermore, steady state and dynamic experimental results verify that the voltage-balance loop does not affect the voltage-current loop of the converter.

C. Efficiency Analysis

In the end, the conversion efficiency curve versus the input voltage for the DITLB converter under both the ISP mode and the SSP mode with different input voltages are presented in Fig. 17. For the ISP mode, the conversion efficiency curve is presented with the black line in Fig. 17 when input source 2 increases by 4V. For the SSP mode, the conversion efficiency curve is plotted with the blue line when the two input sources increase by 4V. Under the ISP mode, the maximum efficiency is 94.4% and the minimum efficiency is 90.1%. In addition, under the SSP mode, the maximum efficiency is 95.0% and the minimum efficiency is 90.2%. It can be concluded that as the input voltage increases, the conversion efficiency increases a little. When input voltage increases with a stable output voltage and a stable output power, the input current decreases. This reduces the conduction losses of the IGBTs and the power diodes.

Based on all of the experimental results, the operating principle analysis and the performance analysis for the proposed converter are correct and the closed-loop control strategy together with the voltage-balance control loop are feasible.

VI. Conclusion

This paper introduces a new interleaved DITLB converter, which can operate under both the ISP and SSP modes. The input current ripple is small since the converter can operate with an interleaved control scheme. The output capacitor voltages can be easily balanced by a simple voltage-balance control loop under the ISP mode. Under the SSP mode, the two output capacitor voltages are controlled to be equal since they are independently controlled by two voltage-current loops with the same referring capacitor voltage. Experimental results verify the effectiveness and feasibility of the proposed DITLB converter.

Acknowledgment

This work was supported by Fundamental Research Funds for the Central Universities, China, under Grant CDJXS12151109.

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