JPE 16-3-10

http://dx.doi.org/10.6113/JPE.2016.16.3.915
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Digital Self-Sustained Phase Shift Modulation Control Strategy for Full-Bridge LLC Resonant Converters

Kai Zheng†, Dongfang Zhou*, Jianbing Li*, Li Li*, and Yujing Zhao*

†,*Zhengzhou Information Science and Technology Institute, Zhengzhou, China

Abstract

A digital self-sustained phase shift modulation (DSSPSM) strategy that allows for good soft switching and dynamic response performance in the presence of step variations is presented in this paper. The working principle, soft switching characteristics, and voltage gain formulae of a LLC converter with DSSPSM have been provided separately. Furthermore, the method for realizing DSSPSM is proposed. Specifically, some key components of the proposed DSSPSM are carefully investigated, including a parameter variation analysis, the start-up process, and the zero-crossing capture of the resonant current. The simulation and experiment results verify the feasibility of the proposed control method. It is observed that the zero voltage switching of the switches and the zero current switching of the rectifier diodes can be easily realized in presence of step load variations.

Key words: Dynamic response, LLC resonant converter, Phase shift modulation, Soft switching, Step load variations, Traveling-wave tube microwave transmitter

I. INTRODUCTION

The traveling-wave tube (TWT) microwave transmitter has a wide bandwidth and a high gain, and it can be used for various applications, including communications, radar, electronic countermeasures, and space applications. The power converter is one of the key modules of the microwave transmitter, which is used to power the TWT. With the development of modern microwave systems, some parameter criterions of TWT power converters are gradually increasing, including the efficiency, power density, and dynamic response [1]-[3]. Resonant converter topologies are usually adopted to meet the high efficiency requirements of the TWT power converter, such as the parallel resonant converter, LCC resonant converter, and full-bridge phase-shift converter [4], [5]. Moreover, the LLC resonant converter has been attracting more and more attention due to its inherent merits, including high efficiency, high power density, soft switching, and low EMI [6]-[10]. Therefore, the LLC converter is a preferred candidate for microwave transmitters.

The TWT is a special load for a power converter. The TWT load is prone to sudden and repeated changes with the pulse modulation of pulsed microwave transmitters. Considering these step load variations, the power converter should possess good dynamic response and soft switching characteristics. At present, the power converter has not been widely studied in the context of such step load variations, especially with respect to transient soft switching. To overcome these drawbacks, the converter topology should be improved, and a novel applicable control strategy should be developed [11]-[14].

Self-sustained phase shift modulation (SSPSM) has been proposed for resonant converters in [15] and [16]. This control scheme is inspired by a timing signal from the resonant current. In this manner, the control system is insensitive to parameter uncertainties, and the gate pulses of the switches can be changed adaptively according to the operating conditions. Unlike the conventional frequency modulation (FM) control, SSPSM has much smaller frequency variation range [15], which makes it easy to optimize the magnetic components and to realize miniaturization. Unlike the conventional phase shift

Manuscript received Sep. 30, 2015; accepted Jan. 16, 2016
Recommended for publication by Associate Editor Joung-Hu Park.
†Corresponding Author: 401221515@qq.com
Tel: +86-186-2552-0283, Zhengzhou Information Sci. and Tech. Inst.
*Zhengzhou Information Science and Technology Institute, China

modulation (PSM) control, SSPSM can improve soft switching in a wide operation range, which can achieve a higher efficiency [15].

There has been considerable research on SSPSM [16]-[18]. The working principle and design method of a full-bridge LCC converter under SSPSM have been presented in [15]-[17]. The sliding-mode control of a full-bridge LCC converter under SSPSM has been introduced in [18]. These references mainly concentrate on the basic working principles of full-bridge LCC converters under SSPSM, in which the characteristics of SSPSM associated with the parameter variations have not been widely analyzed. In addition, in these references, the SSPSM is realized by analog circuits, which are quite complicated, and some of their control functions are difficult to implement. For example, the loop for adaptively compensating the sawtooth wave is difficult to achieve. Consequently, digital self-sustained phase shift modulation (DSSPSM) used for other novel converter topologies in the presence of parameter variations needs to be investigated further.

The major contribution of this paper is the design and development of a novel DSSPSM control strategy. Some new technical factors of DSSPSM, which are used for LLC converters in the presence of the step load variations have been proposed. First, the working principle of a LLC converter with DSSPSM is discussed, which provides new insights into the improvement of the soft switching and dynamic response characteristics of LLC converters. Second, the parameter design method of DSSPSM is presented, which is used to implement the soft switching. Third, a concrete realization method of DSSPSM is elaborated, especially in applications associated with parameter variations. Finally, the transient soft switching of the resonant converter is analyzed and evaluated.

The rest of this paper is organized as follows. The full bridge LLC resonant converter is discussed under DSSPSM in Section II. After that, the hardware and software realization of the DSSPSM is presented in Section III. Then, the key parts of the DSSPSM design are elaborated upon in Section IV. Simulation and experimental results are given in Section V. Finally, some concluding remarks are provided in Section VI.

II. Full Bridge LLC Resonant Converter under DSSPSM

A. Circuit Analysis

Fig. 1 shows a schematic of the proposed full-bridge LLC converter with a voltage multiplier rectifier under DSSPSM. The switch pairs Q_1 and Q_2 as well as Q_3 and Q_4 form the full-bridge inverter. The resonant inductor L_r, transformer magnetic inductor L_m, and resonant capacitor C_r form the LLC resonant tank. The diodes D_5 and D_6, and the capacitors C_5 and C_6 form the symmetrical multiplier rectifier. The

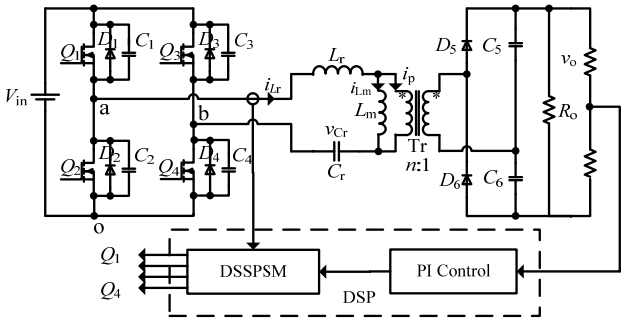


Fig. 1. Schematic of the proposed full-bridge LLC converter.

DSSPSM and proportional plus integral (PI) control are adopted to implement the feedback control.

The main features of the proposed converter can be summarized as follows.

1) Because the phase-shifting angle is the main control variable to regulate converters under DSSPSM, the switching frequency of a converter with DSSPSM has minimalistic variance, which can optimize the magnetic components and passive filters with respect to the volume and losses [15].

2) The timing signal of DSSPSM is derived from the resonant current, which can form a control loop. In this way, the control scheme can eliminate the sensitivity to parameter variations, and the control system can compensate for variations.

3) The control scheme can ensure that the resonant current i_{Lr} lags behind the inverter output voltage v_{ab} under any operating condition to realize zero voltage switching (ZVS) of the switches by adjusting the shifting-phase angle, which results in increased efficiency and improved reliability. In addition, zero current switching (ZCS) of the rectifier diodes can be easy to realize under DSSPSM.

4) A symmetrical voltage multiplier rectifier is proposed, which benefits the realization of a high-voltage output and miniaturization of power converters.

B. Working Principle

Fig. 2 shows the working principle of the proposed DSSPSM. γ_a is the phase angle between the reverse resonant current $-i_{Lr}$ and drain-source voltage v_{ao} of Q_2, and γ_b is the phase angle between the resonant current i_{Lr} and drain-source voltage v_{bo} of Q_4. The sawtooth wave v_{st} is a modulation wave, whose amplitude should be almost constant. v_{ca} and v_{cb} are two modulation lines; v_{ca} is the upper modulation line, v_{cb} is the lower modulation line, and $v_{ca} \geq v_{cb}$. If the gradient k of v_{st} is assumed to be constant, v_{ca} and v_{cb} can be described by the following functions, $v_{ca} = k\gamma_a$ and $v_{cb} = k\gamma_b$. Usually, v_{ca} is kept constant, and v_{cb} is used as the control variable to regulate the converter.

Fig. 3 shows typical waveforms of a LLC converter under DSSPSM. In terms of the timing diagrams, there are ten switching modes in a complete switching cycle, and the resonance mode between two components (L_r and C_r) and the

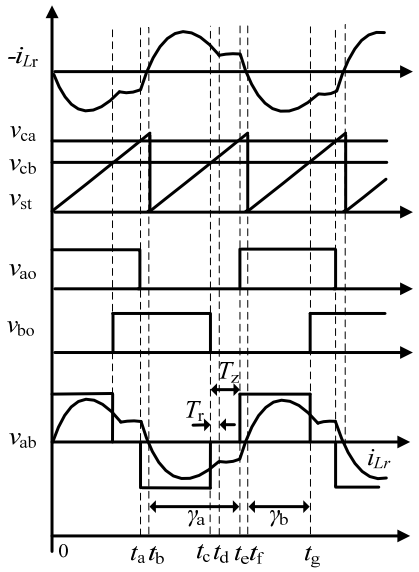


Fig. 2. Working principle of DSSPSM.

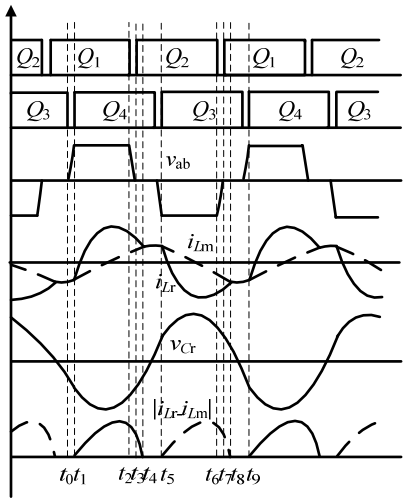


Fig. 3. Typical waveforms of LLC converter under DSSPSM.

resonance mode between three components (L_r, L_m and C_r) are involved. i_{Lr} is the resonant current, and i_{Lm} is the magnetizing current. When $i_{Lr} > i_{Lm}$, the two component resonance occurs. When $i_{Lr} = i_{Lm}$, the three component resonance occurs. The starting moment of the two component resonance (the stopping moment of the three component resonance) corresponds to the time when the switches are turned on or off, such as the times t_0 and t_2. The stopping moment of the two component resonance (the starting moment of the three component resonance) is not related to the time that the switches are turned on and off, such as the times t_1 and t_3. The energy of the resonant tank is sent to the load by the form ($i_{Lr} - i_{Lm}$).

C. Soft-Switching Analysis

1) ZVS Analysis of the Switches: In order to realize ZVS of the switches, according to Fig. 2, the polarity of the resonant current i_{Lr} should be kept in the dead time T_d between Q_1 & Q_2 or Q_3 & Q_4, and the limited condition is given by:

$$T_d < t_b - t_a \tag{1}$$

The function can be further expressed as:

$$T_d < (1 - \frac{v_{ca}}{V_p}) \frac{1}{2 f_s} \tag{2}$$

where, f_s is the switching frequency, and V_p is the amplitude of the sawtooth wave v_{st}.

Function (2) can be realized by selecting suitable parameters. In this situation, the resonant current i_{Lr} lags behind the inverter output voltage v_{ab}, and the zero crossing points of the resonant current are within the inverter output voltage pulse v_{ab}. When one switch is turned on, the resonant current flows through the antiparallel body diode of this switch, and then its drain-source voltage is clamped to zero. In this case, ZVS can be implemented.

2) ZCS Analysis of the Rectifier Diodes: Under DSSPSM, if $\gamma_a - \gamma_b > 0$, the period where $v_{ab} = 0$ is certain to exit in one switch cycle. In Fig. 2, T_z represents the period where $v_{ab} = 0$. At the beginning of $v_{ab} = 0$ (such as the moment t_c in Fig. 2), if $i_{Lr} = i_{Lm}$, the converter enters into the three component resonance. If $i_{Lr} > i_{Lm}$, the load power is supplied by the LC (L_r and C_r) resonant tank, the resonant current i_{Lr} decreases fast, and soon $i_{Lr} = i_{Lm}$. T_r represents this decreasing period. If $T_z > T_r$, the converter will enter into the three-component resonance.

In order to realize ZCS of the rectifier diodes, the three component resonance should always exist in one switch cycle, and the limited condition is given by:

$$T_r < t_d - t_c \tag{3}$$

The function can be further expressed as:

$$T_r < (1 - \frac{v_{cb}}{V_{ca}}) \frac{1}{2 f_s} \tag{4}$$

Function (4) can be realized by selecting suitable parameters. In this situation, all of the rectifier diodes are switched off with zero current. This reduces the reverse recovery losses of the diodes, which contributes to increased efficiency.

D. Modeling Analysis

In order to guide the circuit analysis and parameter design, based on the First Harmonic Approximation (FHA) method [19], [20], a LLC converter model under DSSPSM is built.

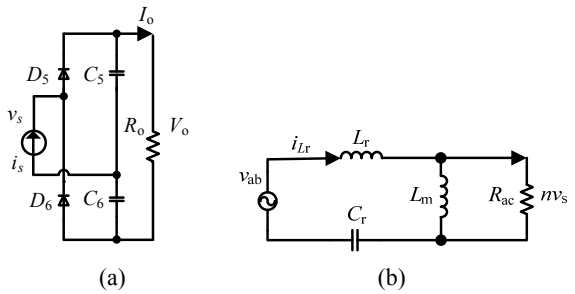
The fundamental component v_{ab1} of the inverter output voltage v_{ab} can be expressed as:

$$v_{ab1} = -\frac{\pi}{4} V_{in} \cos\left(\frac{\gamma_a - \gamma_b}{2}\right) \sin\left(\omega_s t - \frac{\gamma_a + \gamma_b}{2}\right) \tag{5}$$

The effective value V_{ab1} of v_{ab1} is described as:

$$V_{ab1} = \frac{2\sqrt{2}}{\pi} V_{in} \cos\left(\frac{\gamma_a - \gamma_b}{2}\right) \tag{6}$$

The symmetrical multiplier rectifier can be simplified as Fig. 4(a). The fundamental component v_{s1} of the inverter



(a) (b)

Fig. 4. Equivalent circuit of the LLC converter. (a) Symmetrical multiplier rectifier. (b) Equivalent circuit of the LLC converter.

voltage v_s can be expressed as:

$$v_{s1} = \frac{2V_o}{\pi}\sin(\omega_s t - \phi_R) \tag{7}$$

The RMS value (V_{s1}) of v_{s1} is described as:

$$V_{s1} = \sqrt{2}V_o / \pi \tag{8}$$

The fundamental component i_{s1} of the inverter current i_s can be expressed as:

$$i_{s1} = \frac{\pi}{2} I_o \sin(\omega_s t - \phi_R) \tag{9}$$

The equivalent reflected impedance R_{eq} of the multiplier rectifier can be derived as:

$$R_{eq} = \frac{v_{s1}}{i_{s1}} = \frac{4R_o}{\pi^2} \tag{10}$$

Through the above analysis, the equivalent circuit of the LLC converter can be shown as Fig. 4(b).

The equivalent reflected impedance R_{ac} on the primary side of the transformer can be expressed as:

$$R_{ac} = n^2 R_{eq} \tag{11}$$

The open loop transfer function of the LLC resonant tank can be given as:

$$G(j\omega_s) = \frac{j\omega_s L_m R_{ac} / (j\omega_s L_m + R_{ac})}{j\omega_s L_r + 1/(j\omega_s C_r) + j\omega_s L_m R_{ac} / (j\omega_s L_m + R_{ac})} \tag{12}$$

Considering (6), (8), and (12), the DC gain of the resonant tank can be obtained as:

$$|G(j\omega_s)| = \frac{nV_{s1}}{V_{ab1}} = \frac{V_o}{V_{in}} \frac{n}{2\cos[(\gamma_a - \gamma_b)/2]} \tag{13}$$

The DC gain of the LLC converter can be expressed as:

$$M(k,F,Q) = \frac{V_o}{V_{in}} = \frac{2}{n}\cos\left(\frac{\gamma_a - \gamma_b}{2}\right)|G(j\omega_s)|$$

$$= \frac{\frac{2}{n}\cos\left(\frac{\gamma_a - \gamma_b}{2}\right)}{\sqrt{[1+(1-1/F^2)/k]^2 + Q^2(F-1/F)^2}} \tag{14}$$

where: $F = \frac{f_s}{f_r}$, $k = \frac{L_m}{L_r}$, $Q = \frac{\sqrt{L_r/C_r}}{4R_o/n^2\pi^2}$, $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$.

According to (15), the voltage gain curves of a full-bridge LLC converter with DSSPSM are plotted, as shown in Fig. 5.

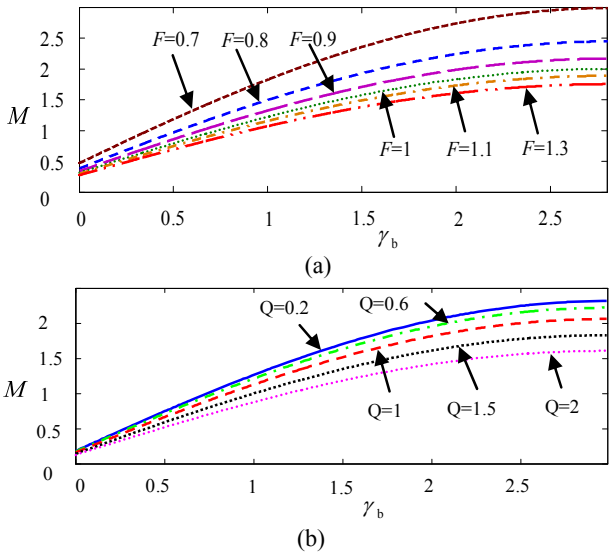


Fig. 5. Voltage gain curves versus γ_b. (a) Q =0.3, γ_a=0.9π, n=1, k=4. (b) F=0.9, γ_a=0.9π, n=1, k=4).

According to this figure, the voltage gain M increases with respect to the increase in phase γ_b. By controlling the phase γ_b, v_{cb} is controlled, and the converter can be regulated. In addition, when the frequency ratio F decreases, the phase γ_b varies little with the same gain change, and the gain range becomes wide, as shown in Fig. 5(a). When the quality factor Q increases, the voltage gain M becomes small, as shown in Fig. 5(b).

III. Realization of DSSPSM

A. Hardware Realization

Fig. 6 shows a hardware realization schematic of DSSPSM. Fig. 7 illustrates the main waveforms of DSSPSM based on a DSP. A DSP board by Texas Instruments (TMS320F2812) is primarily used to implement the control scheme. The general timer of the DSP event manager is set to the continuous incremental mode, and is used to generate the sawtooth wave v_{st}. The comparison unit registers CMPR1 and CMPR2 separately represent the modulation lines v_{ca} and v_{cb}. The logic signals v_{r1} and v_{r2} are separately obtained by comparing v_{st} with v_{ca} and v_{cb}. The zero-crossing moment of the resonant current can be captured by the DSP, and then the signal v_{r3} can be easily generated.

In Fig. 6, the logic signals v_{r1}, v_{r2}, and v_{r3} can be converted to the drive signals LQ1–LQ4, through the logic operations of NOT gate, NAND gate, and RS flip-flop. After that, the dead-time of LQ1-LQ4 is generated by the RCD circuit. Lastly, two drive chips Si8235 are used to drive the switches.

B. Software Realization

Fig. 8 shows software realization flowcharts of DSSPSM. The software is mainly composed of the main program and the interrupt programs, and the interrupt programs consist of

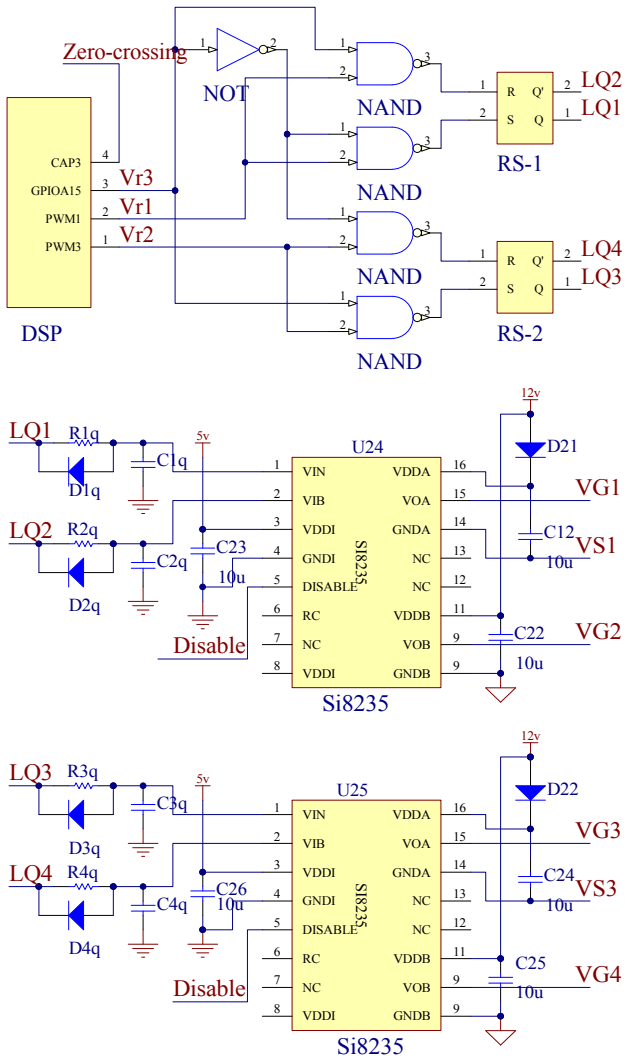


Fig. 6. Hardware schematic of DSSPSM.

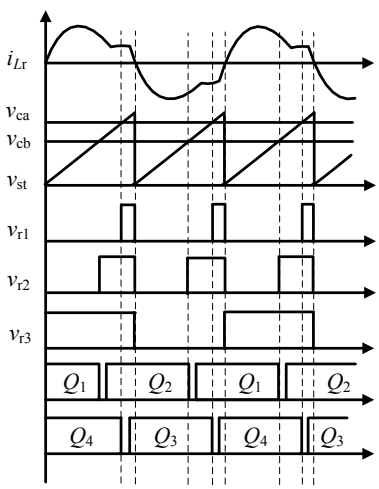


Fig. 7. Main waveforms of DSSPSM based on DSP.

the capture interrupt, the timer-underflow interrupt, and the analog-to-digital conversion (ADC) interrupt.

Fig. 8(a) shows the main program flowchart. The program initialization is carried out first, and then the main program

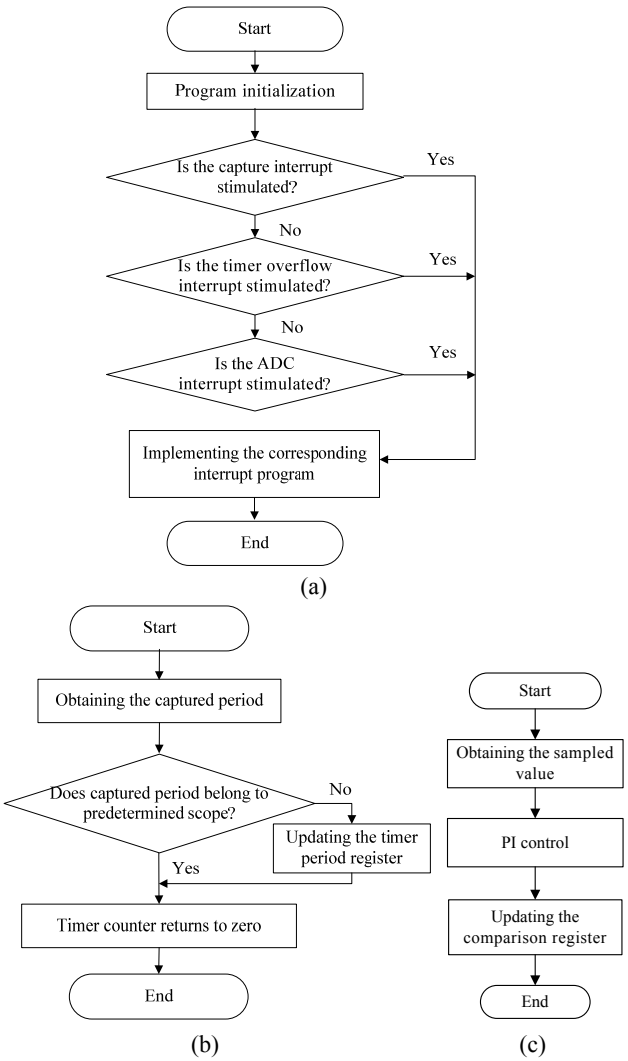


Fig. 8. Software flowcharts of DSSPSM. (a) Main program. (b) Capture interrupt program. (c) ADC interrupt program.

waits to respond to the interrupt flags.

Fig. 8(b) shows a capture interrupt program flowchart. The capture interrupt is stimulated at the zero-crossing moment of the resonant current. The zero-crossing moment can be captured, and the zero-crossing period can be calculated. If the captured period belongs to the predetermined scope, the timer counter returns to zero. If the captured period does not belong to the predetermined scope, the timer period register is updated.

The program flowchart of the timer underflow interrupt is relatively simple. The timer underflow interrupt is stimulated when the timer counter becomes zero. The zero-crossing square wave v_{r3} is generated in this program, and then the ADC converter is stimulated by the timer underflow interrupt flag.

Fig. 8(c) shows an ADC interrupt program flowchart. The ADC interrupt is stimulated by the ADC flag. After the sampled value is obtained, the feedback control signal can be calculated by the digital position PI control algorithm, and

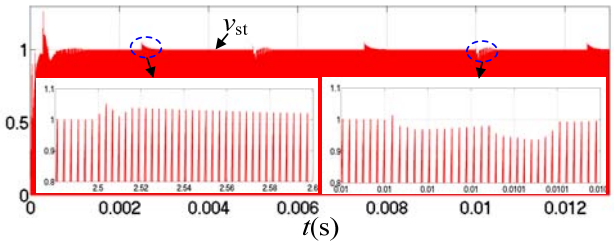


Fig. 9. Simulation results of sawtooth wave changes with respect to step load variations.

then the comparison register CMPR2 is updated by the feedback control value.

IV. Key Parts of DSSPSM Design

A. DSSPSM Design Regarding Parameter Variations

Parameter variations of the converter, such as step load variations, introduce some problems to the DSSPSM design. For instance, the sawtooth wave may have distortions. Fig. 9 shows simulation results of the sawtooth wave when the load is changed repeatedly between 600 Ω and 1200 Ω every 2.5 ms. It can be seen that the amplitude of the sawtooth wave begins to change at the load change moment. This phenomenon may lead to some mistakes, and some measures should be taken.

Fig. 10 shows two concrete mistakes associated with the sawtooth wave of DSSPSM.

As shown in Fig. 10(a), during the period $T_1(k+1)$, for the zero-crossing moment of the resonant current advances, the captured zero-crossing period $T_1(k+1)$ is less than the normal value $T_1(k)$, and the amplitude V_{p1} of the sawtooth wave is less than the normal amplitude T_{PR} of the sawtooth wave v_{st} in the period $T_1(k+1)$. In this situation, if the modulation line v_{ca} is larger than the amplitude V_{p1}, the logic signal v_{r1} cannot be obtained in the correct manner. As a result, the gate pulses of the switches will be wrong.

As shown in Fig. 10(b), during the period $T_2(k+1)$, for the zero-crossing moment of the resonant current delays, the captured zero-crossing period $T_2(k+1)$ is larger than the normal value $T_2(k)$, and two sawtooth waves will appear in the period $T_2(k+1)$. In this situation, the logic signal v_{r3} will be wrong. In addition, if the amplitude V_{p2} of the second sawtooth wave in the period $T_2(k+1)$ is larger than the modulation line v_{cb}, the logic signal v_{r2} can not be obtained in the correct manner. As a result, the gate pulses of the switches will be wrong.

In order to fix the two mistakes shown in Fig. 10, some measures should be taken.

1) For the mistake shown in Fig. 10(a), the parameter variations should be taken into consideration when selecting the value of v_{ca}. The value of v_{ca} should be always less than the normal amplitude T_{PR} of the sawtooth wave v_{st}. Moreover, if the captured amplitude V_{p1} is less than v_{ca}, the value of v_{ca}

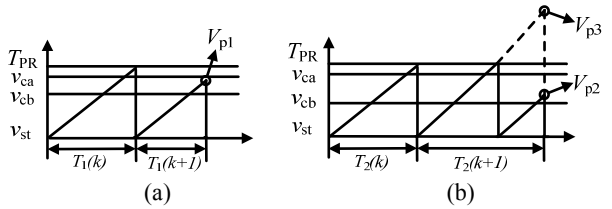


Fig. 10. Concrete mistakes of sawtooth wave of DSSPSM ((a) The first mistake and (b) The second mistake).

should be immediately updated as:

$$v_{ca} < V_{p1} \tag{15}$$

2) For the mistake shown in Fig. 10(b), if the captured zero-crossing period $T_2(k+1)$ is larger than the normal value $T_2(k)$, the value of T_{PR} should be immediately updated as:

$$T_{PR} > V_{p3} \tag{16}$$

B. Start-Up Process

There are several situations that warrant consideration in the start-up process.

1) The resonant current may not be regular and stable in the start-up process, and DSSPSM may become unreliable.

2) A sudden power-on may impact the converter hardware, so soft starting should be realized.

In order to solve these two problems, following measures should be taken.

1) In the start-up period, the traditional phase shift control is adopted first. When the converter becomes stable, the DSSPSM control begins to work.

2) The control signal v_{cb} varies slowly from zero to a predetermined value, and the pulse width of the inverter output voltage v_{ab} becomes gradually wider. In this way, soft starting can be realized.

C. Zero-Crossing Capture

Zero-crossing capture is a vital part of the DSSPSM design. If the zero-crossing moment cannot be correctly captured, DSSPSM may not work. Fig. 11 shows the zero-crossing detection circuit. A hall-effect current sensor TBC06DS3.3 is adopted to sample the resonant current, and the zero-crossing square-wave of the resonant current is obtained through an ultrafast comparator LT1720. However, the rising edge and falling edge of the square-wave may have some chattering. Therefore, the figuration function of this square-wave needs to be achieved through a RC filter and NOT gate 74LS14. In this way, the zero-crossing signal can be obtained in a correct manner, and sent to the capture port of the DSP.

V. Simulation and Experimental Results

A. Simulation Results

In order to evaluate the performance of the proposed DSSPSM control strategy, some simulation results are presented in this section. The simulations are carried out with

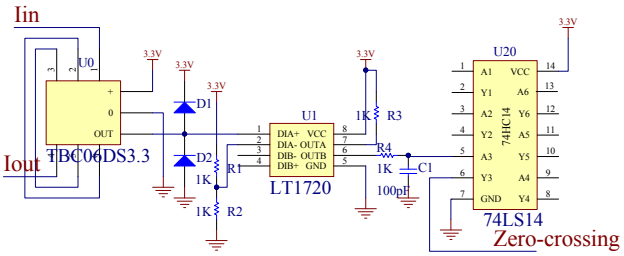


Fig. 11. Zero-crossing detection circuit.

TABLE I
CONVERTER PARAMETERS

Input voltage (V_{in})	270 V
Output voltage (V_o)	550 V
Resonant inductor (L_r)	104 μH
Resonant capacitor (C_r)	20 nF
Transformer magnetic inductor (L_m)	416 μH
Transformer turns ratio (n)	1:1
Output capacitor (C_o)	220 nF
Constant angle (γ_a)	0.9π

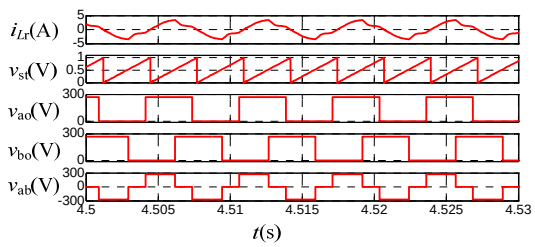


Fig. 12. Typical simulation waveforms of DSSPSM.

MATLAB/SIMULINK software.

The simulation and experiment are carried out on a LLC resonant converter with an input voltage of 270 V. The resonant frequency is set to 115 kHz with a L_r of 104 μH and a C_r of 20 nF. The magnetic inductor L_m is set to 416 μH. Thus, L_r/L_m is 4. The main parameters of the designed converter are shown in Table I.

Fig. 12 shows typical simulation waveforms of DSSPSM, including the resonant current i_{Lr}, the sawtooth wave v_{st}, the drain-source voltage v_{ao} of the switch Q_2, the drain-source voltage v_{bo} of the switch Q_4, and the inverter output voltage v_{ab}. As can be seen, the simulation results are in accordance with the theoretical analysis.

Fig. 13 shows a simulation waveform of the output voltage v_o with respect to step load variations. The load resistance is changed between 600 Ω and 1200 Ω every 2.5 ms. As can be seen, the output voltage v_o has a little ripple against the step load changes, and the converter stays stable during the entire process.

Fig. 14 shows simulation waveforms of the resonant current i_{Lr} and inverter output voltage v_{ab} in the presence of step load variations. As can be seen, i_{Lr} is kept lagging behind v_{ab} when the load resistance becomes larger or smaller. In this situation, when one switch is turned on, the resonant current flows through the antiparallel body diode and the drain-source voltage is clamped to zero. Then the ZVS can be realized.

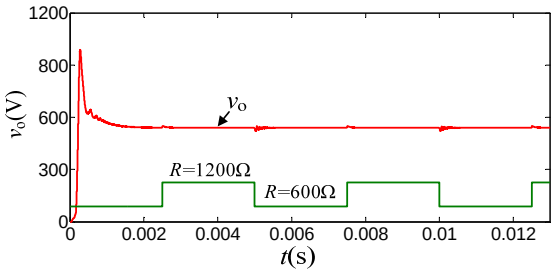


Fig. 13. Simulation waveform of output voltage v_o with respect to step load variations.

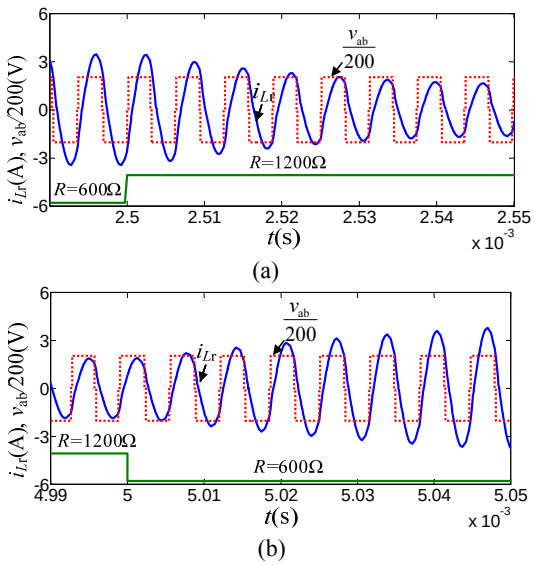


Fig. 14. Simulation waveforms of resonant current i_{Lr} and inverter output voltage v_{ab} with respect to step load variations ((a) From 600 Ω to 1200 Ω and (b) From 1200 Ω to 600 Ω).

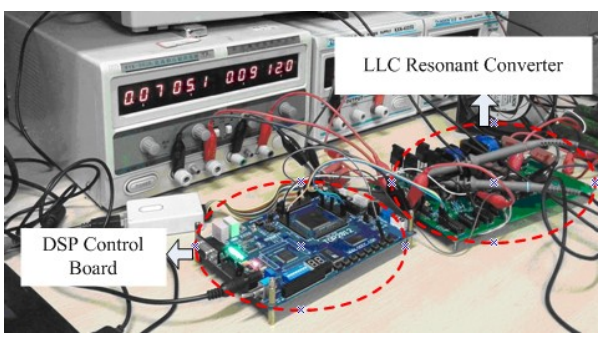
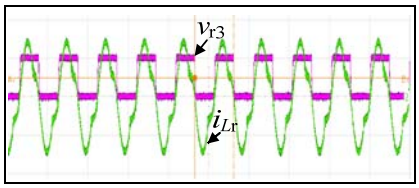


Fig. 15. Laboratory prototype.

B. Experimental Results

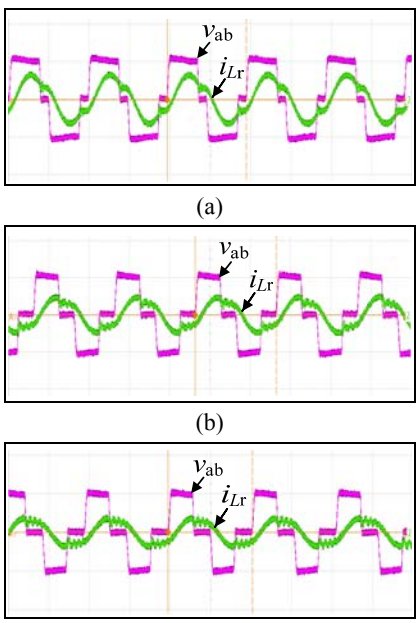
In order to investigate the performance of the proposed DSSPSM control strategy, a laboratory prototype has been built, as shown in Fig. 15. The parameters of the converter are listed in Table I.

1) Steady State Performance: Fig. 16 shows experimental waveforms of the resonant current i_{Lr} and zero-crossing square signal v_{r3} at a full load. As can be observed, there is no chattering in the rising edge or falling edge of v_{r3}, and the zero-crossing moment can be correctly captured by the DSP.



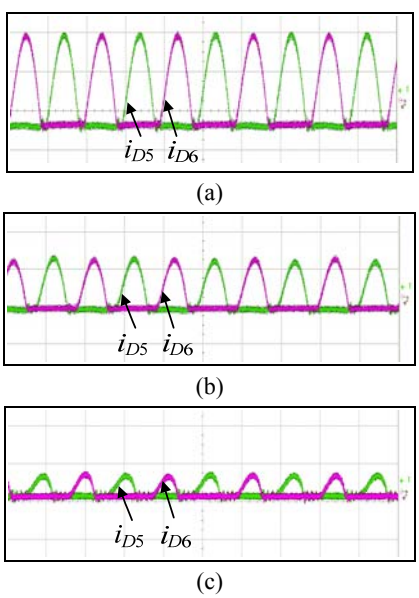
10 μs/div, v_{r3}: 2V/div, i_{Lr}: 3A/div

Fig. 16 Experimental waveforms of resonant current i_{Lr} and zero-crossing square wave v_{r3}.



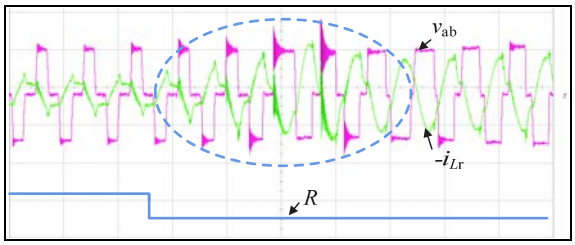
5 μs/div, v_{ab}: 270 V/div, i_{Lr}: 8 A/div

Fig. 17. Experimental waveforms of resonant current i_{Lr} and inverter output voltage v_{ab} ((a) Full load, (b) Half load and (c) Light load (10% load)).



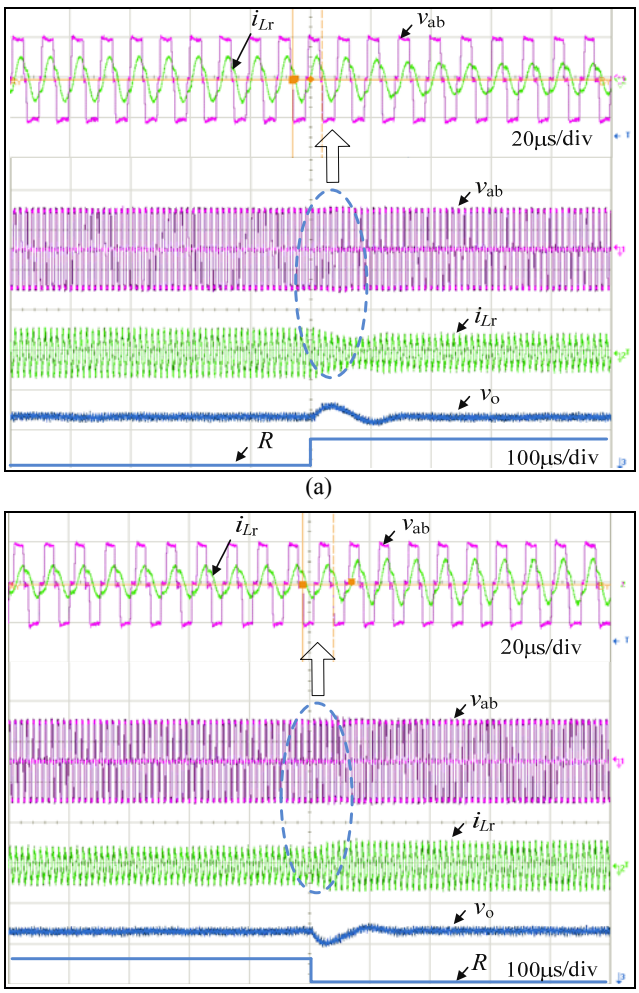
5 μs/div, i_{D5}: 0.6 A/div

Fig. 18. Experimental current waveforms of the rectifier diodes D_5 and D_6 ((a) Full load, (b) Half load and (c) Light load (10% load)).



10 μs/div, v_{ab}: 250 V/div, i_{Lr}: 4 A/div

Fig. 19. Transient waveforms under PSM for the step load variations.



v_{ab}: 270 V/div, i_{Lr}: 8 A/div, v_o: 5 V/div

Fig. 20. Transient waveforms under DSSPSM for the step load variations ((a) From 600 Ω to 1200 Ω and (b) From 1200 Ω to 600 Ω).

Fig. 17 shows experimental waveforms of the resonant current i_{Lr} and inverter output voltage v_{ab} at a full load, half load and light load (10% load). As can be seen, under different load conditions, i_{Lr} can lag behind v_{ab}, and all of the switches can implement ZVS which reduces the switching losses of the switches.

Fig. 18 shows experimental current waveforms of the rectifier diodes D_5 and D_6 at a full load, half load, and light

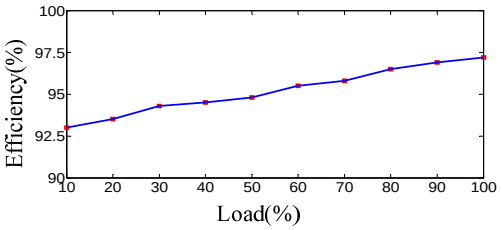


Fig. 21. Efficiency curve according to load.

load (10% load). All of the rectifier diodes can implement ZCS which reduces the reverse recovery losses of the rectifier diodes.

2) Dynamic State Performance: Fig. 19 shows transient waveforms of the reverse resonant current $-i_{Lr}$ and inverter output voltage v_{ab} under the conventional PSM in the presence of of step load variations. As can be seen, the current i_{Lr} cannot keep lagging behind the voltage v_{ab}, and sometimes the soft switching characteristic of the converter is not so good for the step load variations.

Fig. 20 shows transient waveforms of the resonant current i_{Lr}, inverter output voltage v_{ab} and output voltage v_o under DSSPSM in the presence of step load variations. Fig. 20(a) shows waveforms when the load resistance increases. Fig. 20(b) shows waveforms when the load resistance decreases. The load resistance is changed between 600 Ω and 1200 Ω, and the load changing transition time is less than 200 ns.

As can be seen, i_{Lr} is kept lagging behind v_{ab} for step load variations, and ZVS can always be implemented. In addition, the converter has good dynamic performance, and the output voltage v_o can be tightly regulated at 550 V. The response time is less than 150 μs, and the output voltage overshoot and undershoot are less than 1% of 550 V.

3) Efficiency Analysis: Fig. 21 shows an efficiency curve according to the load. The figure indicates that the efficiencies under different load conditions are higher than 92%, and their variance is minimalistic. The soft switching of the LLC converter with DSSPSM can be realized under different load conditions leading to an improved efficiency in a wide operation range.

VI. Conclusion

In this paper, a novel DSSPSM control strategy is proposed, and a full bridge LLC resonant converter with a multiplier rectifier under DSSPSM is introduced. The working principle, soft-switching characteristic, and realization procedure of DSSPSM are separately analyzed. Simulation and experimental results validate that the proposed LLC converter under DSSPSM has a good dynamic performance and soft switching characteristics in presence of the step load variations. Therefore, the proposed DSSPSM control strategy is valuable for improving the efficiency and power density of power converters. In addition, a simulated resistance load is used to represent a TWT in the simulation and experiment, which makes it easy to test the steady-state and dynamic-state performance of DSSPSM. In future work, the practical application of DSSPSM in TWT microwave transmitters will be explored.

References

[1] N. V. Bijeev, A. Malhotra, and V. Kumar, "Design and realization challenges of power supplies for space TWT," *in Proc. IEEE Vacuum Electronics Conference*, pp. 431-432, 2011.

[2] I. Barbi and R. Gules, "Isolated DC-DC converters with high-output voltage for TWTA Telecommunication Satellite Applications," *IEEE Trans. Power Electron.*, Vol. 18, No. 4, pp. 975-984, Jul. 2003.

[3] D. Springmann, D. Chan, and T. Schoemehl, "A 50W Ka-band NanoMPM," in *Proc. IEEE Vacuum Electronics Conference*, pp. 123-124, 2014.

[4] A. K. Singh, P. Das, and M. Pahlevaninezhad, "A novel high output voltage DC-DC LLC resonant converter with symmetric voltage quadrupler rectifier for RF communications," in *Proc. IEEE Telecommunications Energy Conference*, pp. 1-6, 2014.

[5] G. Zhang, D. Zhou, and L. Yang, "Development of novel type of two-stage high voltage converter," *Chinese Journal of Vacuum Science and Technology*, Vol. 33, No. 5, pp. 419-425, May 2013.

[6] B. Yang, "Topology investigation for front end DC/DC power conversion for distributed power system," Ph.D. Dissertation, Virgina Polytechnic Institute and State University, USA, 2003.

[7] R. Beiranvand, B. Rashidian, M.R. Zolghadri, and S. M. H. Alavi, "A design procedure for optimizing the LLC resonant converter as a wide output range voltage source," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3749-3763, Aug. 2012.

[8] W. Feng, F. C. Lee, and P. Mattavelli, "Simplified optimal trajectory control (SOTC) for LLC resonant converters," *IEEE Trans. Power Electron.*, Vol. 28, No. 5, pp. 2415-2426, May 2013.

[9] X. D. Li, "LLC-type dual-bridge resonant converter: Analysis, design, simulation, and experimental results," *IEEE Trans. Power Electron.*, Vol. 29, No. 8, PP. 4313-4321, Aug. 2014.

[10] Y. Zhao, X. Xiang, W. Li, and X. He, "Advanced symmetrical voltage quadrupler rectifiers for high step-up and high output-voltage Converters," *IEEE Trans. Power Electron.*, Vol. 28, No. 4, PP. 1622-1631, Apr. 2013.

[11] H. Pan, C. He, and F. Ajmal, "Pulse-width modulation control strategy for high efficiency LLC resonant converter with light load applications," *IET Power Electron.*, Vol. 7, No. 11, PP. 2887-2894, Nov. 2014.

[12] N. Shafiei, M. Ordonez, M. Cracium, and M. Edington, "High power LLC battery charger: Wide regulation using phase-shift for recovery mode," in *Proc. IEEE Energy Conversion Congress and Exposition*, PP. 2037-2042, 2014.

[13] X. F. Sun, Y. F. Shen, Y. Zhu, and X. Guo, "Interleaved boost-integrated LLC resonant converter with fixed-frequency PWM control for renewable energy generation applications," *IEEE Trans. Power Electron.*, Vol. 30, No. 8, PP. 4312-4326, Aug. 2015.

[14] C. Buccella, C. Cecati, H. Latafat, and P. Pape, "Observer-based control of LLC DC/DC resonant converter using extended describing functions," *IEEE Trans. Power Electron.*, Vol. 30, No. 10, PP. 5881-5891, Oct. 2015.
[15] Z. Y. Mohamed and K. J. Praveen, "A review and performance evaluation of control Techniques in resonant converters," in *Proc. IEEE Industrial Electronics Society*, PP. 215-221, 2004.
[16] Z. Y. Mohamed, P. Humberto, and K. J. Praveen, "Self-sustained phase shift modulated resonant converters: Modeling, design, and performance," *IEEE Trans. Power Electron.*, Vol. 21, No. 2, PP. 401-414, Mar. 2006.
[17] Z. Y. Mohamed, "Control and modeling of high frequency resonant DC/DC converters for powering the next generation microprocessors," Ph. D. Dissertation, Queen's University, Canada, 2005.
[18] L. S. Jorge, C. Miguel, and M. Jaume, "Modeling and performance analysis of the DC/DC series–parallel resonant converter operating with discrete self-sustained phase-shift modulation technique," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 3, PP. 697-705, Mar. 2009.
[19] X. Fang, H. Hu, J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the LLC resonant converter," *IEEE Trans. Power Electron.*, Vol. 27, No. 4, PP. 1985-1995, Apr. 2012.
[20] Y. J. Park, H. J. Kim, J. Y. Chun, J. Y. Lee, Y. G. Pu, and K. Y. Lee, "A wide frequency range LLC resonant controller IC with a phase-domain resonance deviation prevention circuit for LED backlight units," *Journal of Power Electronics*, Vol. 15, No. 4, pp. 861-875, Jul. 2007.

Kai Zheng was born in Henan Province, China. He received his B.S. and M.S. degrees in Electrical Engineering from the New Star Research Institute of Applied Technology, Hefei, China, in 2005 and 2009, respectively. He is presently working toward his Ph.D. degree in Electrical Engineering at the Zhengzhou Information Science and Technology Institute, Zhengzhou, China. His current research interests include the modeling and control of resonant power converters.

Dongfang Zhou was born in Zhejiang Province, China. He received his B.S. degree in Electrical Engineering from the Zhengzhou Information Science and Technology Institute, Zhengzhou, China, in 1983; his M.S. degree in Electrical Engineering from Xidian University, Xi'an, China, in 1989; and his Ph.D. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2005. He is presently working as a Professor in the Zhengzhou Information Science and Technology Institute. His current research interests include power electronics and the control of microwave systems.

Jianbing Li was born in Hubei Province, China. He received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from the Zhengzhou Information Science and Technology Institute, Zhengzhou, China, in 1999, 2002 and 2006, respectively. He is presently working as an Associate Professor in the Zhengzhou Information Science and Technology Institute. His current research interests include power electronics and control.

Li Li was born in Henan Province, China. She received her B.S. degree in Electrical Engineering from the North China University of Water Resources and Electric Power, Zhengzhou, China, in 2012. She is presently working towards her M.S. degree in Electrical Engineering at the Zhengzhou Information Science and Technology Institute, Zhengzhou, China. Her current research interests include the topologies and control of power converters.

Yujing Zhao was born in Henan Province, China. He received his B.S. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 2012. He is presently working towards his M.S. degree in Electrical Engineering at the Zhengzhou Information Science and Technology Institute, Zhengzhou, China. His current research interests include the topologies and control of power converters.