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The Impact of Parasitic Elements on Spurious Turn-On in Phase-Shifted Full-Bridge Converters

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Abstract

This paper presents a comprehensive analysis of the spurious turn-on phenomena in phase-shifted full-bridge (PSFB) converters. The conventional analysis of the spurious turn-on phenomenon does not establish in the PSFB converter as realizing zero voltage switching (ZVS). Firstly, a circuit model is proposed taking into account the parasitic capacitors and inductors of the transistors, as well as the parasitic elements of the power circuit loop. Second, an exhaustive investigation into the impact of all these parasitic elements on the spurious turn-on is conducted. It has been found that the spurious turn-on phenomenon is mainly attributed to the parasitic inductors of the power circuit loop, while the parasitic inductors of the transistors have a weak impact on this phenomenon. In addition, the operation principle of the PSFB converter makes the leading and lagging legs have distinguished differences with respect to the spurious turn-on problems. Design guidelines are given based on the theoretical analysis. Finally, detailed simulation and experimental results obtained with a 1.5 kW PSFB converter are given to validate proposed analysis.

Key words: Crosstalk, Leading and lagging legs, Parasitic inductor, Spurious turn-on

I. INTRODUCTION

The phase-shifted full-bridge (PSFB) converter is applied in medium to high power conversions due to its attractive features including a simple circuit, constant operation frequency and ZVS-on of the primary switches [1]-[5]. This type of converter has been extensively studied in the literature, including modeling, design optimization, control method, flux bias compensation, improved full-bridge topologies, etc. [6]-[10].

Despite all its merits, the PSFB converter has the risk of spurious turn-on of the transistors. The interaction between the upper and lower transistors in a bridge leg during a switching transient (crosstalk) can appear. This leads to additional switching losses and overstress of the power devices. With the increased demand for high power density, larger currents and higher switching frequencies are the new trends for power supplies. Under these circumstances, the effects of the circuit parasitic parameters on the converter's performance are becoming more and more significant [11]. As a result, the PSFB converter is becoming more vulnerable to spurious turn-on problems.

Actually, the spurious turn-on phenomena in power switching converters and has been studied in many works [12]-[17]. In these studies, the spurious turn-on phenomena are mainly induced by the hard switching of transistors. High dv/dt during fast switching on the transient of one device affects the operating behavior of its complementary device [12]-[15]. Meanwhile, the high di/dt induces a negative voltage across the parasitic source inductor of the MOSFET, pulling down its source voltage [16], [17]. The parasitic source inductor, the recovery current presented by the body diode, and the parasitic capacitors are thought to be the key elements of the spurious turn-on phenomena in hard switching power converters. However, in PSFB converters, ZVS on is achieved and the conventional analysis does not apply here. In addition, the mechanism of the spurious turn-on phenomena in PSFB converters has been rarely analyzed comprehensively. Thus, it is very meaningful to conduct studies on phase-shifted full-bridge converters.

In this paper, the switching transition when the spurious turn-on phenomenon occurs in a PSFB converter will be specified by an analytical model, which takes into account the parasitic inductors of the power circuit loop, as well as the parasitic capacitors and inductors of the transistors. According to the analysis, the parasitic inductors of the power circuit loop

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are the key elements of the spurious turn-on in PSFB converters, while the parasitic source inductors and the recovery current presented by the body diode have weak impacts on this phenomenon since ZVS-on is realized here. Design guidelines for reducing the spurious triggering pulse are then given. At last, a series of simulation and experimental results will be provided to verify the theoretical analysis.

II. Spurious Turn-On Phenomenon

A. Operation Principle of PSFB Converters

Fig. 1(a) and (b) show a circuit diagram [1], [18] and key waveforms [18], [19] of the standard PSFB converter. According to Fig. 1(a), a PSFB converter is formed by four transistors Q_1-Q_4, a power transformer T_r, a resonant inductor L_R (including the leakage inductor), output rectifier diodes D_{R1} and D_{R2}, an output filter inductor L_f and a capacitor C_f. Meanwhile, as shown in Fig. 1(b), Q_3 and Q_4 are switched on/off before Q_1 and Q_2. Thus, the Q_3-Q_4 leg is designated as the "leading leg", while the Q_1-Q_2 leg is designated as the "lagging leg". The primary current I_p reaches its peak value when the transistor of the leading leg is turned off.

It is well known that ZVS turn-on can be achieved by utilizing the energy stored in the resonant inductor L_R to charge and discharge the parasitic capacitors of MOSFETs [19]. The voltage across the drain-to-source terminals of a MOSFET should be discharged to zero before it is switched on. Meanwhile, the current through the MOSFET decreases to zero. This transition interval (TI), between t_b-t_2, is accomplished during the turn off procedure of the MOSFET as shown in Fig. 2 [20], [21]. The voltage across the drain-to-source terminals of the MOSFET and current through the MOSFET change drastically. For example, the voltage across the drain-to-source terminals of Q_4 is charged to V_{in} and the voltage across the drain-to-source terminals of Q_3 is discharged to zero during the turn-off procedure of Q_4. Meanwhile, the drain current of Q_4 decreases to zero during this interval.

B. Spurious Turn-On in Practice

According to the analysis in [15], in the soft-switching power converters, during the turn-off transient of the lower switch, the negative spurious voltage induced at the gate–source terminals of the upper switch may overstress the power device if its magnitude exceeds the maximum allowable negative gate voltage that is acceptable to the semiconductor device. For example, when Q_4 is turned off, there is a negative spurious voltage across the gate–source terminals of Q_3. However, in addition to a negative spurious voltage at the gate–source terminals of the complementary transistor, a positive spurious voltage is observed at the gate-source terminals of the transistors. This is shown in Fig. 3, which is directly obtained from a 1.5 kW phase-shifted full-bridge converter. Since the Q_1-Q_2 leg is the lagging leg, Q_1 is still on when Q_4 is turned off and the spurious turn-on of Q_2 leads to an

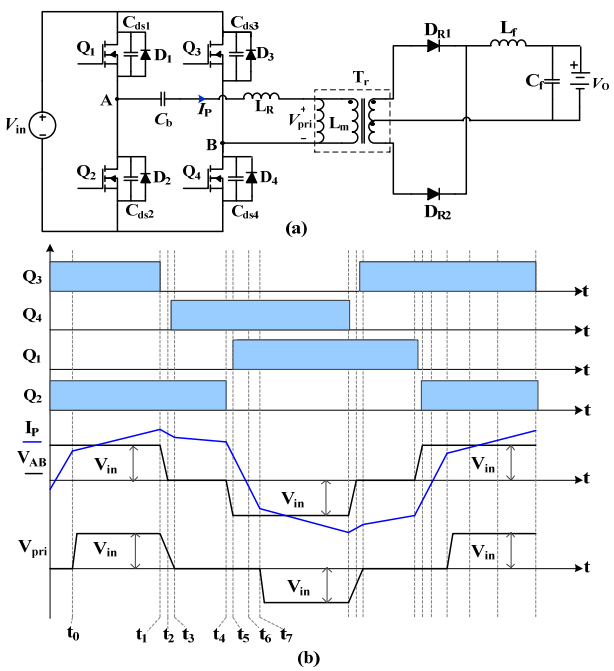


Fig. 1. PSFB converter topology and key waveforms.

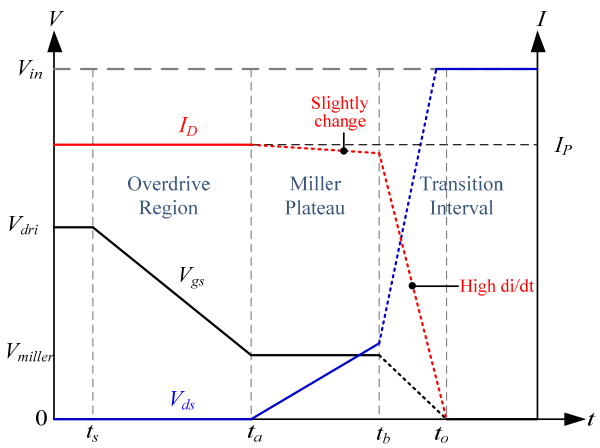


Fig. 2. Turn-off procedure of MOSFET in PSFB converter.

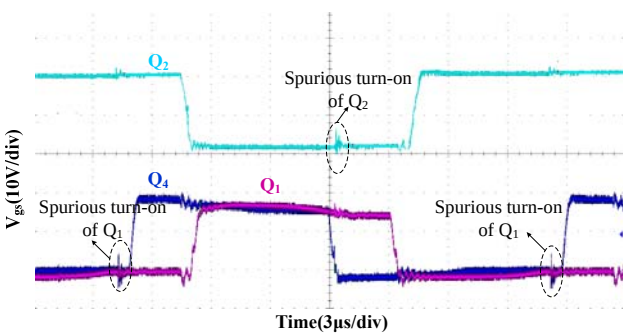


Fig. 3. Spurious turn-on of the transistors in lagging leg.

interaction between the transistors of the lagging leg (crosstalk).

Actually, a positive induced voltage can be observed during every transistor's turn-off procedure. As shown in Fig. 3, when the transistor in a lagging leg, such as Q_2, is turned

off, an oscillation can be observed at the gate-to-source terminals of Q_4. However, the amplitude of the voltage oscillation is much smaller than the positive voltage when the transistor in the leading leg is turned off. A detail analysis and explanations are given in Section III.

III. Mechanism Analysis and Design Guidelines

A. Circuit Modeling and Mechanism Analysis

An equivalent circuit model of a PSFB converter is shown in Fig. 4. The parasitic elements considered for the transistors are the gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, drain-source capacitance C_{ds}, internal gate inductor $L_{g\text{-}in}$, drain inductor $L_{d\text{-}in}$, source inductor $L_{s\text{-}in}$, and the body diode D. The drain inductor $L_{d\text{-}cw}$ and source inductor $L_{s\text{-}cw}$ are the parasitic inductors introduced by the copper wires and the pads of the printed circuit board. In addition, the parasitic inductors of the power circuit loop, L_{pc1}, L_{pc2}, L_{pc3} and L_{pc4}, are considered in the proposed equivalent circuit model. It should be noted that the proposed equivalent circuit model is valid only when a PSFB converter has a large power (usually larger than 500W) and is realized within the printed circuit board (PCB). The large power of the converter means bulky capacitors with a large size at the input terminal [22]. As a result, the copper lines from the drain node to the input capacitor are long enough to produce parasitic inductors. This can be verified by the layout shown in Fig. 8. These parasitic inductors, which are introduced by the copper wires of the power circuit loop, have been neglected in previous analyses since they are not involved in the gate drive loop, as shown in Fig. 4, and are thought to be irrelevant in terms of the spurious turn-on phenomena. However, the occurrence of crosstalk is mainly induced by the parasitic inductors of the power circuit loop due to the special operation principle of the PSFB converter. Detailed analyses are shown as follows.

Since the oscillation is observed during the turn-off procedure, the converter is analyzed in four different modes, as shown in Fig. 2: (1) *Energy transfer and overdrive region* (before t_a). (2) *Miller Plateau* (t_a~t_b). (3) *Transition interval* (t_b~t_o). (4) *Circulating mode* (after t_o). Equivalent circuits of the four operating modes are illustrated in Fig. 5. For simplicity, the output stage is not shown in the equivalent circuits.

Due to the symmetric nature of the two bridge legs, the analysis process for each transistor is similar. Therefore the turn-off procedure of Q_4 is taken as an example. Details of each operation mode are described as follows.

Mode 1 [Energy transfer, before t_a]

This is an energy transfer mode. The diagonal switches Q_1 and Q_4 were conducting. The primary current flows through the diagonal transistor Q_1 in the lagging leg and the transistor Q_4 in the leading leg. This is shown in Fig. 5(a). At t_a, the primary current reaches its maximum value and can be expressed as [1]:

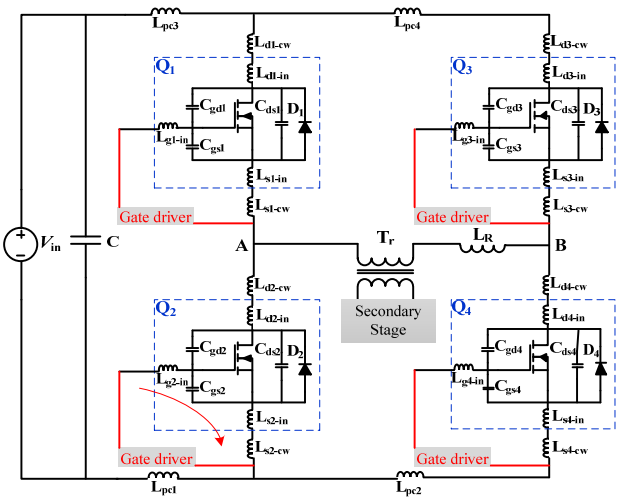


Fig. 4. Equivalent circuit of a PSFB converter.

$$I_{d4} = IP_{ta} = \frac{I_o}{N} + \frac{\left(\frac{V_{in}}{N} - V_o\right)V_o T_s}{4L_f V_{in}} + \frac{NT_s V_o}{2L_m} \tag{1}$$

This mode ends when the drain current of Q_4 starts to decrease, which starts at t_a according to Fig. 2.

Mode 2 [Miller Plateau，t_a-t_b]

This stage begins when the gate-to-source voltage V_{gs} decreases to the Miller Plateau level V_{miller}. During this stage, the gate-to-drain capacitor C_{gd} is charged by the driving current, and the drain-to-source capacitor C_{ds} is charged by the primary current. Although the current through the resonant inductor L_R is nearly constant, the current through Q_4 (including D_4 and C_{ds4}) starts to decrease. This is the beginning of the ZVS procedure.

It should be pointed out that the current through Q_4 changes slightly in this plateau. This is because the driving current is mainly used to discharge the gate-to-drain parasitic capacitor. This is not shown in Fig. 5.

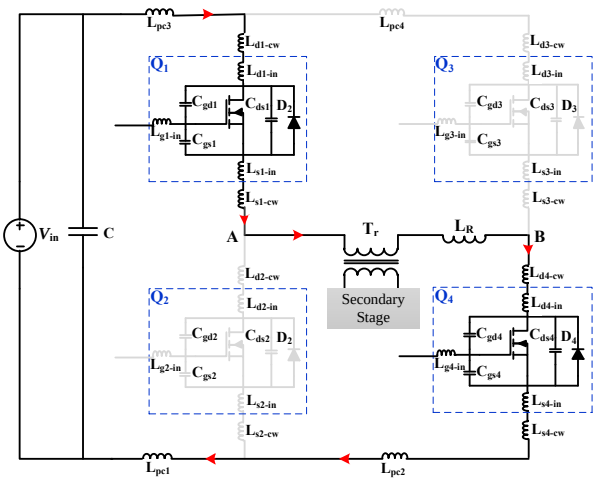
Mode 3 [Transition Interval, t_b~t_o]

According to Fig. 2, the gate-to-source voltage of Q_4 starts to decrease at t_b. Therefore, the current through the channel of Q_4 decreases drastically. The primary current flows through both of the drain-to-source parasitic capacitors of Q_3 and Q_4. Obviously, the current through Q_4 is same as the current through the parasitic inductors L_{pc1}, L_{pc2} and L_{pc3} as shown in Fig. 5(b).

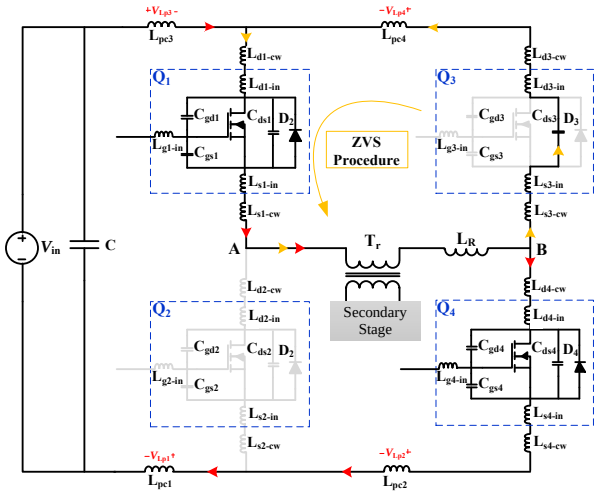
$$I_{Lp1} = I_{Lp2} = I_{Lp3} = I_{d4} \tag{2}$$

where I_{Lp1} ,I_{Lp2} and I_{Lp3} are the currents through the parasitic inductors L_{pc1}, L_{pc2} and L_{pc3}.

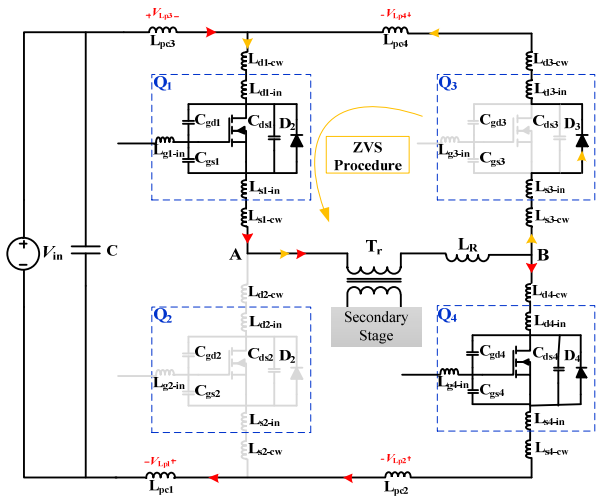
Therefore, the currents through the parasitic inductors L_{pc1}, L_{pc2} and L_{pc3} decrease drastically. With the decreasing of the current, there is an inductive voltage across the parasitic inductors, which is shown in Fig. 5 (b). Among them, V_{Lp1} can be expressed as:



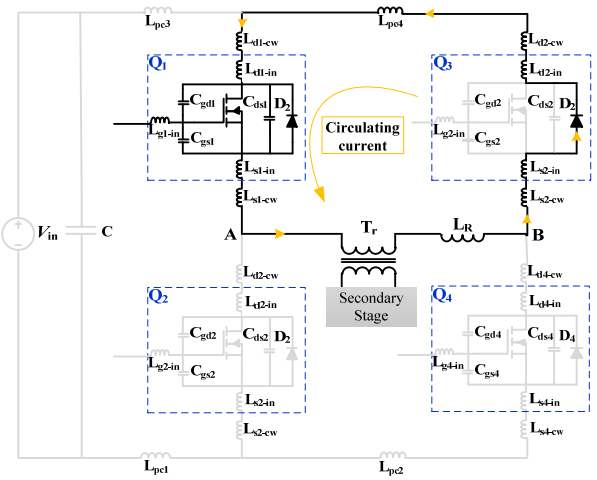
(a) Energy Transfer.



(b) Stage 1 of Transition interval.



(c) Stage 2 of Transition interval.



(d) Circulating Mode.

Fig. 5. Equivalent circuits of different operating modes.

$$V_{Lp1}=-L_{pc1}\frac{dI_{Lp1}}{dt} \quad (3)$$

Similarly, there are inductive voltages across L_{pc2} and L_{pc3}. The expressions of the two inductive voltages can be deduced as:

$$V_{Lp2}=-L_{pc2}\frac{dI_{Lp1}}{dt} \quad (4)$$

$$V_{Lp3}=-L_{pc3}\frac{dI_{Lp1}}{dt} \quad (5)$$

The parasitic inductors around the transistor and the gate driver loop can be summarized as:

$$L_s=L_{s-in}+L_{s-cw} \quad (6)$$

$$L_d=L_{d-in}+L_{d-cw} \quad (7)$$

According to Fig. 5(b), during the transition interval, the current through the parasitic inductors around Q_2 remains constant. Therefore, the parasitic inductors of the transistor have a weak influence on the spurious turn-on phenomenon of Q_2. It should be noticed that the current through the parasitic inductors around Q_4 also changes during this interval. An analysis of this has been presented in [17] and is not be shown here. More importantly, the inductive voltage across the parasitic inductors of the power circuit loop may lead to the spurious turn-on phenomena since the parasitic inductances of the power circuit loop is much larger than the parasitic inductances around the MOSFETs. To be specific, the negative induced voltage across L_{pc1} may lead to the spurious turn-on phenomenon of Q_2 and the crosstalk of the lagging leg occurs when Q_1 is still on. The negative induced voltage across L_{pc1} and L_{pc2} may lead to a positive voltage across the gate-to-source terminals of Q_4 and increase the switching loss. The negative induced voltage across L_{pc3} leads to a positive voltage across the gate-to-source terminals of Q_1. The positive induced voltage of Q_1 has no significant influence unless the voltage amplitude exceeds the maximum tolerant voltage.

In order to obtain the maximum amplitude of the positive induced voltage, the decreasing slope of I_{Lp1} is deduced as

follows. According to Fig. 2, the current decreasing slope changes in *Mode 2*. Therefore, the transition interval can be divided into two stages.

***Stage 1 (t_b-t_c)*:** At the beginning of the transition interval, the primary current keeps flowing using the switch channel and its drain-to-source parasitic capacitor, C_{ds4}. This charges the drain-to-source parasitic capacitance of Q_4 from essentially zero volts to the upper voltage rail, V_{in}. Simultaneously, the drain-to-source parasitic capacitor of the switch Q_3 is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions the switch Q_3 with no drain to the source voltage prior to turn-on and facilitates lossless, zero voltage switching. This is shown in Fig. 5(c).

Therefore, during *Stage 1*, the primary current is equal to the sum of three parts: I_{c4} (the current through the channel of Q_4), I_{Cds4} (the current through the drain-to-source parasitic capacitor of Q_4) and I_{Cds3} (the current through the drain-to-source parasitic capacitor of Q_3).

$$IP_{t1} = I_{c4} + I_{Cds4} + I_{Cds3} \tag{8}$$

Among them, the voltage transition rates of C_{ds3} and C_{ds4} are equal, and C_{ds3} is equal to C_{ds4} since the same type of MOSFETs are adopted. Therefore, I_{Cds4} is equal to I_{Cds3} according to following equations.

$$I_{Cds4}=C_{ds4}\frac{dV_{ds4}}{dt} \tag{9}$$

$$I_{Cds3}=C_{ds3}\frac{dV_{ds3}}{dt} \tag{10}$$

The current through Q_4 can be expressed as:

$$I_{d4} = I_{c4} + I_{Cds4} \tag{11}$$

The relationship between V_{gs4} and I_{c4} can be deduced as follows.

$$I_{c4} = g_m(V_{gs4} - V_{th}) \tag{12}$$

where g_m is the trans-conductance of the MOSFET, and V_{th} is the threshold voltage of the MOSFET.

The gate driving current is used to discharge C_{gs4} while V_{gs4} decreases. It should be noticed that the driving current is used to charge C_{gd4} while V_{gd4} simultaneously changes. V_{gs4} can be expressed as:

$$V_{gs4}(t) = V_{miller} - \int_{t_b}^{t}\frac{I_{dri} - C_{gd}\frac{dV_{ds4}}{dt}}{C_{gs}}dt \tag{13}$$

where V_{miller} is the voltage amplitude of the miller plateau, I_{dri} is the driving current, and C_{gd} is the parasitic capacitance across the gate-to-drain.

Substitute (9) into (8):

$$I_{c4} = g_m(V_{miller} - \int_{t_b}^{t}\frac{I_{dri} - C_{gd}\frac{dV_{ds4}}{dt}}{C_{gs}}dt - V_{th}) \tag{14}$$

Then substitute (9), (10) and (14) into (8), and it can be deduced that:

$$IP_{t1} = g_m(V_{miller} - \int_{t_b}^{t}\frac{I_{dri} - C_{gd}\frac{dV_{ds4}}{dt}}{C_{gs}}dt - V_{th}) + 2C_{ds4}\frac{dV_{ds4}}{dt} \tag{15}$$

V_{ds} can be deduced from (14):

$$V_{ds4}(t) = \frac{I_{dri}}{C_{gd}} + C_1 + C_2 e^{-\frac{C_{gd}}{2C_{gs}C_{ds}}t} \tag{16}$$

The constants C_1 and C_2 can be evaluated from the initial conditions. V_{ds4} is equal to V_{in} at t_c and it is equal to zero at t_b.

Meanwhile, since the current through L_{pc1} is equal to the current through Q_4, the changing rate of I_{Lp1} during *stage 1* can be deduced as:

$$\frac{dI_{Lp1}}{dt}=\frac{dI_{d4}}{dt}=\frac{d(I_{c4}+I_{Cds4})}{dt}=\frac{d[g_m(V_{miller}-\int_{t_b}^{t}\frac{I_{dri}-C_{gd}\frac{dV_{ds4}}{dt}}{C_{gs}}dt-V_{th})+C_{ds4}\frac{dV_{ds4}}{dt}]}{dt} \tag{17}$$

Substitute (16) into (17). Then the changing rate of I_{Lp1} can be deduced. However, the result is too complicated and is not shown here.

This stage ends when the voltage of V_{ds4} reaches V_{in}, and the driving current is all applied to discharge C_{gs}.

***Stage 2 (t_c-t_2)*:** When the voltage of V_{ds4} reaches V_{in}, the primary current continues to flow using the switch and body diode of Q_3, which is shown in Fig .5 (c).

Since the driving current is all applied to discharge C_{gs}, (13) can be rewritten as:

$$V_{gs4}(t) = V_{t_c} - \int_{t_c}^{t}\frac{I_{dri}}{C_{gs}}dt \tag{18}$$

Substitute (14) into (8):

$$I_{c4} = g_m(V_{t_c} - \int_{t_c}^{t}\frac{I_{dri}}{C_{gs}}dt - V_{th}) \tag{19}$$

Then substitute (9), (10) and (19) into (8), and it can be deduced that:

$$I_{Lp1} = g_m(V_{t_c} - \int_{t_c}^{t}\frac{I_{dri}}{C_{gs}}dt - V_{th}) \tag{20}$$

Then the change rate of I_{Lp1} during *Stage 2* can be deduced as:

$$\frac{dI_{Lp1}}{dt}=-\frac{I_{dri}}{C_{gs}} \tag{21}$$

Substitute (17) and (21) into (3), and the inductive voltage across the parasitic inductor L_{pc1} can be deduced as:

$$V_{Lp1}=-L_{pc1}\frac{dI_{Lp1}}{dt}=\begin{cases}-L_{pc1}\left(\frac{I_{dri}}{C_{gs}}-\frac{3C_{gd}^{\ 2}}{4C_2C_{gs}C_{ds}^{\ 2}}e^{t}\right), & \cdots\cdots t_b<t<t_c\\ -L_{pc1}\frac{I_{dri}}{C_{gs}}, & \cdots\cdots t_c<t<t_3\end{cases} \tag{22}$$

Since Q_1 is still on, the voltage of the drain node of Q_2 is constant. Thus, the spurious-on voltage of Q_2 can be deduced as [17]:

$$V_{gs2} \approx V_{Lp1}\frac{C_{gs}}{C_{gd}} \tag{23}$$

Mode 3 [Circulating mode，$t>t_2$]

Q_4 is completely turned off and all of the primary current is

flowing through D_3. This is shown in Fig. 5(d).

B. Impact of the Parasitic Elements

According to the above analysis results, the spurious-on voltage is mainly correlated with the value of the parasitic inductors of the power circuit loop. The parasitic inductors of the transistors have a weak influence on the spurious-on voltage. In addition, the current change rate is positively correlated with the current amplitude when the transistor is turned off according to (21). Meanwhile, the primary current reaches its peak value when the transistor in the leading leg is turned off, and the transistor in the leading leg is turned off with a much smaller current when the primary current decreases a lot during the circulating mode. The peak value of the primary current has been deduced in (1). The primary current decreases a lot during the circulating mode due to the dc blocking capacitor, which is widely used in PSFB converters to eliminate the flux density bias [19]. The current decrease during this mode can be expressed as [23]:

$$\Delta I_{Lp1} \approx \frac{V_{cb}}{L_R}(t_4 - t_3) \tag{24}$$

where V_{cb} is the voltage across the dc blocking capacitor. Since the primary current when the transistors of the leading leg are turned off is much smaller, the amplitude of the voltage oscillation is much smaller than the positive voltage when the transistor in the leading leg is turned off. As a result, the spurious turn-on phenomenon is not induced by the turn-off of the transistors in the lagging leg. The turn-off of the transistors in the leading leg leads to crosstalk of the lagging leg and degrades the system efficiency and reliability. Meanwhile the turn-off of the transistors in the lagging leg have a weak effect on the performance of the system.

Actually, the spurious-on voltage of different transistors during different transition intervals are determined by the different parasitic inductors of the power circuit loop. Details of this are shown as follows.

1) Q_4's Turn-Off Procedure: The analysis in Section III-A shows that the spurious turn-on voltage of Q_2, when Q_4 is turned off, is correlated with the parasitic inductor L_{pc1}. During this transition interval, the voltage of the gate-to-source terminals of Q_1 and Q_4 are the superposition of the positive induced voltage and the drive signals. Among them, the positive induce voltage of Q_1 is mainly determined by the parasitic inductor L_{pc3}. Meanwhile the positive induce voltage of Q_4 is mainly determined by the parasitic inductors L_{pc1}, L_{pc2} and L_{s4}. This is shown in Fig. 3.

When Q_1 is still on, the positive induced voltage of Q_2 leads to crosstalk of the lagging leg. The positive induced voltage of Q_1 has no significant influence unless the voltage amplitude exceeds the maximum gate-to-source tolerant voltage. Meanwhile, the positive induced voltage of Q_4 slows down the turn-off procedure of Q_4 and leads to more switching losses.

2) Q_3's Turn-Off Procedure: Similarly, the transition interval of Q_3 induces a positive voltage at the gate-to-source terminals of Q_1, Q_2 and Q_3. Among them, the positive induced voltage of Q_1 is mainly determined by the parasitic inductor L_{pc3}, the positive induce voltage of Q_2 is mainly determined by the parasitic inductor L_{pc1}, and the positive induce voltage of Q_3 is mainly determined by the parasitic inductors L_{pc3}, L_{pc4} and L_{s3}.

When Q_2 is still on, the positive induced voltage of Q_1 leads to crosstalk of the lagging leg. The positive induced voltage of Q_2 has no significant influence unless the voltage amplitude exceeds the maximum gate-to-source tolerant voltage. Meanwhile, the positive induced voltage of Q_3 slows down the turn-off procedure of Q_3 and leads to more switching losses.

3) Q_2's Turn-Off Procedure: The transition interval of Q_2 induces a positive voltage at the gate-to-source terminals of Q_1, Q_2 and Q_4. Among them, the positive induce voltage of Q_1 is mainly determined by the parasitic inductor L_{pc3}, the positive induce voltage of Q_4 is mainly determined by the parasitic inductor L_{pc1}, and the positive induced voltage of Q_2 is mainly determined by the parasitic inductors L_{pc1} and L_{s2}.

When D_3 is forward bias, the positive induced voltage of Q_4 does not lead to crosstalk of the leading leg. Meanwhile, the positive induced voltage of Q_2 slows down the turn-off procedure of Q_2 and leads to more switching losses.

4) Q_1's Turn-Off Procedure: The transition interval of Q_1 induces a positive voltage at the gate-to-source terminals of Q_1, Q_2 and Q_3. Among them, the positive induce voltage of Q_2 is mainly determined by the parasitic inductor L_{pc1}, the positive induce voltage of Q_3 is mainly determined by the parasitic inductor L_{pc3}, and the positive induce voltage of Q_2 is mainly determined by the parasitic inductors L_{pc3} and L_{s1}.

When D_4 is forward bias, the positive induced voltage of Q_3 does not lead to crosstalk of the leading leg. Meanwhile, the positive induced voltage of Q_1 slows down the turn-off procedure of Q_1 and leads to more switching losses.

It should be noticed that all of the above conclusions are based on the assumption that Q_3-Q_4 is the leading leg. A similar analysis can be extended into the operation mode where Q_1-Q_2 is the leading leg.

In conclusion, since ZVS can be achieved in PSFB converters, the positive voltages across the gate-to-source terminals of the transistors are mainly induced by the parasitic inductors of the power circuit loop. The parasitic inductors of the transistors have a weak impact on the crosstalk phenomena. In addition, the specific operation principle of a PSFB converter makes the leading and lagging legs have distinguished differences with respect to the spurious turn-on problem.

C. Design Guidelines

At first, the transformer turns ratio should be selected. It is well known that the primary current is significantly affected by the transformer turns ratio *n* [1]. Since the oscillation amplitude is positively correlated with the peak current of the primary

side, the transformer ratio should be designed while carefully considering the primary RMS current and the duty cycle loss [24]. Moreover, the transformer turns ratio has an effect on the signal analysis. Specifically, the signal analysis is impacted by the transformer turns ratio in two ways, both directly and indirectly. The transformer turns ratio n appears on the expression of the duty-to-output transfer function of G_{vd}. The natural frequency ω_n and the damping ratio ξ can be expressed as [25]:

$$\xi = \frac{\sqrt{\frac{L_o}{C_o}} + \sqrt{\frac{C_o}{L_o}}[(R_{\text{load}} + ESR_{\text{o}})(R_{\text{load}} + R_{\text{eq}} + 4n^2 f_s L_R) - R_{\text{load}}^2]}{2\sqrt{(R_{\text{load}} + ESR_{\text{o}})(R_{\text{load}} + R_{\text{eq}} + 4n^2 f_s L_R)}} \tag{25}$$

$$\omega_n = \frac{1}{\sqrt{L_o C_o}} \sqrt{\frac{R_{\text{load}} + R_{\text{eq}} + 4n^2 f_s L_{\text{R}}}{R_{\text{load}} + ESR_{\text{o}}}} \tag{26}$$

The transformer turns ratio n explicitly appears in equations (25) and (26), which shows the direct impact on the damping ratio and the natural frequency. As a result, the transformer turns ratio directly influences the PSFB signal analysis. The direct impact is also verified by the analysis presented in [26]. Meanwhile, according to (25) and (26), the power loss equivalent resistor R_{eq} also has an impact on the damping ratio and natural frequency, where the power loss equivalent resistor R_{eq} can be expressed as:

$$R_{\text{eq}} = \frac{P_{\text{loss}}}{I_{\text{out}}^2} \tag{27}$$

P_{loss} is the power loss in a PSFB converter. Meanwhile, the selection of the transformer turns ratio has a significant influence on the overall efficiency of the PSFB converter [27], [28]. Specifically, a smaller turns ratio means a wider output voltage range. However, the conducting loss and the circulating period of the primary side increase with a smaller transformer turns ratio, which leads to more power loss and lower efficiency. Therefore, the selection of the transformer turns ratio has an effect on the efficiency of PSFB converters, and in turn indirectly impacts the signal analysis.

After that, in order to suppress the detrimental effects brought on by the positive induced voltage, several design guidelines can be given as follows according to the above analysis.

(1) Optimizing the PCB layout and minimizing the parasitic inductor in the power circuit loop. According to Sections III-A and III-B, the parasitic inductors L_{pc1} and L_{pc3} have a significant influence on the positive induced voltages. Therefore, it is important to optimize the PCB layout and reduce the copper line length of L_{pc1} and L_{pc3}. Meanwhile, the parasitic inductors L_{pc2} and L_{pc4} do not impact the crosstalk phenomena. Only the turn-off loss of Q_3 and Q_4 are influenced by the two parasitic inductors.

(2) The choice of the leading and lagging legs influences the spurious turn-on phenomena. The leading leg is turned off with a larger current than the lagging leg, and the current flows through different parasitic inductors when the control of leading and lagging legs changes. It is preferable to make the Q_1-Q_2 leg, which is closer to the input terminal shown in Fig. 8 of Section IV, the leading leg. Then the turn-off loss is reduced.

(3) Slow down the turn-off rate of the MOSFET, and decrease the current change rate of the current through the parasitic inductors. This can be realized by reducing the driving current I_{dri}. However, power loss occurs at the transition interval when the voltage and current are overlaid. Therefore, the turn-off rate should be as fast as possible in consideration of the power loss. A tradeoff should been made.

IV. Experimental Verification

In order to verify the above analysis and calculations, a 1.5 kW prototype with the PSFB topology is built. A STM32F051 microcontroller from ST Microelectronics is used to provide the PWM driving signals for the MOSFETs of the phase-shifted full-bridge converter. A microcontroller is chosen since this provides a convenient method for adjusting the switching frequency easily without the need to change the component values. More importantly, with the digital control method, it is very convenient to change the Q_1-Q_2 leg to be the leading or the lagging leg without modifying the layout. All of these are important factors for the experimental verifications carried out below. The simplified digital control scheme for the phase-shifted full-bridge converter in this paper is shown in Fig. 6.

As shown in Fig. 6, a voltage control loop is used to regulate the output voltage V_{o} of the PSFB converter. The output voltage is conditioned and sensed by a feedback network, which is made up of the resistors divider (1:100) and the operational amplifier. Then it is converted by the analog-to-digital converter in the STM32F051. After that, the voltage error e[k] between the output voltage V_{o}[k] and its reference voltage V_{REF} is fed to the digital PI controller. At last, the phase-shift modulator is used to adjust the phase-shift angle and to generate the gate driver signals. Specifically, the gate driver PWM signals are generated from the timer in the STM32F051. Thus, the phase-shift angle and the frequency of the switching signals can be controlled by modified the configuration of the timer.

The phase-shifted full-bridge prototype (1.5 kW) is shown in Fig. 7. The dimensions of the power board are also shown in this figure. The parasitic inductances introduced by the copper lines are mainly determined by the length and width of the copper lines, while the thickness of the copper lines has very little effect on the value of these inductors [30]. Thus, the dimensions of the copper interconnections that could cause this phenomenon are presented in Fig. 8. The irrelevant components are not shown. In order to make the dimensions more clear, they are listed in Table I.

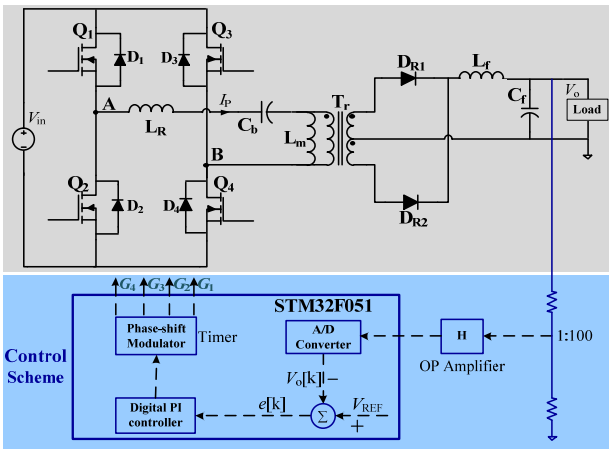


Fig. 6. Control scheme of the phase-shifted full-bridge converter.

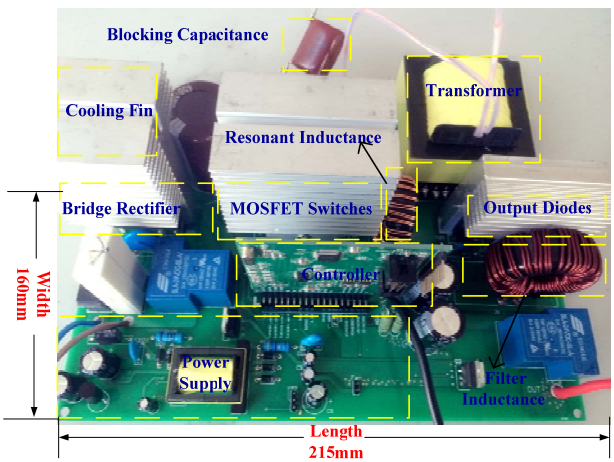


Fig. 7. Physical aspect of the PSFB Prototype.

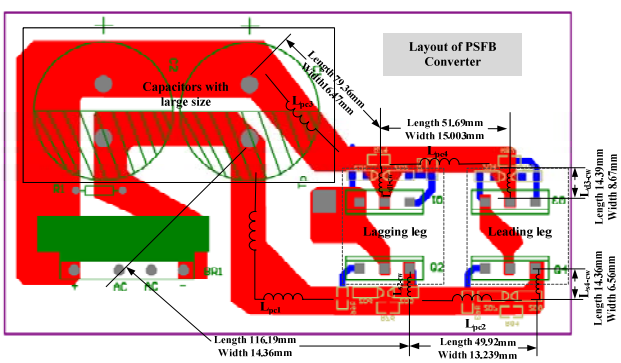


Fig. 8. Dimensions of the copper interconnect in the converter.

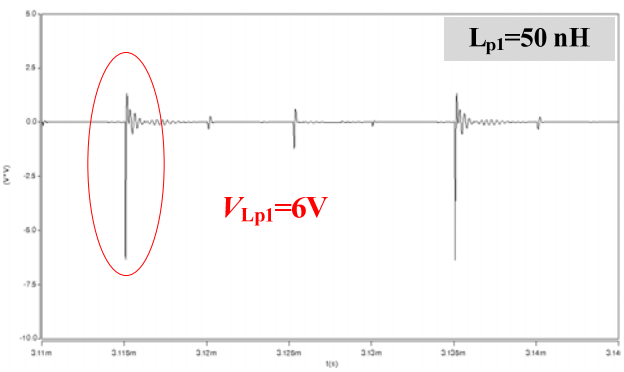
The main parameters of the prototype are listed in Table II. The maximum gate-to-source voltage of the transistor is 30V, and the minimum gate threshold voltage is 3V. The input capacitance C_{iss} is 5870 pF, the output capacitance C_{oss} is 530 pF and the reverse transfer capacitance C_{rss} is 54 pF when V_{GS}=0 and V_{DS}=25 V [29]. First, simulation results of the voltage across the source node and the power ground, V_{Lp1}, when Q_4 is switched off, are shown in Fig. 9. Simulation results with various values of the parasitic inductor L_{pc1} are shown in Fig. 9(a) and (b). It has been found that the oscillation

TABLE I
DETAILED CHARACTERIZATION OF THE DIMENSIONS OF THE COPPER LINE

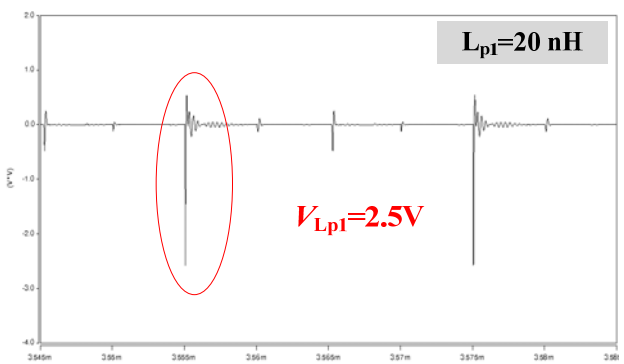
Parameters	Dimensions	
	Length (mm)	Width (mm)
Power board	215.646	159.385
L_{pc1}	116.19	14.360
L_{pc2}	49.921	13.329
L_{pc3}	79.362	16.470
L_{pc4}	51.691	15.003
$L_{s2\text{-}cw}$	13.963	5.130
$L_{s4\text{-}cw}$	14.362	6.561
$L_{d1\text{-}cw}$	14.413	9.793
$L_{d3\text{-}cw}$	14.391	8.673

TABLE II
MAIN PARAMETERS OF THE PSFB PROTOTYPE

Parameter	Value
Input DC Voltage	260~380 Vdc
Output DC Voltage	60~100 Vdc
Maximum Output Current	15 A
Maximum Output Power	1.5 kW
Switching Frequency	40 kHz
Turn Ratio of the Transformer	20:9
Resonant Inductor	57 μH
Bobbin of the Transformer	EE55
Magnetic Inductor	1.8 mH
MOSFET	IRFPS30N60K



(a) Larger parasitic inductance (L_{p1}=50 nH).



(b) Smaller parasitic inductance (L_{p1}=20 nH).

Fig. 9. Induced voltage across the parasitic inductor with different inductor values.

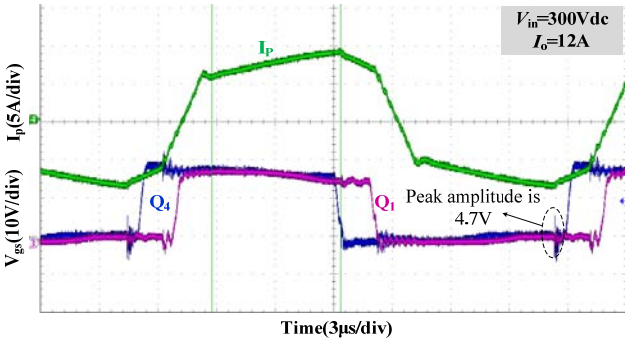


Fig. 10. Operational waveforms with Q_3-Q_4 as the leading leg.

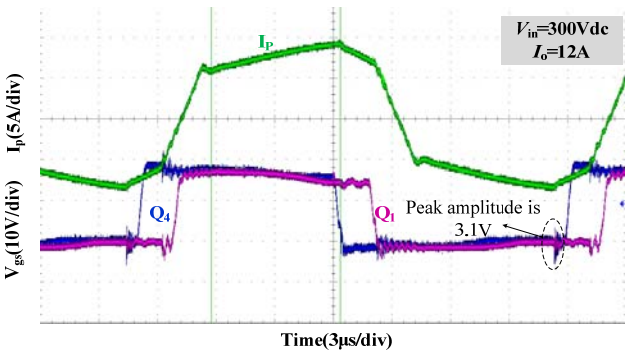


Fig. 11. Operational waveforms with small L_{pc3}.

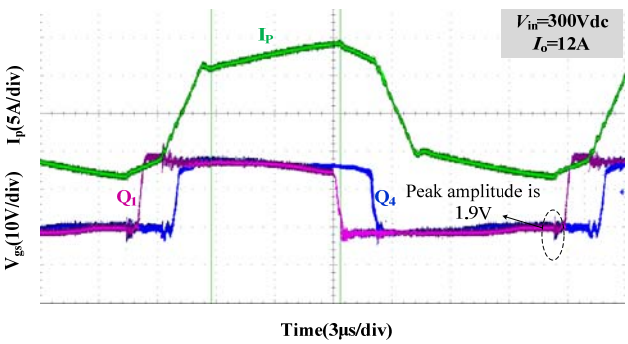


Fig. 12. Operational waveforms with Q_1-Q_2 as the leading leg.

amplitude decreases with a smaller L_{pc1}.

In order to verify the analysis in Section III, several tests are built separately. First, the Q_3-Q_4 leg is controlled as the leading leg as shown in Fig. 8. Basic operation waveforms and gate-to-source waveforms of the PSFB converter are shown in Fig. 10.

A. Minimized the Parasitic Inductor L_{pc3}

According to the above analysis, the spurious turn-on voltage of Q_1 is positively correlated with the value of the parasitic inductor L_{pc3}. The parasitic inductor is introduced by the copper line on the printed circuit board.

Therefore, in order to shorten the length between the source node and the power ground, a short-thick line is used to shorten the two points. Test results are shown in Fig. 11.

According to the formula presented in [30], the parasitic inductor L_{pc3} is reduced from about 47 nH to 31.7 nH. As a result, the positive induced voltage of Q_1 is suppressed when Q_3 is turned off. However, the effect is not very significant since the existing copper line is not very long when compared to the short line.

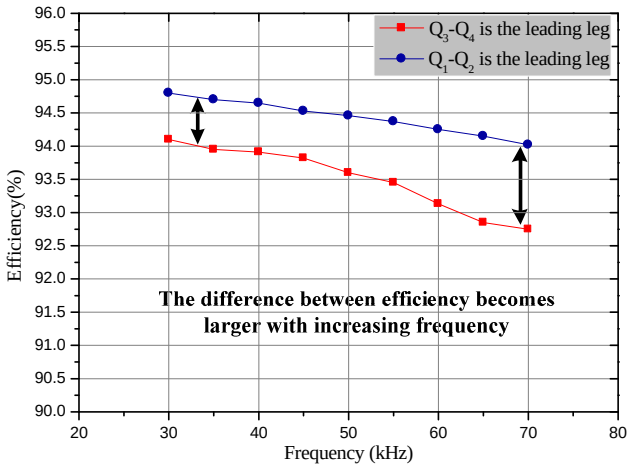


Fig. 13. Efficiency comparison with different leading leg.

TABLE III
SUMMARY OF CONVERTERS CHARACTERISTICS

Topology	Efficiency	Voltage Stress	Current Stress	Circuit Complexity
CPSFB Converter	Normal	Normal	Normal	Normal
Proposed Converter	Higher	Normal	Normal	Normal
Converter in [7]	Higher	Normal	Higher	Higher
Converter in [8]	Highest	Normal	Highest	Highest

B. Changing the Q_1-Q_2 Leg as the Leading Leg

The Q_1-Q_2 leg is controlled as the leading leg. Experimental waveforms are shown in Fig. 12. According to Fig. 12, the peak amplitude of the induced positive voltage of Q_4 in the lagging leg is sharply reduced.

The efficiency is improved correspondingly. In order to verify the effect, the overall efficiency is tested with different switching frequency using the Q_1-Q_2 leg and the Q_3-Q_4 leg as leading legs separately. Test results are shown in Fig. 13. The efficiency increased with the Q_1-Q_2 leg as the leading leg. Meanwhile, the difference between the efficiencies becomes more and more evident when the switching frequency increases.

The comparison results between the PSFB converter proposed in this paper, the conventional PSFB converter (CPSFB) and the latest novel PSFB converters proposed in [7], [8] can be summarized in Table III. The proposed PSFB converter can achieve a relatively high efficiency without additional auxiliary components. In addition, the control scheme of this converter is easy to implement. Moreover, the voltage and current stresses are low when compared to the

other existing high-efficiency PSFB converters.

V. CONCLUSION

The PSFB converter is a widespread preferred topology for isolated dc-dc power conversion in medium to high power applications. The spurious turn-on phenomena have been observed in PSFB converters which lead to additional switching losses and overstress of the power devices. By taking into account the parasitic inductors of the power circuit loop and the transistors in the PSFB converter, the spurious turn-on phenomena are thoroughly analysed considering the special operation principle of this topology. It has been found that this phenomenon is mainly induced by the parasitic inductors of the power circuit loop. The parasitic inductors of the transistors have a weak impact on the crosstalk phenomena. In addition, the specific operation principle of the PSFB converter makes the leading and lagging legs have distinguished differences with respect to the spurious turn-on problem.

Based on this analysis, several design guidelines are presented. Detailed simulation and experimental results obtained from a 1.5 kW PSFB converter are given to verify the above theoretical analysis. The positive induced voltage can be reduced with the proposed method and the efficiency can be improved.

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