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A Novel PCCM Voltage-Fed Single-Stage Power Factor Correction Full-Bridge Battery Charger

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Abstract

A novel pseudo-continuous conduction mode (PCCM) voltage-fed single-stage power factor correction (PFC) full-bridge battery charger is proposed in this paper. By connecting a freewheeling transistor in parallel with an input inductor, the PFC cell can operate in the PCCM with a constant duty ratio. Thus, the dc/dc stage can be designed using this constant duty ratio and the restriction on the duty ratio of the PFC cell is eliminated. As a result, the input current distortion is less and the dc bus voltage becomes controllable over the wide output power range of the battery charger. Moreover, the operation principle of the dc/dc stage is designed to be similar to that of a conventional phase-shifted full-bridge converter. Therefore, it is easy to implement. In this paper, the operation of the new converter is explained, and the design considerations of the controller and key parameters are presented. Simulation and experimental results obtained from a 1 kW prototype are given to confirm the operation of the proposed converter.

Key words: Battery charger, Full-bridge, Power factor correction, Single-stage

I. INTRODUCTION

In recent years, battery chargers have become a key component for the emergence and acceptance of electrical vehicles. A well-known topology for battery chargers is the two-stage structure. A front stage, which is usually a boost converter, is adopted to perform power factor correction (PFC). A second stage, which is usually a high-efficiency isolated dc/dc converter, is adopted to realize isolation and to control the charging current. Normally, a full-bridge (FB) converter is the most popular topology for the dc/dc converter in battery charger applications (1-5 kW) [1]-[5].

However, the cost and complexity of the overall two-stage converter are increased because an additional converter must be implemented. Therefore, using a single-stage topology to realize the PFC, isolation and dc/dc conversion sounds more attractive. Several single-stage full-bridge topologies can be found in the literature [6]-[21]. Among them, voltage-fed full-bridge converters [13]-[21], which can operate with a constant frequency and do not have a voltage overshoot problem across the dc bus, have been widely studied. In [13]-[20], two inherent duty ratios, the dc/dc stage duty ratio D_o and the PFC cell duty ratio D_i, are defined. However, D_i is restricted by D_o, and there are only three discontinuous values of D_i when D_o is settled. Therefore, distortions of input current are high and the dc bus voltage may become uncontrollable, especially in battery charger applications where the output power varies a lot. In [21], the restriction of the PFC cell duty ratio is weakened by using two controllers, and the PFC cell duty ratio can vary continuously. Nevertheless, the range of D_i should still be limited to implement the control of the output voltage. Thus, input current distortions inevitably appear due to the limited duty ratio band. In addition, two controllers increase the system complexity.

In this paper, a novel pseudo-continuous conduction mode (PCCM) voltage-fed single-stage full-bridge battery charger topology is proposed. The proposed converter can operate with a constant frequency, less input current distortion and a controllable dc bus voltage. These features are realized by using PCCM control in the PFC cell. It is well known that discontinuous conduction mode (DCM) PFC converters suffer from heavy current stresses, which restrict the power range of DCM PFC converters to the low power range (<250W) [22]. Therefore, the continuous conduction mode (CCM) is the most

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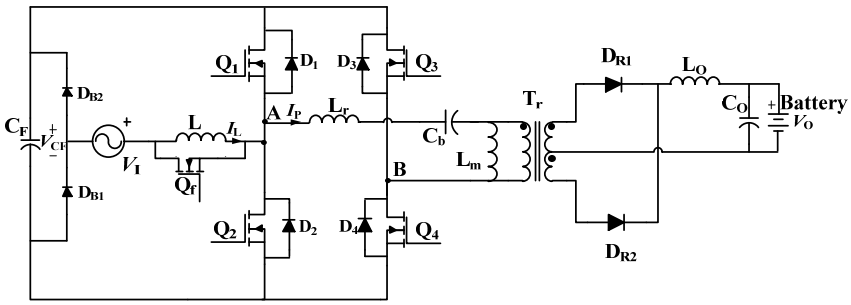


Fig. 1. Proposed PCCM single-stage PFC full-bridge converter for battery charger.

popular modulation method in large power applications such as battery chargers. However, the duty ratio of CCM PFC varies a lot over one ac line cycle which limits the regulation range of the output voltage, as is shown in [21]. In this paper, PCCM control, which can be used to achieve a large output power while having a constant on-time, is adopted here. With a constant on-time, the restriction of the input duty ratio can be eliminated. In addition, the operation of the dc/dc stage is designed to be similar to that of the conventional phase-shifted full-bridge (PSFB) converter which makes it easy to implement.

This paper is organized as follows. The operation of the proposed converter is explained in Section II. The converter characteristics are presented in Section III. Then the design procedure of the proposed battery charger is proposed in Section IV. In Section V, simulation and experimental results obtained from a 1kW single-stage battery charger prototype are given to confirm the operation of the proposed converter. Finally, some conclusions are given in section VI.

II. Converter Description and Operation Principle

A circuit diagram of the proposed single-stage full-bridge converter is shown in Fig. 1. The two bridge legs of the full-bridge converter are composed of four transistors, Q_1, Q_2, Q_3 and Q_4. Q_1 and Q_2 are used to perform the same current-shaping function as the switch in a boost converter. The input inductor L is connected to the Q_1–Q_2 leg. The power transformer T_r, the resonant inductor L_r (including the leakage inductor), the output diodes D_{R1} and D_{R2}, the output filter inductor L_O and the capacitor C_O make up a standard full-bridge converter. An energy storage capacitor C_F is placed across the primary-side dc bus. The freewheeling power switch Q_f is placed in parallel with the input inductor L.

The PFC function can be accomplished by two input boost converters (*Boost-1*, when V_I <0; and *Boost-2*, when V_I >0), as shown in Fig. 2. The operations of the two boost converters *Boost-2* (V_I >0) as an example.

Key waveforms of the proposed converter are shown in Fig. 3. d_a is the duty ratio of Q_2, which is the PFC cell duty ratio, and the inductor current I_L ramps up in the time interval d_aT. With the PCCM control, d_a is nearly constant over half a line

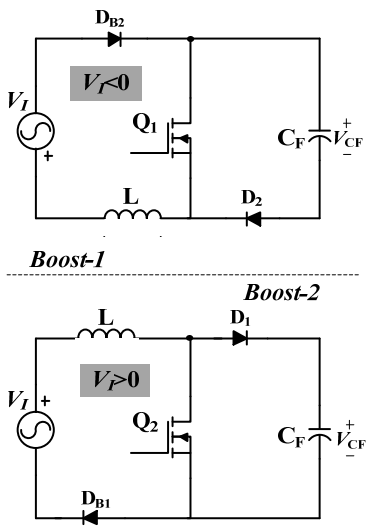


Fig. 2. Two input boost converters provided by the proposed topology.

are symmetric. Thus, the operation explanation below takes cycle (typical 100 Hz), and V_{CF} is regulated to be constant. Obviously, V_{CF} is larger than V_I. Meanwhile, the operation principle of the dc/dc stage (charging current control stage) is similar to that of the PSFB converter. The duty ratio of Q_4 is equal to that of Q_2, which is nearly constant. Meanwhile, the gating signals for Q_1 and Q_3 are complimentary to those for Q_2 and Q_4, respectively. Whenever the top switch of a converter leg is on, the bottom switch in the same leg is off and vice versa. The charge current is controlled by phase-shifting the gating signals of the switches in the Q_1–Q_2 leg with respect to those of the Q_3–Q_4 leg. φ is the phase difference between the two legs. Although the transformer primary voltage's positive and negative halves are asymmetrically placed, the voltage-second balance can be achieved. In addition, the time interval d_bT represents the period when the input inductor current I_L ramps down and the capacitor C_F is charged. This happens when both Q_2 and Q_f are off. d_cT is the time interval when the switch Q_2 is off, and Q_f is on. In this interval, the input inductor current is in the freewheeling mode and is kept constant. It should be noted that:

$$d_a + d_b + d_c = 1 \tag{1}$$

Equivalent circuit diagrams of the operation modes that the converter goes through during a switching cycle are shown in

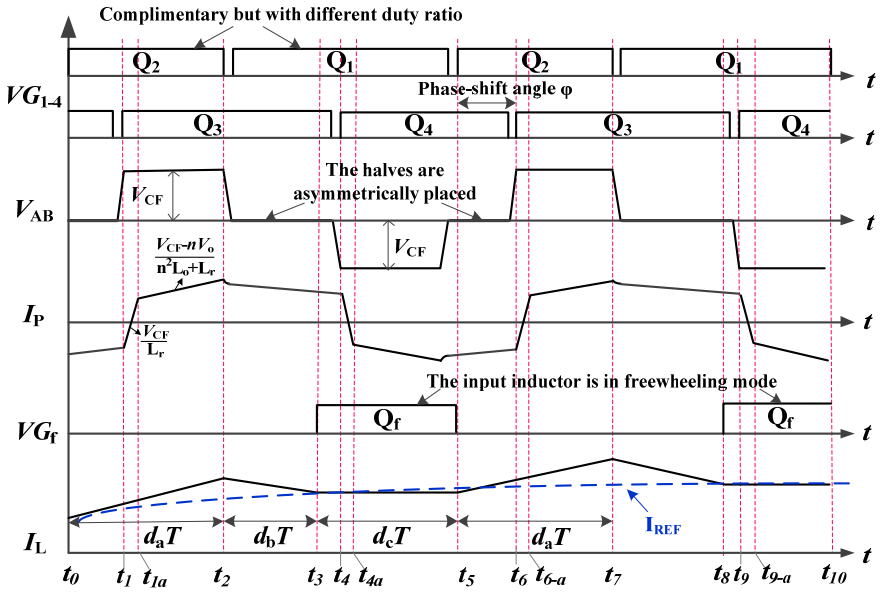


Fig. 3. Key waveforms of the proposed converter.

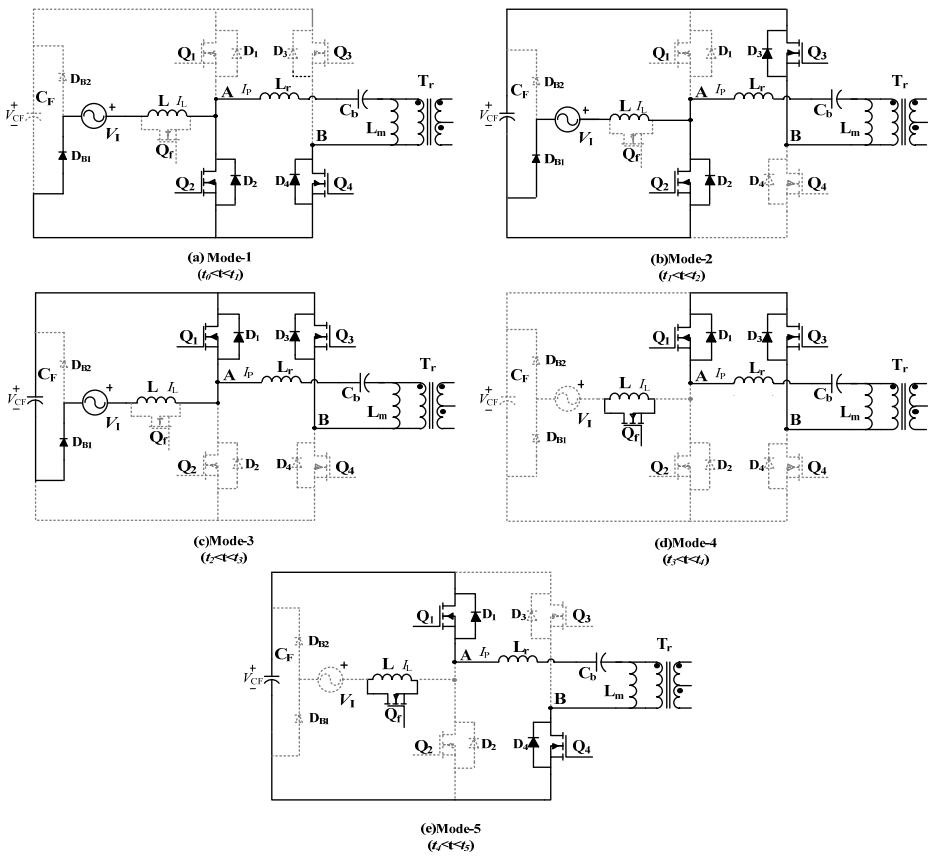


Fig. 4. Equivalent circuits of the proposed converter in different modes.

Fig. 4. Since the operation principle of the dc-dc stage is similar to that of the conventional PSFB converter, the output stage, dead-time and duty cycle loss have been neglected here for the sake of simplicity.

The details of each operation mode are described as follows: *Mode 1*(t_0<t<t_1): This mode begins when Q_2 is switched on. During this mode, Q_2 and Q_4 are on. The primary voltage V_{AB} is equal to zero, and the current through the resonant inductor decreases. The transformer primary current during this mode is given by:

$$I_p(t) = I_p(t_0) - \frac{nV_o}{n^2L_o + L_r}(t - t_0) \tag{2}$$

where n is the turns ratio of the transformer and V_o is the

battery voltage. No energy has been transferred to the load from C_F in this period.

Meanwhile, since Q_2 and D_{B1} are on, the input voltage remains impressed across the input inductor L and its current ramps up. The current through the input inductor can be expressed as:

$$I_L(t) = I_{REF}(t_p) + \frac{|V_m \sin \omega t|}{L}(t - t_0) \quad (3)$$

where V_m is the peak input voltage. $I_{REF}(t_p)$ represents the reference of the input current in the previous switching cycle. This is because the inductor current I_L reaches the reference current I_{REF} when Q_f is turned on and I_L remains constant during d_cT.

This mode ends when Q_4 is turned off and Q_3 is turned on. It should be noted that the dead-time is neglected here and the ZVS turn-on of the transistors is achieved in the dead-time.

Mode 2($t_1<t<t_2$): This mode begins when Q_3 is switched on. Actually, two modes are included during this interval. They are the commutation mode and the energy transfer mode. Since the two modes share the same equivalent circuit, as shown in Fig. 4(b), and the commutation mode is relatively short compared with the other modes, the two modes are analyzed together in this section. The commutation mode is the time interval [$t_1<t<t_{1a}$], as shown in Fig. 3. This interval is known as the duty cycle loss in the standard PSFB converters. During this interval, the dc bus voltage is completely impressed on the resonant inductor L_r and the primary current starts to commutate with a finite slope.

$$I_p(t) = I_p(t_1) + \frac{V_{CF}}{L_r}(t - t_1) \quad (4)$$

At t_{1a}, the commutation of the primary current is finished, and the energy transfer mode begins. The energy is transferred from the dc bus to the output through the transformer. The positive voltage of V_{CF} is impressed across the series combination of the leakage inductor and the equivalent output inductor reflected on the primary side. It should be noted that the magnetizing inductance L_m is much larger than the output filter inductance L_o and is neglected here [21]. Thus, the current in the transformer primary and the output inductor L_o rise during this mode. The transformer primary current can be given by:

$$I_p(t) = I_p(t_{1a}) + \frac{V_{CF} - nV_o}{n^2 L_o + L_r}(t - t_{1a}) \quad (5)$$

Meanwhile, a positive input voltage continues to be impressed across the input inductor L in *Mode 2*, and its current can be expressed as:

$$I_L(t) = I_L(t_1) + \frac{|V_m \sin \omega t|}{L}(t - t_1) \quad (6)$$

At the end of this mode, Q_2 is turned off.

Mode 3($t_2<t<t_3$): This mode begins when Q_2 is switched off and Q_1 is switched on. When Q_2 is turned off, the energy-transfer mode ends and the primary current freewheels through Q_1 and Q_3. The transformer primary current during this mode is given by:

$$I_p(t) = I_p(t_2) - \frac{nV_o}{n^2 L_o + L_r}(t - t_2) \quad (7)$$

Meanwhile, this is the capacitor-charging mode (d_bT interval). C_F is charged in this interval from the energy stored in L. The voltage across the input inductor L can be given by:

$$V_L = |V_m \sin \omega t| - V_{CF} \quad (8)$$

In addition, V_{CF} is controlled to be larger than V_m. Therefore, the input inductor current starts to ramp down and can be expressed as:

$$I_L(t) = I_L(t_2) - \frac{V_{CF} - |V_m \sin \omega t|}{L}(t - t_2) \quad (9)$$

This mode ends when the input inductor current reaches the reference current, which means that:

$$I_L(t_3) = I_{REF}(t_3) \quad (10)$$

At $t = t_3$, the freewheeling power switch Q_f is turned on and the next mode begins.

Mode 4($t_3<t<t_4$): This mode begins when Q_f is switched on. The primary current freewheels through Q_1 and Q_3. The transformer primary current during this mode is given by:

$$I_p(t) = I_p(t_3) - \frac{V_{Cb}}{L_r}(t - t_3) \quad (11)$$

When Q_f is switched on, the voltage across the input inductor is approximately equal to zero. Thus, D_{B1} is reverse biased, and the voltage across D_{B1} is (V_{CF}-V_I). Meanwhile, the current through the input inductor does not change.

$$I_L(t) = I_{REF}(t_3) \quad (12)$$

At the end of this mode, Q_4 is turned on and Q_3 is turned off.

Mode 5($t_4<t<t_5$): This mode begins when Q_4 is switched on. The commutation mode is the time interval [$t_4<t<t_{4a}$] shown in Fig. 3. During this interval, the dc bus voltage is completely impressed on the resonant inductor L_r and the primary current starts to commutate with a finite slope.

$$I_p(t) = I_p(t_4) + \frac{V_{CF}}{L_r}(t - t_4) \quad (13)$$

At t_{4a}, the commutation of the primary current is finished, and the energy transfer mode begins. The energy is transferred from the dc bus to the output through the transformer. The positive voltage of V_{CF} is impressed across the series combination of the leakage inductor and the equivalent output inductor reflected on the primary side. Thus, the current in the transformer primary and the output inductor L_o rises during this mode. The transformer primary current can be given by:

$$I_p(t) = I_p(t_{4a}) + \frac{V_{CF} - nV_o}{n^2 L_o + L_r}(t - t_{4a}) \quad (14)$$

Meanwhile, a positive input voltage continues to be impressed across the input inductor L in *Mode 5*, and its

current can be expressed as:

$$I_L(t) = I_L(t_4) + \frac{|V_m \sin \omega t|}{L}(t - t_4) \qquad (15)$$

This mode ends when Q_2 is turned on and another switching sequence begins.

III. Features of the Proposed Converter

The PCCM converter inherits some characteristics of CCM and DCM operations. They can be illustrated as follows.

Like CCM converters, the PCCM converter has a low inductor current ripple. This is because, according to the operation principle presented in Section II, the inductor current I_L is reset to I_{REF} instead of zero in every switching cycle. Meanwhile, the PCCM converter can deliver a larger power by simply boosting the current level of I_{REF}. In addition, the ratio d_a/d_b, is almost constant when the output power changes. This is determined by the input and output voltage.

Like DCM converters, the on-time of power the MOSFETs in PCCM converters can be designed to be constant over half of the line cycle. This is realized by introducing a freewheeling period d_cT. The design and implementation of the dc-dc stage is very simple when the duty ratio of the PFC cell d_a is constant. In addition, the output power varies with the duty ratio d_a. Actually, d_a can be nearly constant over the entire power range with the control method proposed in Section IV. In addition, the output power is mainly regulated by modulating I_{REF}.

Since the duty ratio of the PFC cell is constant, when compared to other voltage-fed single-stage full-bridge converters, the proposed converter has the following attractive features.

1) There is no restriction of the PFC cell duty ratio which is used to shape the input current in the proposed converter. d_a is nearly constant in the proposed PCCM converter. Therefore, with proper design of the controller and turns ratio of the transformer, the output voltage (or charging current) can be modulated without inducing input current distortions or an uncontrollable dc bus voltage, which are common problems in previous studies.

2) The turns ratio of the transformer in the proposed converter can be designed so that it is larger than that of the other voltage-fed single-stage full-bridge converters. Since the duty ratio d_a in the proposed converter is nearly constant, the turns ratio can be designed to be as large as possible. Meanwhile, in other voltage-fed single-stage converters, in order to achieve a high PF, the PFC cell duty ratio band must be designed wide enough, which means the turns ratio should be designed considering the minimum duty ratio in a wide scope. Therefore, the circulating loss can be reduced in the proposed converter.

3) The operation principle of the dc-dc conversion stage is similar to that of a standard phase-shift full-bridge converter.

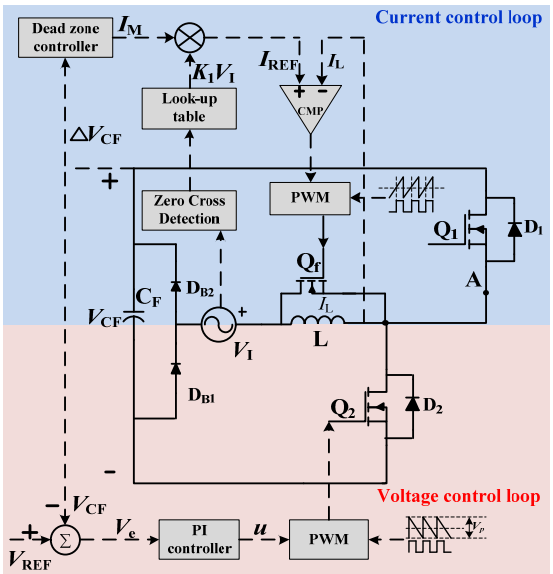


Fig. 5. PFC controller in the proposed converter.

Therefore, it is easy to implement. In addition, the output diodes can be replaced with synchronous rectifier MOSFETs for high output current applications. This is very difficult for converters that operate with non-standard control methods.

4) Single-ended transformer coupled gate driver circuits [23] can be used as the MOSFET gate driver for the proposed converter. Meanwhile, in other voltage-fed single-stage full-bridge converters, the asymmetric driver signals, which vary over every switching cycle, cause saturation of the pulse-transformer. Driver ICs had to be used in [13]-[21]. The driver ICs, especially ones that can provide isolation [24], are much more expensive than the isolated single-ended transformer-based topology.

IV. Design Considerations

A. PFC Controller Design

Fig. 5 shows a schematic of the controller of a PFC cell. Irrelevant components are neglected for the sake of simplicity. A voltage control loop is used to regulate the voltage across the dc bus (V_{CF}). A current control loop is used to control the reference current to make the inductor current in the same wave shape as and in phase with the input voltage to achieve unity power factor. Also In addition, the power delivered by the converter can be regulated by the current control loop. Unlike the conventional average current controller of a CCM boost PFC converter, the output of the voltage control loop is no longer the input of the current control loop. Therefore, the voltage loop and the current loop can be designed separately.

In the voltage control loop, the voltage error V_e between the dc bus voltage V_{CF} and its reference voltage V_{REF} are fed back to generate the gating signal of Q_2 or Q_1. The bandwidth of the voltage control loop is designed to be very narrow. As a result, d_a changes slowly and is thought to be constant over a half line cycle. According to (3) and (6), the peak inductor current can

be given as:

$$I_L(t) = I_{REF}(t_p) + \frac{|V_m \sin \omega t|}{L} d_a T \tag{16}$$

where the line voltage and reference current are sinusoidal, and d_aT and the input inductor L are constant. Thus, the peak inductor current $I_L(t)$ naturally follows the sinusoidal line-voltage waveform.

A triangle-trailing-edge modulation, as seen in Fig. 5, is adopted for Q_2.

In the current control loop, a reference current I_{REF} is produced by multiplying the input voltage k_1V_1 by the desired current amplitude I_M.

$$I_{REF} = k_1 I_M V_m \sin \omega t \tag{17}$$

where k_1 is a coefficient produced by the controller, and $k_1V_m \approx 1$. Thus:

$$I_{REF} \approx I_M \sin \omega t \tag{18}$$

The input voltage V_1 is implemented by a look-up table with the sensing of the zero cross signal.

The key issue of the current control loop is to obtain I_M. As mentioned in Section III, the output power is mainly regulated by modulating I_{REF}. Thus, I_M should be proportional to the load current of the PFC section I_{bus} (which is proportional to the load power since the dc bus voltage is constant). Equation (18) can be rewritten as:

$$I_{REF} \approx k I_{bus} \sin \omega t \tag{19}$$

In order to obtain the desired reference current without sampling the load current I_{bus}, a dead-zone controller, which was proposed in [25]-[26], is used in this paper. The voltage ripple across C_F is sensed here, since the difference between the instantaneous input power and the constant output power produces a voltage ripple $\Delta V_{CF}(t)$ at twice the line frequency. The voltage ripple can be expressed as:

$$\Delta V_{CF}(t) \approx \frac{I_{bus} \sin(4\pi f_{line} t)}{4\pi f_{line} C_F} \tag{20}$$

From (20), it can be seen that the load current I_{bus} is directly proportional to the ripple voltage. In the dead-zone controller, the sampled frequency of the output voltage is f_a, and f_a is significantly higher than the line frequency. The sampled voltage is then used to calculate the output voltage ripple magnitude $\Delta V_{CF}[n]$, which is compared with several preset digital dead-zone reference levels to give the corresponding predefined I_M.

In order to ensure that the converter operate in the PCCM, which requires $d_c>0$, and based on the power conservation of the converter, the following equation should be satisfied:

$$\frac{V_m}{\sqrt{2}} \frac{I_M}{\sqrt{2}} > V_{bus} I_{bus} \tag{21}$$

Thus, based on (18) and (19), the predefined I_M can be determined as:

$$I_M > \frac{8\pi f_{line} C_F V_{bus} \Delta V_{CF}}{V_m} \tag{22}$$

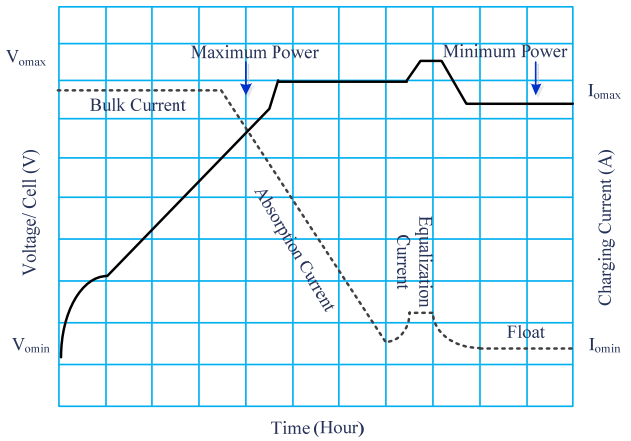


Fig. 6. Simplified adaptive four-step lead-acid battery charging profile.

According to the sensed ripple voltage, one of the predefined values of I_M will be used. If the dead-zone controller senses a higher voltage ripple, a higher level of I_M is chosen. Meanwhile, in order to minimize the power loss caused by Q_f, the controller limits the minimum turn-on time of Q_f to be less than 5% of the switching period. This is achieved by slightly adjusting k_1. Therefore, d_a is almost constant over the entire power range as the ratio d_a/d_b does not change when the output power changes. The output power is mainly regulated by modulating I_{REF}.

B. Design of the Input Inductor L

The inductor-current ripple of the PCCM operation is much smaller than the DCM operation and larger than the CCM operation. Thus, a medium inductor is needed in the PCCM operation. According to [22], the minimum value of the input inductor for the CCM operation and the maximum value for the DCM operation can be derived as:

$$L_{CCM} > \frac{T}{2G_e(P_{o-\min})} \tag{23}$$

$$L_{DCM} < \frac{T}{2G_e(P_{o-\max})}\left(1 - \frac{V_m}{V_{CF}}\right) \tag{24}$$

where:

$$G_e = \frac{2P_o}{V_m^2} \tag{25}$$

Meanwhile, the power range of a typical four-step battery charger for a 60V system is shown in Fig. 6 [27]. The value of the input inductor L can be selected based on (23), (24), (25) and Fig. 6.

C. Design of the Turns Ratio n

As previously mentioned, the main feature of the proposed converter is that it has no restriction of the PFC cell duty ratio d_a. In addition, d_a is nearly constant over the entire power range. Meanwhile, based on the operation principle presented in Section II, the maximum effective duty ratio for the charging current regulation is determined by d_a. Thus, for designing the turns ratio of the transformer T_r, it is necessary

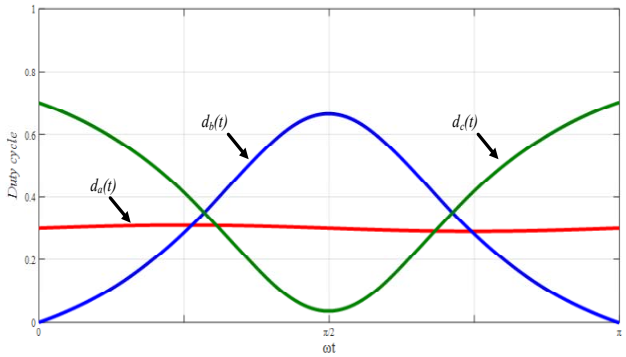


Fig. 7. $d_a(t)$, $d_b(t)$ and $d_c(t)$ during half line cycle.

to get the operating range of d_a.

According to the instantaneous expressions of the input inductor current, the following relation can be obtained:

$$\frac{V_m|\sin\omega t|}{L}d_aT+\frac{V_m|\sin\omega t|-V_{CF}}{L}d_bT=I_{REF}(t+T)-I_{REF}(t) \quad (26)$$

From (19) and (26), the following equation can be deduced:

$$d_b=\frac{V_m|\sin\omega t|}{V_{CF}-V_m|\sin\omega t|}d_a-\frac{kI_{bus}L}{T}\frac{|\sin\omega(t+T)|-|\sin\omega t|}{V_{CF}-V_m|\sin\omega t|} \quad (27)$$

According to the analysis in Section IV-A, the duty ratio d_a is almost constant over one line cycle. In order to make the theoretical analysis more clear, the duty ratios d_a, d_b and d_c over one line cycle can be plotted in a figure. Firstly, based on the assumption that d_a remains constant at 0.3, the duty ratios d_b and d_c can be calculated with (1) and (27). The parameters used for the calculation of $d_b(t)$ in (27) are obtained from the prototype shown in Section V (Table I). Then, the values of $d_a(t)$, $d_b(t)$ and $d_c(t)$ over one half line cycle are plotted in Fig. 7 using Matlab. Actually, the value 0.3 is selected because d_a is almost equals to 0.3 (0.28 in practice) in the prototype proposed in Section V. In addition, the calculated curves of d_b and d_c shown in Fig. 7 are based on the system parameters of the prototype.

In the PCCM operation, it is easy to obtain:

$$d_b+d_a<1 \quad (28)$$

From (27) and (28), the constraint of d_a can be deduced as:

$$d_a<\frac{V_{CF}-V_m|\sin\omega t|}{V_{CF}}+\frac{kI_{bus}L}{T}(|\sin\omega(t+T)|-|\sin\omega t|) \quad (29)$$

Since the switching period T is much smaller than the line period, the following equation can be calculated:

$$|\sin\omega(t+T)|-|\sin\omega t|\approx\omega T\cos\omega t \quad (30)$$

Therefore, (29) can be rewritten as:

$$d_a<1-\frac{V_m|\sin\omega t|}{V_{CF}}+kI_{bus}L\omega|\cos\omega t|=1-\frac{V_m|\sin\omega t|}{V_{CF}}+\frac{kP_oL\omega}{V_{CF}}|\cos\omega t| \quad (31)$$

Since d_a is constant over half a line cycle, (31) should be satisfied over half a line cycle. According to (27), the envelope of $d_b(t)$ shown in Fig. 7 increases with a larger d_a. Meanwhile, d_b varies during half a line cycle and reaches its maximum value at $\omega t=\pi/2$ with a constant d_a. Thus, the available maximum value of d_a can be deduced as:

$$d_{a-\max}=\left[1-\frac{V_m|\sin\omega t|}{V_{CF}}+\frac{kP_oL\omega}{V_{CF}}|\cos\omega t|\right]_{\omega t=\frac{\pi}{2}}=1-\frac{V_m}{V_{CF}} \quad (32)$$

For V_{in}=220Vac, and from (32), it can be concluded that $d_{a\text{-}max}$ is usually smaller than 0.5 because of the limitation of V_{CF}. Thus, the maximum effective duty ratio for dc/dc regulation is equal to $d_{a\text{-}max}$ when the phase difference φ is zero.

Meanwhile, the output filter inductor L_o is designed to work in the CCM mode. Thus, with a constant primary dc bus voltage, the maximum value of the turns ratio n can be deduced considering the maximum effective duty ratio $d_{a\text{-}max}$ and the maximum battery voltage $V_{o\text{-}max}$. The following constraint, based on the standard full-bridge operation, can be placed on n.

$$n<\frac{2d_{a-\max}V_{CF}}{V_{o-\max}} \quad (33)$$

where V_{omax} can be obtained from Fig. 6. From (32) and (33), the following relation can be obtained:

$$n<2\frac{V_{CF}-V_m}{V_{o-\max}} \quad (34)$$

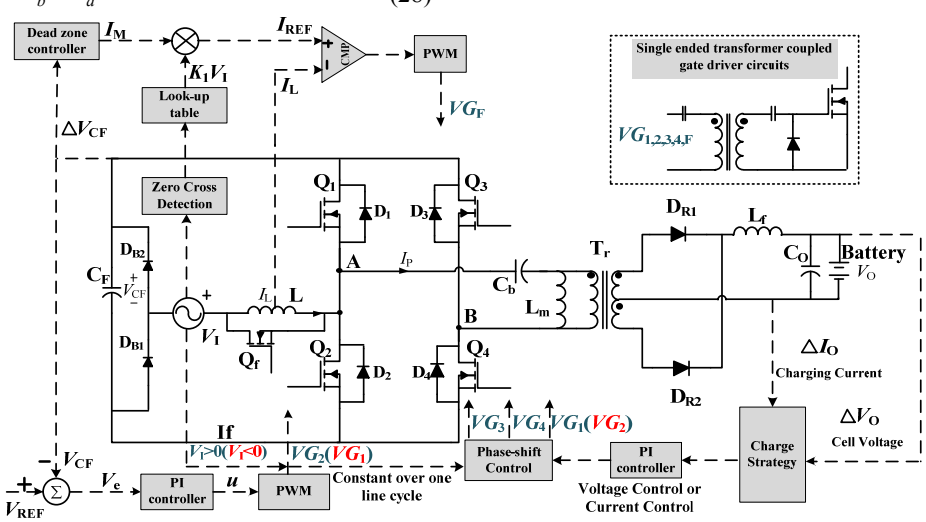


Fig. 8. Simplified schematic of the proposed converter with controllers.

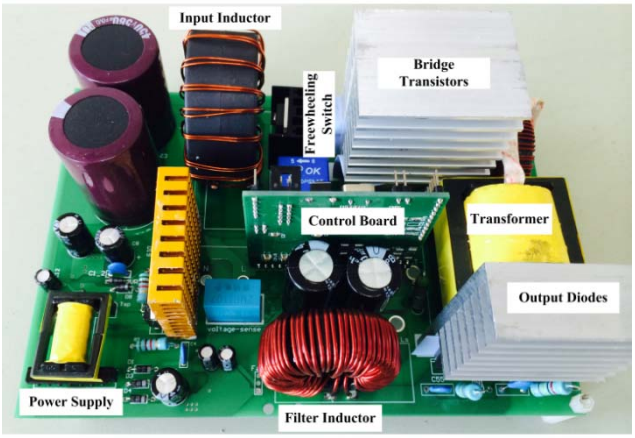
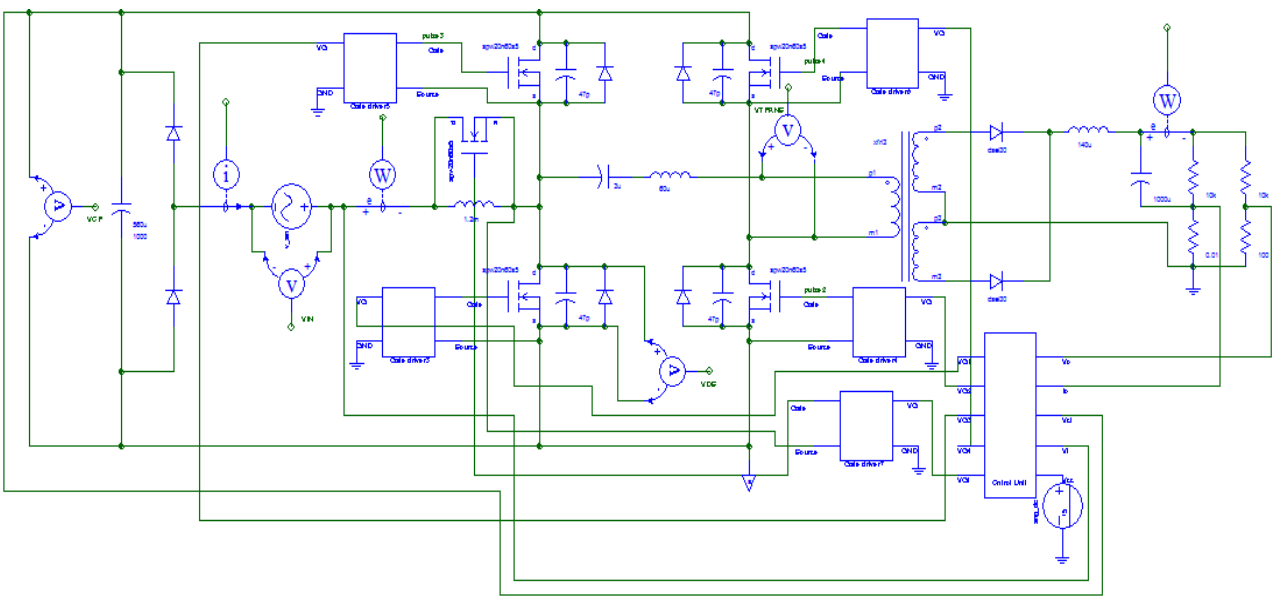


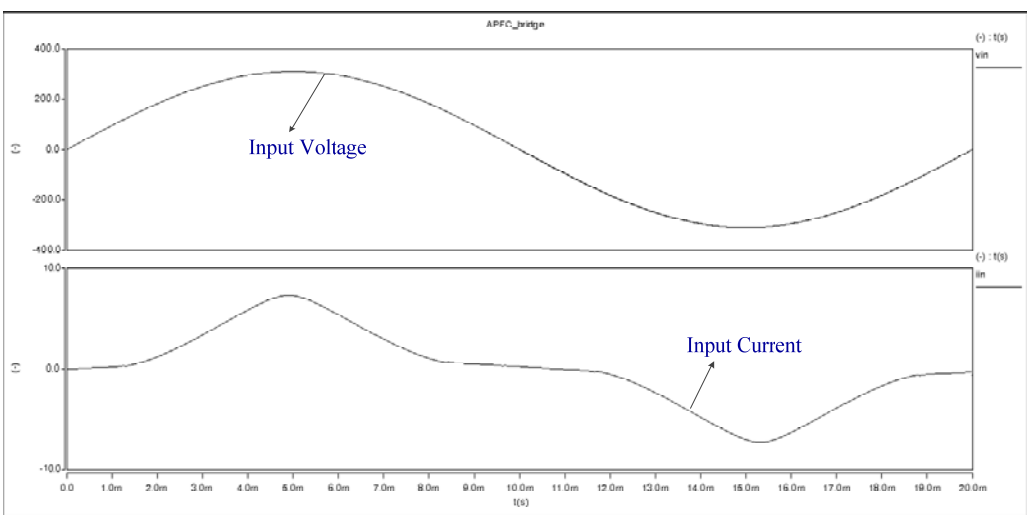
Fig. 9. Physical aspect of the developed prototype.

TABLE I
MAIN PARAMETERS OF THE PROTOTYPE

Parameter	Value
Input Voltage	220Vac/50Hz
Output Voltage	50~78Vdc
Bulk Current	13A
Float Current	5A
Maximum Output Power	1kW
Switching Frequency	50KHz
Dc-bus Voltage	420Vdc
Dc-bus Capacitor	2×450V/560μF
Input Inductance	1.2mH
Turns Ratio of Transformer	21:9
Bobbin of the Transformer	EE42
Output Filter Inductance	118μH



(a) Simulation model.



(b) Simulation results.

Fig. 10. Simulation model and simulation results of the proposed PCCM converter.

It is well known that a smaller turns ratio means a larger circulating loss in the primary side. Therefore, n should be chosen as large as possible after considering the duty cycle loss and the margin.

D. Selection of the Dc Bus Voltage VCF

According to (34), a larger dc bus voltage means a larger turns ratio and less circulating loss. However, the value of the dc bus voltage should be less than 450 V to allow the bulk capacitance at the primary-side dc bus to be implemented with standard 450 V electrolytic capacitors. Therefore, a voltage of 420V is chosen considering the voltage ripple.

E. Implementation of the Control Circuit

Fig. 8 shows a simplified schematic of the power converter and the controller. The single-ended transformer coupled gate driver circuit, which can provide isolation, is also presented in Fig. 8.

V. Simulation and Experimental Verifications

In order to verify the analysis above, a 1 kW voltage-fed single-stage full-bridge battery charger prototype for 60V-90Ah lead-acid batteries is built. The prototype is shown in Fig. 9. A TMS320F2812 is used to realize the controller and the charging strategy.

The main parameters of the prototype are selected based on the design considerations shown in Section IV. The detailed parameters are listed in Table I.

At first, the converter is built in Saber simulation software with the parameters in Table I. This is shown in Fig. 10(a).

Fig. 10(b) shows the steady-state input voltage and current waveforms of the PCCM voltage-fed single-stage full-bridge converter. The function of power factor correction is well realized.

The efficiency of the proposed converter obtained from the simulations is compared to that from the experiments in Fig. 11. The efficiency results are simulated for different load conditions which can be obtained from the charging profile shown in Fig. 6.

As shown in Fig. 11, the maximum error between the simulation and experimental results is less than 2% at the minimum load, and most of the errors are less than 1%. Thus, the simulation results are consistent with the experimental results.

Fig. 12 shows the input voltage V_I and inductor current I_L of the proposed battery charger at the maximum load. It can be seen that the inductor current ripple of the proposed converter is lower than that of the DCM converter. Thus, compared to the DCM control, the PCCM control increases the current-handling capability at heavy loads and a larger output power can be achieved.

Fig. 13 shows the input voltage and the input current. The input current is slightly distorted, the PF is 0.986, and the THD is 16.1%. Meanwhile, the PF and the overall efficiency during the charging process are plotted in Fig. 14. The power

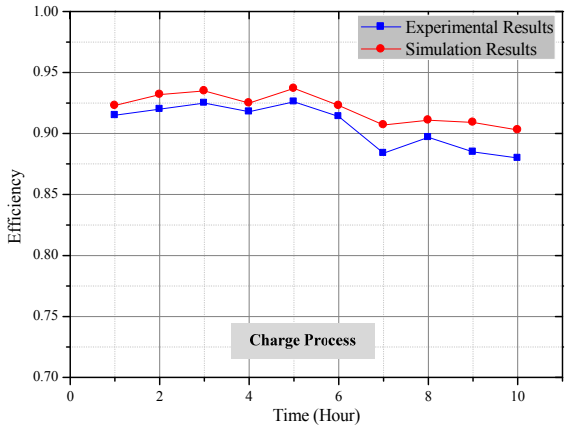


Fig. 11. Simulation results of the efficiency.

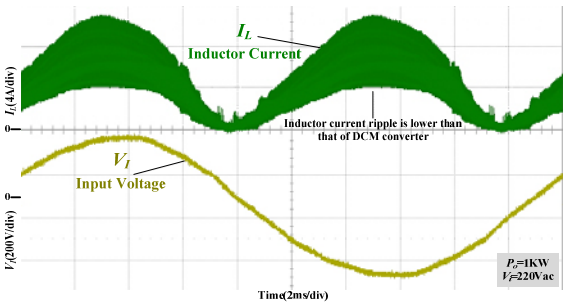


Fig. 12. Experimental waveform of input voltage V_I and input inductor current I_L.

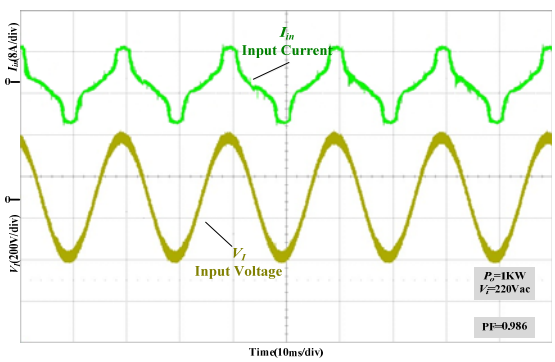


Fig. 13. Experimental waveform of input voltage and current.

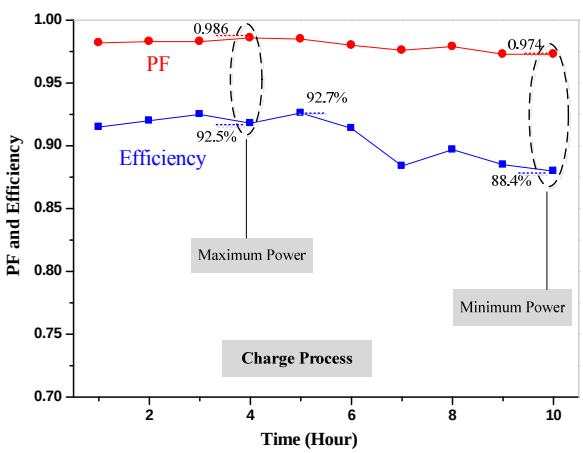


Fig. 14. PF and the overall efficiency over entire output power range.

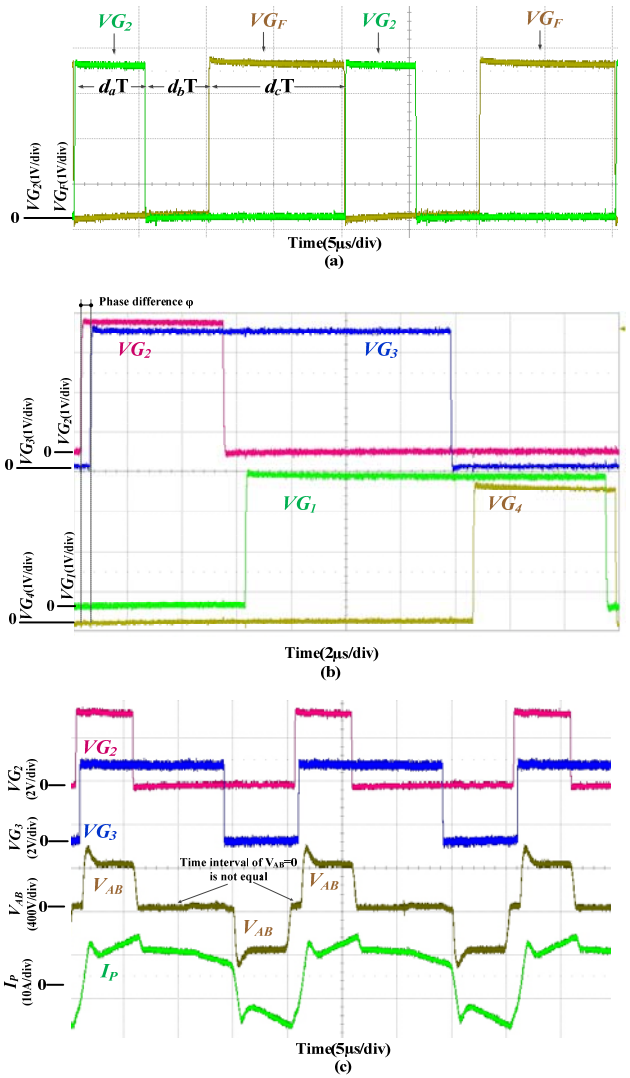


Fig. 15. Experimental waveforms of key drive signals. (a) Drive signals waveform of Q_2 and Q_f. (b) Drive signals waveform of the two legs. (c) Voltage across primary side V_{AB} and primary current I_P waveform versus gate drive signals.

factor is kept high over the wide output power range because there is no restriction of the PFC cell duty ratio.

Experimental waveforms of the drive signals of Q_2, Q_f, VG_2 and VG_F, over several switching cycles are shown in Fig. 15(a). Q_f is switched off just before Q_2 is switched on. Fig. 15(b) and (c) show the phase-shifted control of the dc/dc stage. In Fig. 15(b), the driver signals of Q_1, Q_2, Q_3 and Q_4 are shown. The gating signals for Q_1 and Q_3 are complimentary to those for Q_2 and Q_4, respectively. It can be seen that the duty ratio of Q_2 is about 0.3 and that the Q_1-Q_2 leg is the leading leg. The driver signals of Q_2 and Q_3 versus the voltage across the primary side and transformer primary current are shown in Fig. 15(c). The experimental waveforms shown in Fig. 15 verify the operating waveforms in Fig. 3.

VI. Conclusion

A novel PCCM voltage-fed single-stage PFC full-bridge battery charger is proposed in this paper. It combines the attractive features of CCM and DCM converters, which includes the low current ripple through the input inductor and the constant on-time operation. With these features, a large output power can be obtained while, more importantly, the restriction of the PFC cell duty ratio, which leads to input current distortion and an uncontrollable dc bus voltage, is eliminated by the constant on-time operation. The operation principle and features of the proposed charger were explained in detail. Then the design of the new converter was discussed. At last, simulation and experimental results were presented to confirm the feasibility of the battery charger and to verify the converter performance. The PF of the proposed converter is kept higher than 0.97 over the entire power range. In addition, the dc-bus voltage is controlled at 420Vdc, and standard 450 V electrolytic capacitors can be used.

The proposed converter operates without a low-frequency output voltage ripple. Thus, it is also suitable for many other applications. In addition, the overall efficiency of the proposed converter is affected by the freewheeling power switch. If a significant increase in the efficiency is desired, the output diodes can be replaced with synchronous rectifier MOSFETs which is very difficult for other single-stage voltage-fed full-bridge converters.

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