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An Isolated Bidirectional Modular Multilevel DC/DC Converter for Power Electronic Transformer Applications

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Abstract

With high penetration of renewable energies, power electronic transformers (PETs) will be one of the most important infrastructures in the future power delivery and management system. In this study, an isolated bidirectional modular multilevel DC/DC converter is proposed for PET applications. A modular multilevel structure is adopted as switching valves to sustain medium voltages to achieve modular design and high reliability. Only one high-frequency transformer is used in the proposed converter, which significantly simplifies the circuit and galvanic insulation design. A dual-phase-shift modulation strategy is proposed to regulate the output power and achieve a simple voltage balancing control. A down-scaled (2 kW/20 kHz) prototype is constructed to demonstrate the proposed converter and verify the control strategy. The experimental results comply with the theoretical analysis well, with the highest power efficiency reaching 97.6%.

Key words: DC/DC, Dual active bridge, Modular multilevel converter, Phase shift control, Power electronic transformer, Solid state transformer, Voltage balancing control

I. INTRODUCTION

With considerable progress of DC smart grids and distributed generations, power electronic transformers (PETs) or solid state transformers with low voltage DC bus have gained significant research interest in recent years [1]-[4].

Until now, several PET structures have been reported in [5]-[15]. Among these configurations, the three-stage structure (Fig. 1) is the most popular one because of its reactive power compensation capability, simple control, and high efficiency [3]. The medium voltage DC (MVDC) bus (Fig. 1) fully decouples the front-end AC/DC stage and the isolated DC/DC stage, while providing the possibility for future MVDC distribution. Voltage conversion and galvanic isolation are realized by the DC/DC stage, which is the main challenge in a PET converter to achieve high efficiency and high power density of the whole converter [16].

Therefore, this study focuses on the DC/DC stage. As shown in Fig. 1, for the 10 kV AC grid, the MVDC bus will reach 15 kV or higher, which is much greater than the voltage rating of present power semiconductor devices. Ultrahigh voltage rating silicon carbide (SiC) power devices show great advantages in this application [17], [18], although they are still far from commercial availability. The voltage issue can also be addressed by connecting low voltage rating power devices in series [19]; however, the voltage balance among these power devices is a great challenge, especially during dynamic transient [3].

Another way to sustain medium voltage is adopting multilevel topologies with low voltage rating power devices. The input–series–output–parallel structure is one of the most popular topologies [15], [16], [20]-[23]. The inputs of low voltage power cells are connected in series to sustain the medium DC voltage. Each power cell requires a high-frequency (HF) transformer to achieve galvanic isolation and voltage conversion. All HF transformers are usually immersed in an oil tank in practical applications to meet the requirements of galvanic isolation and heat dissipation [14]. The structure inside the oil tank is complex and fabricating cost is high. Meanwhile, each transformer requires four or more terminals outside the oil tank, which

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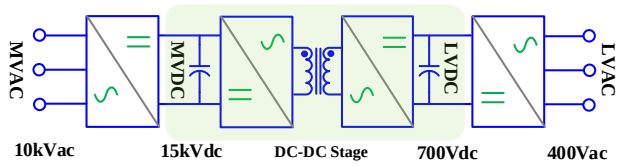


Fig. 1. Typical circuit structure of the three-stage PET converter.

makes the assembly more difficult. Therefore, a single HF transformer is preferred for such applications.

The modular multilevel structure can also sustain high input voltage with low voltage power devices, which has many advantages for high voltage applications, like modular design, high voltage scalability, simple redundancy design, high reliability, and controllable voltage slope (dv/dt) [24], [25]. Recently, a front-to-front modular multilevel converter is proposed to interconnect an HVDC grid and a MVDC grid [26]-[29]. Only one transformer is used in the converter to realize voltage matching and power transfer, which considerably simplifies the circuit and galvanic insulation design. A two-level or quasi-two-level modulation method is proposed to improve core utilization factor of the HF transformer [28], [29]. However, realizing voltage balancing control with the two-level or quasi-two-level modulation method is quite difficult.

Regarding the previously mentioned issues, a new isolated bidirectional modular multilevel DC/DC converter for PET applications is proposed in this study. A dual-phase-shift control strategy is proposed to regulate output power and achieve simple voltage balancing control. This study mainly discusses the characteristics of the proposed converter and the related control strategy. This paper is organized as follows: Section II presents the converter characteristics and operation principle. In Section III, the voltage balancing strategy is discussed. In Section IV, a down-scaled prototype is constructed to verify the proposed converter, and key experimental results are presented. Finally, the conclusion is given in Section V.

II. Principle of Operation

The circuit diagram of the proposed modular multilevel DC/DC converter is shown in Fig. 2 [30]. The primary H-bridge consists of two legs as switching valves. Each leg is composed of an upper arm, a lower arm, and a coupled inductor. A number of low voltage submodules (SMs) are cascaded to form an arm. Each SM is a half-bridge circuit with a voltage clamping capacitor. A coupled inductor is used to withstand instant voltage difference between the bus voltage and arm output voltage, and the inductor serves as a buffer impedance. In the secondary side, an active full bridge (H-bridge) circuit is adopted for bidirectional power flow.

With the modular multilevel structure, only one HF transformer is required to achieve voltage matching, galvanic

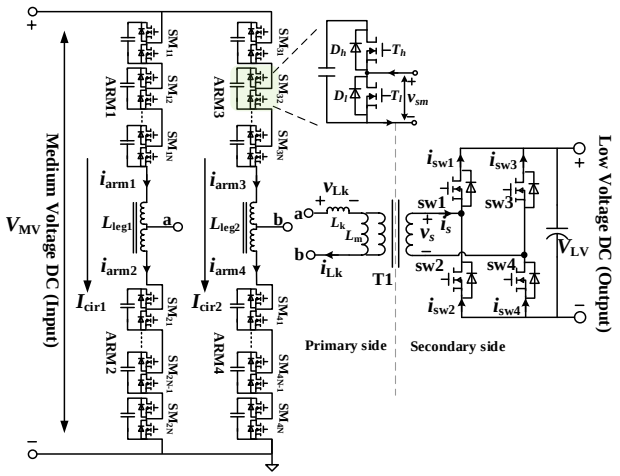


Fig. 2. Diagram of the proposed DC/DC converter.

isolation, and power exchange between the MVDC bus and LVDC bus; thus, the transformer can be easily immersed into an oil tank with a simple structure. As a result, assembly cost will be reduced and a smaller volume can be achieved. Meanwhile, the modular multilevel structure has high voltage modulation flexibility and low dv/dt can be achieved, which can further benefit the galvanic insulation design inside the transformer.

In the proposed topology, a coupled inductor instead of separate inductors is adopted in each leg for the following considerations: (1) The phase shift control for the traditional phase shifted dual active bridge (PS-DAB) converter is adopted for output power regulation to fully utilize the leakage inductance of transformer T1. Thus, with the coupled inductors, only their leakage inductances will be included in the power path, which are usually small and have a weak influence on output power control. As a result, the design of the coupled inductor and transformer can be decoupled. (2) The coupled inductors can guarantee that the primary winding current i_{Lk} is equally distributed into the upper and lower arms, to simplify voltage balancing control. (3) The magnetizing inductance of the coupled inductor serves as the arm inductance. High magnetizing inductance can be designed for circulating current ripple reduction and circuit protection, which does not affect the output power capability. For simplicity, leakage inductances of the coupled inductors are ignored in the following analysis.

Key steady-state voltage waveforms of the proposed converter are shown in Fig. 3. Output power is regulated by the phase shift angle Φ between the primary H-bridge output voltage v_{ab} and secondary H-bridge output voltage v_s, which is the same as that in a PS-DAB converter [31], [32]. In Fig. 3, v_{armi} is the output voltage of each arm and v_{smij} is the SM output voltage, which is the voltage across the low-side device in each SM, as shown in Fig. 2. Subscript $i \in \{1,2,3,4\}$ denotes the arm number and subscript $j \in \{1,2 \ldots N\}$ denotes the SM position in an arm. N is the total SM numbers in each

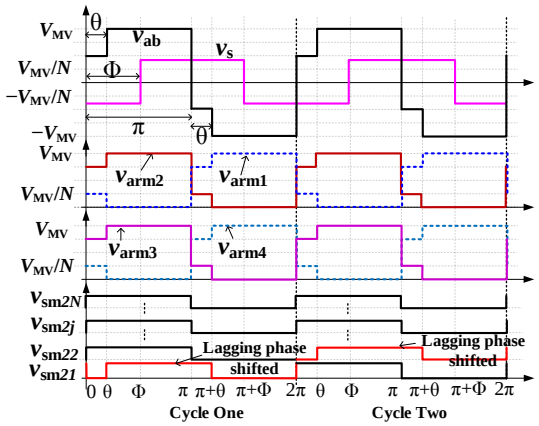


Fig. 3. Key steady-state voltage waveforms.

arm. The duty cycle of each SM output voltage is 50% by ignoring dead time. Given the symmetrical structure, only the SM output voltages in ARM2 are presented in Fig. 3 as an example.

In any switching cycle, one SM output voltage is lagging phase-shifted from the others in the same arm with angle θ, which is proposed for the voltage balancing control. This will be further elaborated in the next section. In the following analysis, θ is defined as the voltage balancing angle and Φ as the power control angle. When all SM voltages are balanced, the medium voltage V_{MV} is evenly distributed across the SM capacitors, and steady-state capacitor voltage V_{Csmij} is equivalent to V_{MV}/N.

Because of the phase-shifted SM output voltage, primary voltage v_{ab} slightly differs from a square waveform. By ignoring the voltage drop across the power devices, the magnitude of v_{ab} is reduced from V_{MV} to $(N-2)V_{MV}/N$ during 0 to θ and π to π + θ, as shown in Fig. 3. The magnitude of v_s is just the output voltage V_{LV}. According to the power control angle Φ and voltage balancing angle θ, the proposed DC/DC converter mainly has three operation modes, namely, Mode I (Φ ≥ θ), Mode II (0 ≤ Φ < θ), and Mode III (Φ < 0), where θ is a fixed angle between 0 and 0.5π. Key steady-state waveforms under different operation modes are shown in Figs. 4 to 6.

Mode I: Φ ≥ θ

Fig. 4 shows the main waveforms in this operation mode. The voltage difference between voltage v_{ab} and primary-referred secondary voltage v_s applies across the leakage inductance L_k, and determines inductor current i_{Lk}.

Based on the instant voltage magnitude of v_{ab} and v_s, instant inductor current i_{Lk} as a function of φ is derived as:

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}\left(\frac{N-2}{N}+G\right)\varphi+I_0,0\le\varphi<\theta \tag{1}$$

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}(1+G)(\varphi-\theta)+I_\theta,\theta\le\varphi<\Phi \tag{2}$$

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}(1-G)(\varphi-\Phi)+I_\Phi,\Phi\le\varphi<\pi \tag{3}$$

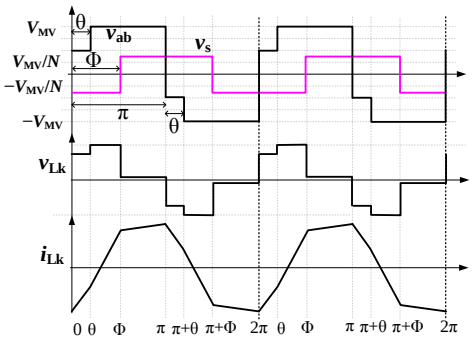


Fig. 4. Key steady-state waveforms in Mode I.

where

$$G=\frac{nV_{LV}}{V_{MV}},\quad \varphi=\omega t=2\pi f_{sw}t,$$

and G is the primary-referred DC voltage gain. n is the transformer primary-to-secondary turns ratio. ω is the angular switching frequency in rad/s. I_0, I_θ, and I_Φ are the inductor currents at $\varphi = 0$, $\varphi = \theta$, and $\varphi = \Phi$, respectively.

Given the symmetrical operation, at the end of the half switching cycle, we can obtain $I_0 = -I_\pi$ under a steady-state operation. Thus, from (1) to (3), inductor currents I_0, I_θ, and I_Φ can be derived as:

$$\begin{cases} I_0=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi-2G\Phi+\dfrac{2}{N}\theta\right] \\ I_\theta=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi-2G\Phi+\left(\dfrac{2N-2}{N}+2G\right)\theta\right] \\ I_\Phi=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi+2\Phi-\dfrac{2}{N}\theta\right] \end{cases} \tag{4}$$

Mode II: 0 ≤ Φ < θ

When the power-control angle Φ decreases to less than θ but greater than zero, the converter will operate in Mode II. The main waveforms in this mode are shown in Fig. 5.

Similar to the analysis in Mode I, instant inductor current i_{Lk} can be derived according to instant voltages v_{ab} and v_s.

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}\left(\frac{N-2}{N}+G\right)\varphi+I_0,0\le\varphi<\Phi \tag{5}$$

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}\left(\frac{N-2}{N}-G\right)(\varphi-\Phi)+I_\Phi,\Phi\le\varphi<\theta \tag{6}$$

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}(1-G)(\varphi-\theta)+I_\theta,\theta\le\varphi<\pi \tag{7}$$

With the relationship of $I_0 = -I_\pi$, inductor currents I_0, I_Φ, and I_θ can be derived as:

$$\begin{cases} I_0=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi-2G\Phi+\dfrac{2}{N}\theta\right] \\ I_\Phi=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi+\dfrac{2N-4}{N}\Phi+\dfrac{2}{N}\theta\right] \\ I_\theta=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi+2G\Phi+\left(\dfrac{2N-2}{N}-2G\right)\theta\right] \end{cases} \tag{8}$$

Mode III: $-\pi+\theta\le\Phi<0$

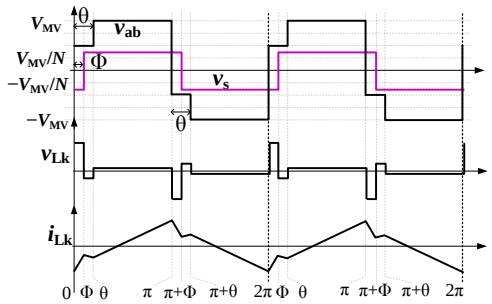


Fig. 5. Key steady-state waveforms in Mode II.

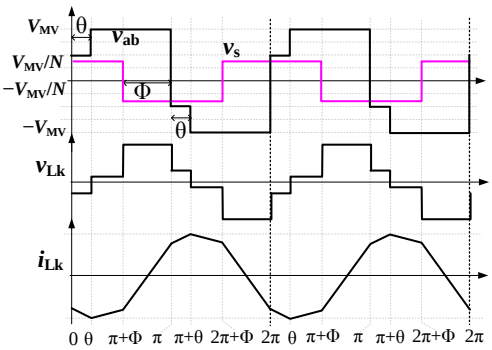


Fig. 6. Key steady-state waveforms in Mode III.

When power control angle Φ is further reduced to a negative value, the converter operates in backward mode and energy is transferred from the low voltage side to the medium voltage side. The key waveforms are shown in Fig. 6.

Similarly, instant inductor current i_{Lk} can be derived according to instant voltages v_{ab} and v_s.

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}\left(\frac{N-2}{N}-G\right)\varphi+I_0,0\le\varphi<\theta \tag{9}$$

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}(1-G)(\varphi-\theta)+I_\theta,\theta\le\varphi<\pi+\Phi \tag{10}$$

$$i_{Lk}(\varphi)=\frac{V_{MV}}{\omega L_k}(1+G)(\varphi-\pi-\Phi)+I_{\pi+\Phi},\pi+\Phi\le\varphi<\pi \tag{11}$$

With the relationship of $I_0 = -I_\pi$, inductor currents I_0, I_θ, and $I_{\pi+\Phi}$ can be derived as:

$$\begin{cases} I_0=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi+2G\Phi+\dfrac{2}{N}\theta\right] \\ I_\theta=\dfrac{V_{MV}}{2\omega L_k}\left[-(1-G)\pi+2G\Phi+\left(\dfrac{2N-2}{N}-2G\right)\theta\right] \\ I_{\pi+\Phi}=\dfrac{V_{MV}}{2\omega L_k}\left[(1-G)\pi+2\Phi-\dfrac{2}{N}\theta\right] \end{cases} \tag{12}$$

With (1)–(12), primary winding current i_{Lk} in a complete switching cycle under different operation modes can be attained.

By assuming a unitary power conversion efficiency, the converter output power is the output power of the primary H-bridge, which can be addressed by averaging the instantaneous power during the half switching period from 0 to π.

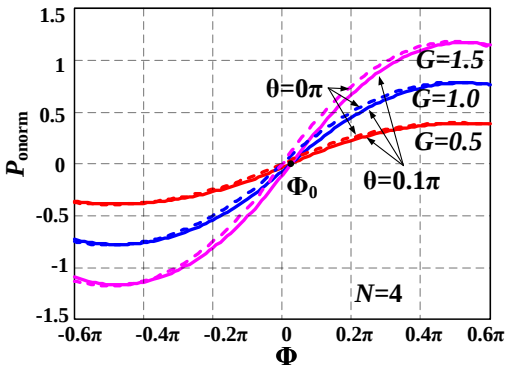


Fig. 7. Normalized output power versus phase shift angle Φ.

$$P_{out}=\frac{1}{\pi}\int_0^\pi v_{ab}(\varphi)i_{Lk}(\varphi)\mathrm{d}\varphi \tag{13}$$

By substituting instant voltage v_{ab} and instant current i_{Lk} under different operation modes into (13), the converter output power in the full power range can be written as (14).

$$P_{out}=\begin{cases} \dfrac{V_{MV}^2}{\omega L_k}\dfrac{G}{\pi}\left[-\Phi^2+\pi\Phi+\dfrac{2}{N}\theta\Phi-\dfrac{1}{N}\theta^2-\dfrac{1}{N}\pi\theta\right],\theta\le\Phi<\pi \\ \dfrac{V_{MV}^2}{\omega L_k}\dfrac{G}{\pi}\left[-\dfrac{N-2}{N}\Phi^2+\pi\Phi-\dfrac{2}{N}\theta\Phi+\dfrac{1}{N}\theta^2-\dfrac{1}{N}\pi\theta\right],0\le\Phi<\theta \\ \dfrac{V_{MV}^2}{\omega L_k}\dfrac{G}{\pi}\left[\Phi^2+\pi\Phi-\dfrac{2}{N}\theta\Phi+\dfrac{1}{N}\theta^2-\dfrac{1}{N}\pi\theta\right],-\pi+\theta\le\Phi<0 \end{cases} \tag{14}$$

For simplicity, the output power is normalized to a power base P_b, which is given as:

$$\begin{cases} P_{onorm}=P_{out}/P_b \\ P_b=V_{MV}^2/(\omega L_k) \end{cases} \tag{15}$$

Based on (14) and (15), the normalized output power of the proposed converter is plotted as the solid curves in Fig. 7 with θ = 0.1π and four SMs in each arm, that is, N = 4. For comparison, the normalized output power of the conventional PS-DAB converter is also plotted in Fig. 7 as dashed curves, which is a special case when the voltage balancing angle θ decreases to zero. The voltage v_{ab} differs from a square waveform; thus, the output power curves slightly deviate from that of a conventional PS-DAB converter. The maximum forward and backward output power occur at Φ = 0.5π + θ/N and Φ = −0.5π + θ/N, respectively. Also, the converter outputs zero power at Φ_0, which is given as:

$$\Phi_0=\frac{N\pi-2\theta-\sqrt{N^2\pi^2-8(N-1)\pi\theta+4(N-1)\theta^2}}{2(N-2)} \tag{16}$$

III. Submodule Voltage Balancing Control

The capacitor voltage of each SM must be balanced to ensure reliable operation of the proposed converter. If all active switches in the primary side are turned on/off simultaneously, the capacitor voltage will deviate from each other because of circuit tolerance. Circuit tolerance can lead to nonsynchronous PWM signals between different SMs,

asymmetrical PWM signals for the high-side switch and low-side switch in each SM, different switching transients, different SM capacitance, and so on. All these factors affect the SM voltage. Therefore, in this study, an additional phase shift control strategy is proposed for voltage balancing control.

Each SM mainly has two states, that is, inserted into an arm and bypassed from an arm (Table I). When the high-side switch (T_h or D_h) is turned on, SM will be inserted into the related arm. Arm current will flow through the SM capacitor, charging or discharging the capacitor. Hence, the integral of the arm current over a switching period when the high-side switch is turned on will determine the SM voltage state.

Given the symmetrical structure, ARM2 is still taken as an example to illustrate the proposed voltage balancing control mechanism. Key waveforms of ARM2 are shown in Fig. 8. In each switching cycle, one SM output voltage is lagging phase-shifted from the others with angle θ.

For a non-phase-shifted (NPS)-SM, the capacitor net charge in one switching cycle is the integral of the arm current from 0 to π, which is given in (17), as shown in Fig. 8.

$$\Delta Q_{C1} = \frac{1}{\omega}\int_0^{\pi} i_{arm2}(\varphi)d\varphi \tag{17}$$

For a lagging-phase-shifted (LPS)-SM, the capacitor net charge in one switching cycle is given in (18), which is the integral of the arm current from θ to π + θ.

$$\Delta Q_{C2} = \frac{1}{\omega}\int_{\theta}^{\pi+\theta} i_{arm2}(\varphi)d\varphi \tag{18}$$

The arm current mainly consists of a circulating current and half of the primary winding current i_{Lk}, which are given in (19) and (20) with direction shown in Fig. 2.

$$i_{arm1} = I_{cir1} + i_{Lk}/2;\ \ i_{arm2} = I_{cir1} - i_{Lk}/2 \tag{19}$$

$$i_{arm3} = I_{cir2} - i_{Lk}/2;\ \ i_{arm4} = I_{cir2} + i_{Lk}/2 \tag{20}$$

where I_{cir1} and I_{cir2} are the circulating currents in each leg by neglecting their ripple components, which can be derived from the converter output power.

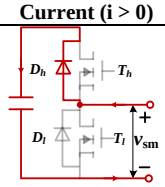
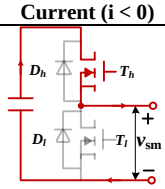
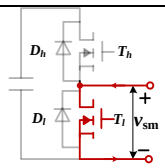
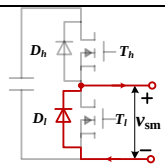
$$I_{cir1} = I_{cir2} = \frac{P_{out}}{2V_{MV}} \tag{21}$$

By substituting the instant arm current into (17), the NPS-SM net charge ΔQ_{C1} in one switching cycle under different operation modes can be derived as (22).

$$\Delta Q_{C1} = \begin{cases} -\dfrac{1}{N}\dfrac{V_{MV}}{2\omega^2 L_k}\left[-2G\Phi-(1-G)\pi+(1+G)\theta\right]\theta, \theta \le \Phi < \pi \\ -\dfrac{1}{N}\dfrac{V_{MV}}{2\omega^2 L_k}\left[-2G\Phi^2+2G\theta\Phi-(1-G)\pi\theta+(1-G)\theta^2\right], 0 \le \Phi < \theta \\ -\dfrac{1}{N}\dfrac{V_{MV}}{2\omega^2 L_k}\left[2G\Phi-(1-G)\pi+(1-G)\theta\right]\theta, -\pi+\theta \le \Phi < 0 \end{cases} \tag{22}$$

From (18), the LPS-SM net charge ΔQ_{C2} in one switching cycle under different operation modes can be derived as (23), which is equal to $N-1$ times ΔQ_{C1} with opposite polarity.

TABLE I
SM STATE ANALYSIS

		Positive Arm Current (i > 0)	Negative Arm Current (i < 0)
Inserted	SM ON		
	Capacitor State	Charging	Discharging
Bypassed	SM OFF		
	Capacitor State	Unchanged	Unchanged

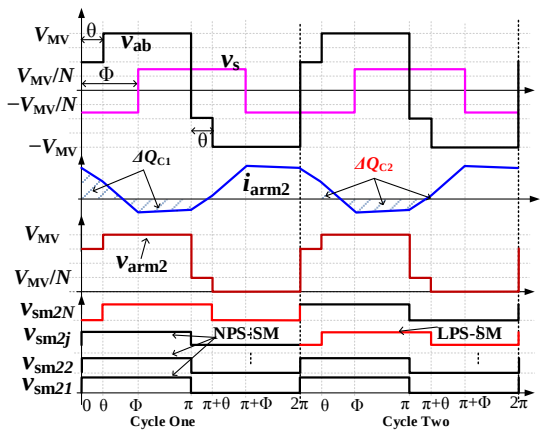


Fig. 8. Key steady-state waveforms of ARM2.

$$\Delta Q_{C2} = -(N-1)\Delta Q_{C1} \tag{23}$$

For simplicity, SM capacitor net charges written in (22) and (23) are normalized to a net charge base ΔQ_{Cb}.

$$\begin{cases} \Delta Q_{C1norm} = \Delta Q_{C1}/\Delta Q_b \\ \Delta Q_{C2norm} = \Delta Q_{C2}/\Delta Q_b \\ \Delta Q_b = V_{MV}/(\omega^2 L_k) \end{cases} \tag{24}$$

The normalized SM capacitor net charge in one switching cycle versus the power control angle Φ at θ = 0.1π is plotted in Fig. 9. Four SMs in each arm are still used for analysis. The minimum ΔQ_{C1} and maximum ΔQ_{C2} occur at Φ = θ/2, which can be derived from (22). If the net charge is positive, the SM capacitor will be charged after one switching cycle; otherwise, it will be discharged. As illustrated in Fig. 9, the voltage gain G has a direct effect on the net charge value. At high voltage gain, the curves will cross the zero line, which means the SM capacitor will change from charging state to discharging state when output power changes, or vice versa. High voltage gain will complicate the voltage balancing control, especially at the zero net charge points Φ_1–Φ_4, where the net charge is zero and SM voltages will be uncontrollable.

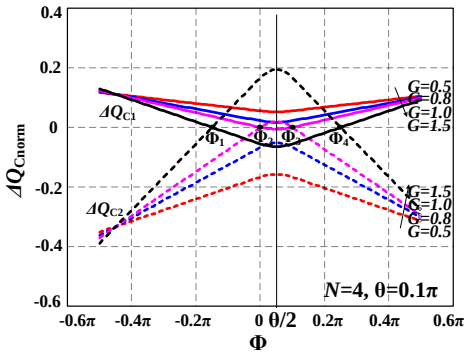


Fig. 9. Normalized SM capacitor net charge versus power-control angle Φ.

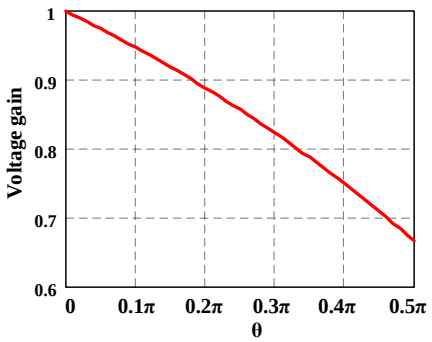


Fig. 10. Critical voltage gain at different voltage-balance angles θ.

In order to simply the voltage balancing control, it is better that the curves in Fig. 9 do not change their polarities during the entire power range, which indicates a critical voltage gain with a given voltage balancing angle θ. By setting the minimum value of ΔQ_{C1} above zero or the maximum value of ΔQ_{C2} below zero, the critical voltage gain can be derived as (25) and plotted in Fig. 10.

$$G \le \frac{2\pi - 2\theta}{2\pi - \theta} \tag{25}$$

When the voltage gain is less than the critical value, the net charge ΔQ_{C1} will always be above zero and ΔQ_{C2} will always be below zero. Thus, with a given angle θ, the capacitor in NPS-SM will be charged and the capacitor in LPS-SM will be discharged after one switching cycle during the whole power range. With this characteristic, the output voltage of the SM with the maximum voltage can be simply lagging phase-shifted with angle θ to discharge the capacitor without detecting the arm current direction, which is usually required in the traditional modular multilevel converter (MMC) [24], [25].

Fig. 11 shows the dynamic voltage balancing process based on the above analysis, which takes four SMs in each arm as examples. The capacitor voltage in each SM realizes once dynamic balance in N switching cycles, which include $N-1$ charging cycles and one discharging cycle as theoretically determined by (23).

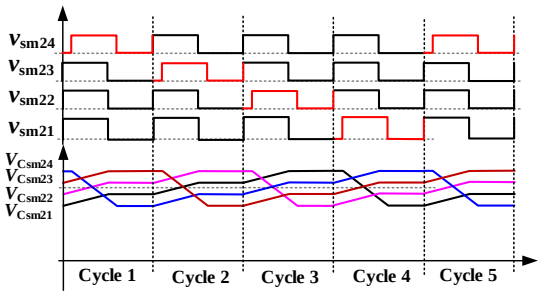


Fig. 11. Dynamic voltage balancing process.

With the proposed voltage balancing strategy, the frequency of AC voltage applied to the isolation transformer is the same as the switching frequency, and a high isolation frequency can be achieved. In addition, the SM capacitor in the proposed converter is a kind of voltage clamping capacitor instead of an energy storage capacitor in the traditional MMC. As shown in the shadowed area in Fig. 8, most of the positive current integral will cancel out with the negative component, and the capacitor net charge in one switching cycle will be small, making the voltage ripple also small. Therefore, the required SM capacitance is small with a given voltage ripple.

In summary, the power regulation method for the proposed converter is similar to a conventional PS-DAB converter. The voltage balancing control for the cascaded SMs is realized by a simple phase-shift scheme between the SM output voltages without arm current detection.

IV. Experimental Verification

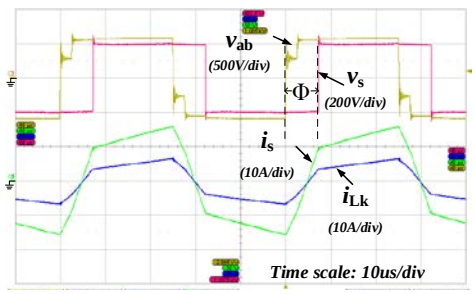
A down-scaled prototype is constructed to demonstrate the proposed modular multilevel DC/DC structure. Discrete SiC MOSFETs (C2M0080120D from Cree) are adopted as active switches to achieve high isolation frequency and low switching loss. Meanwhile, the intrinsic diodes of SiC MOSFETs show a small reverse recovery current [33]. Thus, even under hard-switching operations, the active devices will not fail to work.

The key parameters of the prototype are listed in Table II. Based on the above analysis, voltage balancing angle θ is fixed to 0.1π. The voltage gain at the rated condition is set at 0.83 to meet the critical voltage gain requirement given in (25). Also, this voltage gain allows voltage disturbance in both voltage buses. The switching frequency is designed at 20 kHz to avoid the acoustic noise. An EE-type ferrite core is used for the HF transformer, and Litz wires are adopted for transformer windings to reduce copper loss.

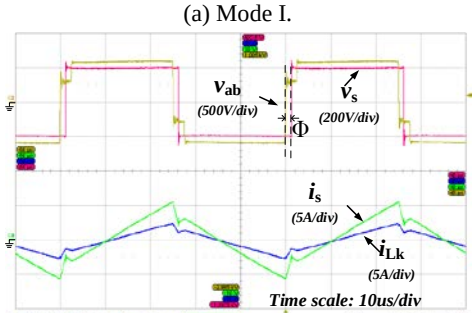
First, the converter under different operation modes is tested, and the experimental waveforms are presented in Fig. 12. Output power is 2 kW in Mode I, 0.25 kW in Mode II, and −2 kW in Mode III. The experimental results match the theoretical analysis well, which means the converter works well with the proposed dual-phase-shift method. The phase

TABLE II
KEY PROTOTYPE PARAMETERS

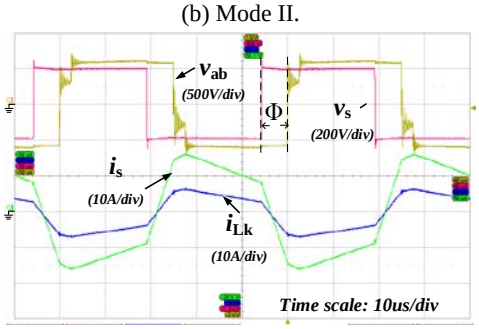
Parameters		Value	Unit
Medium voltage DC bus		600	Vdc
Low voltage DC bus		200	Vdc
Rated output power		2	kW
Isolation frequency		20	kHz
SM number in each arm		4	/
SM voltage		150	V
SM capacitance		10	μF
Transformer	Turns ratio	40:16	/
	Primary magnetizing inductance	16.54	mH
	Primary side leakage inductance	658	μH
	Core	EE130/130/40	mm
Coupled inductor	Turns ratio	1:1	/
	Magnetizing inductance per winding	370	μH
	Leakage inductance per winding	25	μH



(a) Mode I.



(b) Mode II.



(c) Mode III.

Fig. 12. Key waveforms in different operation modes.

shift angle Φ at the rated forward power is greater than that at the rated backward power, which complies with the theoretical output power curves shown in Fig. 7. Because of voltage balancing control, the primary H-bridge outputs a multilevel voltage with 50% duty cycle, which is different from the traditional PS-DAB converter.

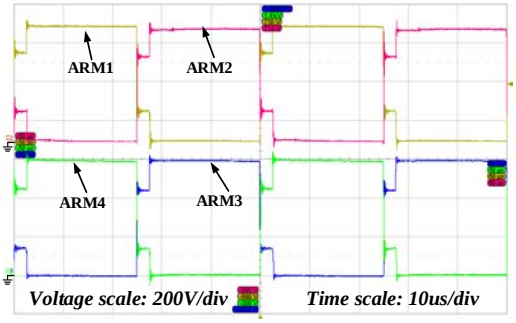


Fig. 13. Arm output voltages at the rated forward power.

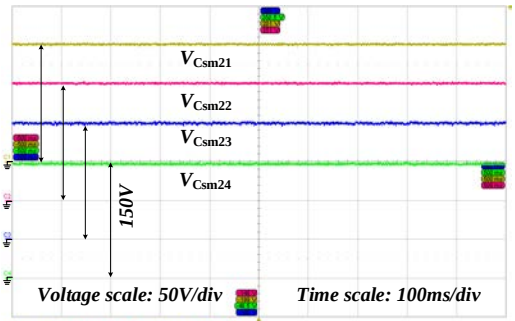


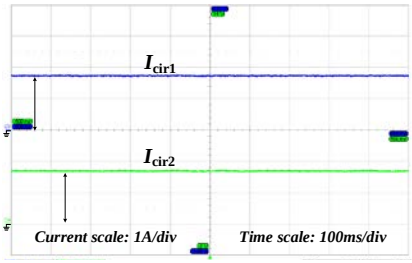
Fig. 14. SM voltages in ARM2 at the rated forward power.

The output voltages of each arm at the rated forward power are given in Fig. 13, which are the same as the theoretical waveforms shown in Fig. 3. The magnitude of the upper arm voltages and lower arm voltages is close to each other.

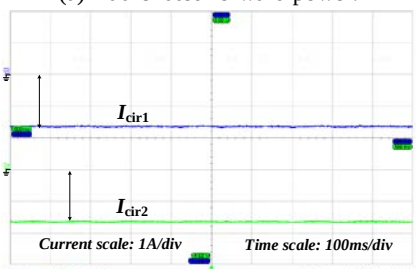
Given the symmetrical structure, only SM voltages in ARM2 are measured for verification, as shown in Fig. 14. The steady-state SM capacitor voltage is 150 V, which is the same as the theoretical value V_{MV}/N. The voltage ripples are small. Figs. 13 and 14 indicate that all SM voltages are well-balanced with the proposed dual-phase-shift control strategy.

Fig. 15 shows the circulating currents in each leg at the rated condition. The two legs share the same DC current either at the rated forward power or at the rated backward power. As shown in Fig. 15(a), the circulating currents are positive at the rated forward power, which means that energy is transferred from the medium voltage side to the low voltage side. At the rated backward power, the polarity of the circulating currents changes to negative, as shown in Fig. 15(b).

Because of the coupled inductor in each leg, the primary winding current i_{Lk} is equally distributed into the upper and lower arms, which can be verified by the measured waveforms shown in Fig. 16. Given the symmetrical structure, only the waveforms of ARM1 and ARM2 are presented here. Obvious DC component can be found in the arm current.

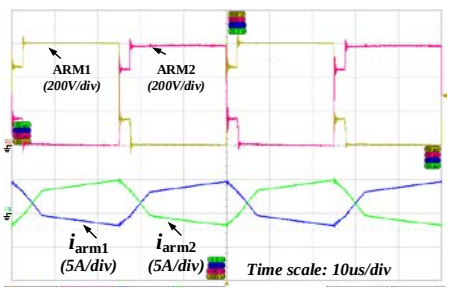


(a) At the rated forward power.

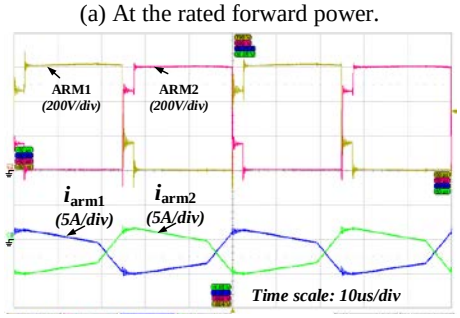


(b) At the rated backward power.

Fig. 15. Circulating current waveforms.



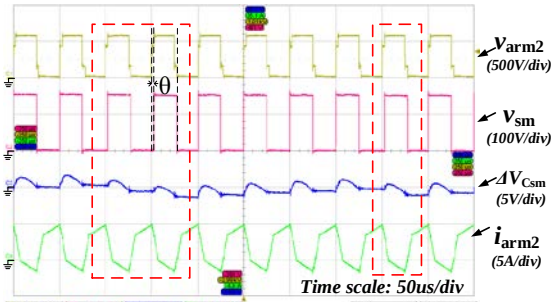
(a) At the rated forward power.



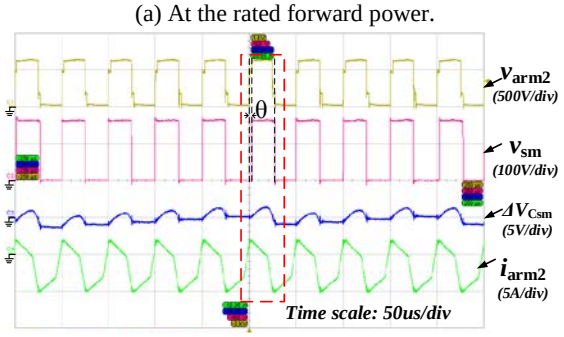
(b) At the rated backward power.

Fig. 16. Arm current waveforms.

Fig. 17 shows the dynamic SM voltage balancing mechanism. For clarity, the SM capacitor voltage ripple (AC component) instead of steady-state voltage is measured. Fig. 17 show the key waveforms at the rated forward power and rated backward power. From the waveforms in the dashed area, SM output voltage is lagging phase-shifted with angle θ compared with the arm output voltage. In both forward and backward modes, the LPS-SM voltage decreases and the capacitor is discharged, which confirms the theoretical analysis shown in Figs. 9 and 11. When the SM capacitor voltage decreases and is not the maximum one in the same arm, the SM output voltage will not be phase-shifted, and the capacitor is charged. This simple method ensures that all

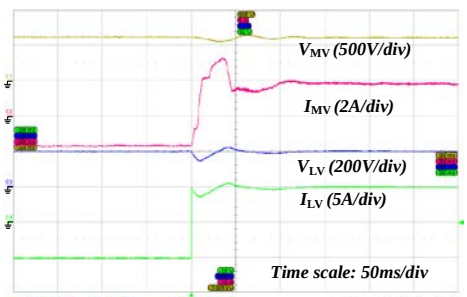


(a) At the rated forward power.

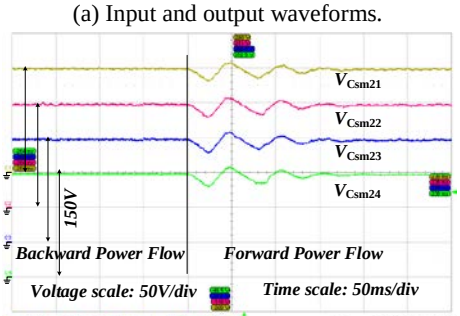


(b) At the rated backward power.

Fig. 17. The dynamic voltage balancing process.



(a) Input and output waveforms.



(b) SM voltages in ARM2.

Fig. 18. Dynamic performance at load transient.

capacitor voltages are balanced. Different from the theoretical waveforms in Fig. 11, SM output voltage may be successively lagging phase-shifted for more than one switching cycle in practical converters, as shown in Fig. 17(a), which is mainly caused by voltage sampling delays, noise, and sampling errors.

The dynamic response performance of the proposed converter is also tested, as shown in Fig. 18. In our setup, the low voltage DC bus is sampled for closed-loop control with a simple PI controller. Fig. 18(a) presents the input and output

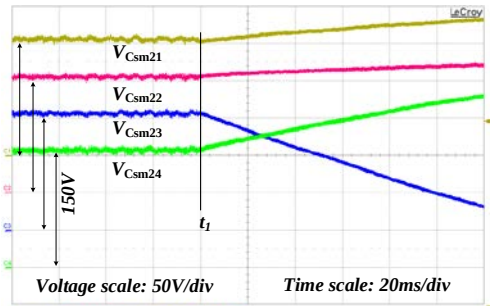


Fig. 19. SM voltages in ARM2 without voltage balancing control.

waveforms when the output power steps are from –1 kW to 1 kW. When the power source at the low voltage side is turned off, the converter will draw high power from the medium voltage input side to maintain the output voltage. SM voltages in ARM2 during the load step transient are shown in Fig. 18(b). After a small voltage oscillation, all SM voltages immediately return to their steady-state value. SM voltages are balanced not only in steady-state operations, but also during dynamic transient, which validates the proposed voltage balancing control strategy.

Fig. 19 shows the submodule voltages in ARM2 when disabling the control method at time t_1. Once the voltage balancing method is disabled, the submodule voltages deviate from each other immediately. After a short transient, the converter fails to work.

The experimental results show that the proposed converter can achieve bidirectional power flow and HF isolation. The proposed voltage balancing strategy guarantees that the capacitor in each SM share a uniform voltage to achieve high input voltage with low voltage power devices. Based on the prototype, the highest measured efficiency reaches 97.6% at approximately 1 kW.

V. CONCLUSIONS

In this study, an isolated bidirectional modular multilevel DC/DC converter with a single HF transformer for PET applications is proposed and analyzed. A modular multilevel structure is adopted to achieve high input voltage and high operation reliability with low voltage power devices. A single transformer dramatically simplifies its galvanic insulation design and circuit structure.

A dual-phase-shift control strategy is proposed to regulate output power and ensure voltage balance among the cascaded submodules to achieve high power efficiency. In addition, the leakage inductance of the HF transformer can be fully utilized.

A down-scaled prototype is constructed to verify the proposed topology and control method. All submodule voltages are well-balanced with the proposed dual-phase-shift method. The experimental results at steady-state and dynamic transient are presented in this study, which are in good agreement with the theoretical analysis.

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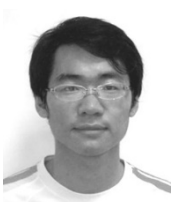

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