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Design of a High-Precision Constant Current AC-DC Converter with Inductance Compensation

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Abstract

A primary-side regulation AC-DC converter operating in the PFM (Pulse Frequency Modulation) mode with a high precision output current is designed, which applies a novel inductance compensation technique to improve the precision of the output current, which reduces the bad impact of the large tolerance of the transformer primary side inductance in the same batch. In this paper, the output current is regulated by the OSC charging current, which is controlled by a CC (constant current) controller. Meanwhile, for different primary inductors, the inductance compensation module adjusts the OSC charging current finely to improve the accuracy of the output current. The operation principle and design of the CC controller and the inductance compensation module are analyzed and illustrated herein. The control chip is implemented based on a TSMC 0.35μm 5V/40V BCD process, and a 12V/1.1A prototype has been built to verify the proposed control method. The deviation of the output current is within ±3% and the variation of the output current is less than 1% when the inductances of the primary windings vary by 10%.

Key words: AC-DC converter, Constant current, Inductance compensation, PFM, Primary-side regulation

I. INTRODUCTION

Flyback AC-DC converters with the PSR (primary-side regulation) structure are widely used in many power supply applications, including LED drivers, chargers for portable electronic equipment and off-line power supply adapters [1], [2], [3]. They have the advantages of simplicity and cost-effectiveness. Compared with the conventional secondary feedback converters, the topology of primary-side regulation does not have the demand for an optical coupler or a precise voltage source [4], [5], which reduces both the volume and cost [6], [7]. In addition, the PSR structure has a good system reliability. Nevertheless, for PSR converters, high demands are required in terms of the performance of the transformer. For CC controllers, the PFM is a common mode for adjustment due to its high efficiency and feasibility [8]. The CC output accuracy of a PSR constant current AC-DC converter is easily affected by the primary inductance of the transformer. However, the inductance of the primary windings in the same batch has a tolerance of ±10%. Thus, for the CC converter, an inductance compensation function should be employed in the circuit, to reduce the variations of the output current caused by differences on the primary inductance.

A primary side inductance compensation circuit is proposed in [9]. The compensation module adjusts the input power, which is influenced by the primary inductance, which keeps it constant. However, it only accomplishes a theoretical analysis. Another compensation technology for inductance tolerance is illustrated in [10]. A target time is set to indicate how long the primary current takes to reach a predetermined current limit. The real ramp time before the primary current stops increasing is compared to this target time and the error signal is used to adjust the switching frequency and pulse width, which maintains a constant output current. However, this compensation circuit has a complex structure. In addition, a primary inductance correction circuit is introduced in [11]. A compensation current is generated based on the output current, which is sampled and injected into the OSC for regulating the switching frequency, to correct the output power change caused by inductance tolerance. However, the output accuracy is constrained by the sampling precision.

To overcome these drawback, a PSR High-precision constant current AC-DC converter, operating in the PFM mode and adopting the inductance compensation method, is presented in this paper. This paper is organized as follows. The

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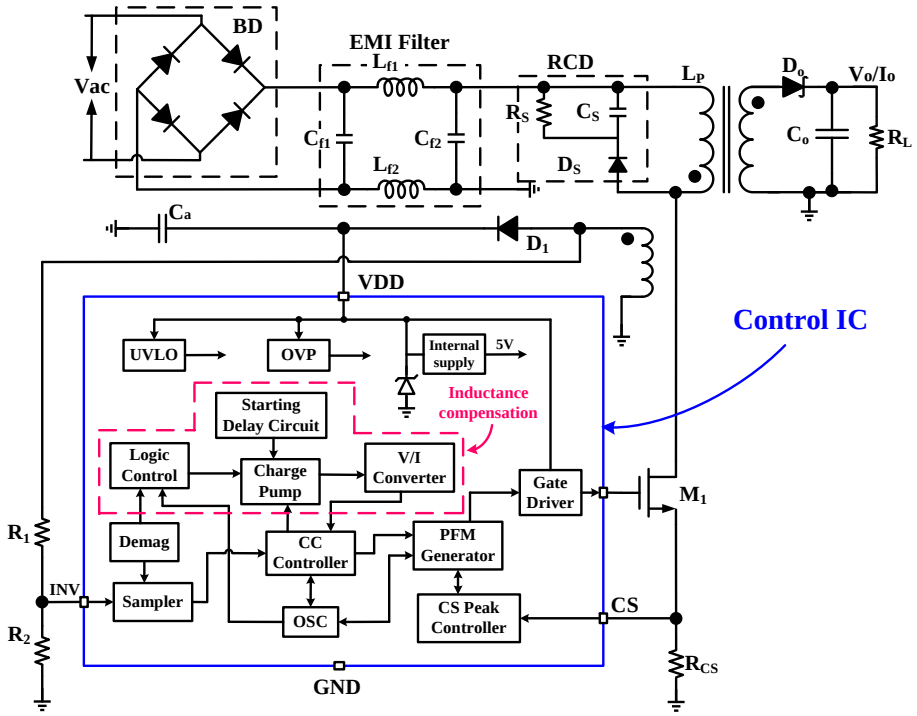


Fig. 1. Schematic diagram of PSR AC-DC converter.

operation principle and design of the constant current and compensation are illustrated in Section II. Some experimental results based on a prototype are given in Section III. Section VI presents some conclusions.

II. Design of the PSR AC-DC Controller Chip

A. System Review

A system diagram of a PSR constant current AC-DC flyback converter with the proposed control chip is shown in Fig. 1 [12]. It is comprised of a bridge rectifier BD, EMI filter, RCD clamp circuit, freewheel diodes D_0 and D_1, capacitors C_0 and Ca, transformer, power switch M_1, primary current sensing resistor R_{CS}, pull-up resistor R_1, pull-down resistor R_2, and control IC. For this control chip, an INV pin is used to detect information on the output voltage through the auxiliary winding. The CS pin is used to detect the primary side current, and GATE pin is used to drive the power switch.

A block diagram of the control IC is shown in Fig. 1. It mainly consists of a sampling trigger module, OSC (Oscillator) module, PFM generator, inductance compensation module, CS peak controller and gate driver module. The switching frequency is generated by the OSC module and in proportion to the charging current. The sampling trigger module contains a sampler and a Demag module, which is a demagnetization time detector. Information on the output voltage is sampled from the auxiliary winding cycle by cycle. It is then input to the CC controller. At this point, the CC controller regulates the frequency of the OSC, which makes the PFM generator create a modulated pulse for driving the power switch. The CS peak controller is used to keep the primary peak current constant. The inductance compensation module, including the control circuit, charge pump, voltage to current (V/I) converter and compensation starting delay circuit, is applied to compensate the loss of the output current accuracy owing to the different inductances of the transformer primary windings in the same batch.

B. Design of Constant Current Modules

The PFM mode is employed to achieve a constant current output. In the switch power circuit, the output power can be expressed as:

$$V_o I_o = \frac{1}{2}\eta \cdot L_p \cdot F_S \cdot I_{pp}^2 \tag{1}$$

where η is the transformer conversion efficiency, L_p is the primary inductance, F_S is the switching frequency, and I_{pp} is the primary peak current.

In the PSR controller, shown in Fig. 1, the relationship between the voltage of the INV pin and the output voltage V_o is:

$$V_o = \frac{R_1 + R_2}{N \cdot R_2} \cdot V_{INV} \tag{2}$$

In eq. (2), R_1 is the pull-up resistance, R_2 is the pull-down resistance, and V_{INV} is the voltage sampled from the INV pin. N is the turn's ratio of the auxiliary and secondary windings. Based on eq. (1) and eq. (2), the output current I_o can be derived as:

$$I_o = \frac{1}{2}\eta \cdot L_p \cdot I_{pp}^2 \cdot N \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{F_S}{V_{INV}} \tag{3}$$

On the basis of the analysis above, the OSC charging

current is adjusted based on the sampled voltage V_{INV} (the OSC charging current is proportional to V_{INV}), and the OSC charging current is proportional to F_S to keep the ratio of F_S and V_{INV} constant. However, the output current precision is influenced by the conversion efficiency of the transformer η, since it may vary slightly under different input voltages and loads.

For a converter operating in the PFM mode, if the load is extremely light (the output voltage is extremely low), the switching frequency F_S drops to a very small value, causing the V_{INV} sampling speed to be quite slow as a result of V_{INV} being sampled cycle by cycle. When the load jumps from light to heavy, the controller cannot handle the load step rapidly and the output current decreases instantly. It would take too long of a response time for the output to become constant again. In order to overcome this shortcoming of the PFM mode, it is necessary to determine a minimum value for the switching frequency. However, this increases the power dissipation under light loads.

The CC controller is shown in Fig. 2, where *EA* is an error amplifier, *INV*1 is an inverter, and *COMP*1 is a current comparator. The connection between the CC controller and the inductance compensation module can also be seen in Fig. 2.

In Fig. 2, *en*1 is the active-low enable signal for the inductance compensation module. I_{OSC}, the OSC charging current, can be expressed as:

$$I_{OSC}=\begin{cases} I_1=\dfrac{V_{INV}}{R_3}-I_{OSCadj} & (I_1\geq I_2) \\ I_2 & (I_1<I_2) \end{cases} \tag{4}$$

I_{OSCadj} is the fine adjusting current from the inductance compensation module, which helps to improve the accuracy of the output current. I_1 is proportional to V_{INV}, and I_2 is a constant value.

For the circuit in Fig. 2, if I_1, the current controlled by V_{INV} and inductance compensation module, is less than I_2, I_{OSC} becomes equal to I_2 due to the current comparator, which determines the minimum frequency under the CC mode. If I_1 is larger than I_2, I_{OSC} is controlled linearly by V_{INV} with the scale factor $1/R_3$ and it is regulated slightly by the inductance compensation module.

C. Design of Inductance Compensation Circuit

For flyback converters produced in the same batch, the inductances of the transformer magnetizing inductors have a tolerance of about 10%, which leads to inconsistent output currents from these converters. This can be explained based on the equation of I_o, eq. (3). The magnetizing inductor of a flyback converter is the primary inductor of the transformer. Hence, an inductance compensation module is needed, in order to acquire a constant output current that is unrelated to the primary inductance L_p.

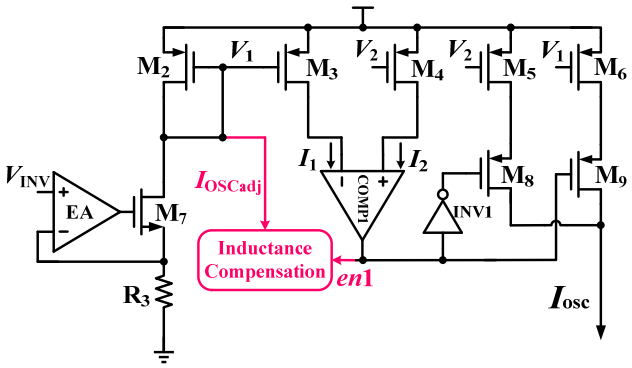


Fig. 2. CC (constant current) Controller.

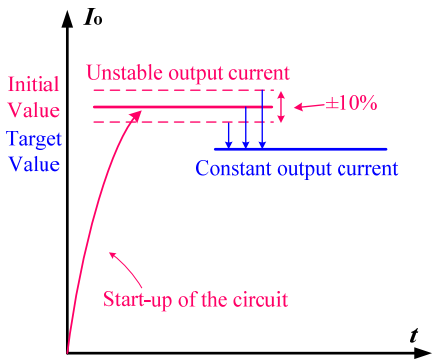


Fig. 3. The process of CC regulation.

The process of CC regulation is illustrated in Fig. 3. It is seen that when the system begin to start up, the compensation module does not work at first. The CC controller enters the operating state and the output current rises to an initial value, which is a little larger than the target value. At this moment, the primary inductance has a bearing on the output current, and the accuracy can be easily influenced. Until the state of the output current becomes steady, the inductance compensation module works, which makes the output current drop to the target value. Then the accuracy of output current is immune to the unstable primary inductance and is maintained at a constant level.

It is known that L_p is difficult to measure directly. Thus, L_p can be calculated based on demagnetization time T_D and primary peak current I_{pp}:

$$L_p=n\cdot\frac{V_o}{\sqrt{\eta}\cdot I_{pp}}\cdot T_D \tag{5}$$

where n is the turn's ratio of the primary and secondary windings. According to eq. (1) and eq. (5), the output current equation can be inferred as follows:

$$I_o=\frac{1}{2}\sqrt{\eta}\cdot n\cdot I_{pp}\cdot T_D\cdot F_S \tag{6}$$

From the above analysis, the primary peak current I_{pp} is fixed. Therefore, if the product of the demagnetization time T_D and the switching frequency F_S is constant, it can be noticed from eq. (6) that the output current is kept constant and is unconcerned with L_p. In addition, comparing the

transformer conversion efficiency η in eq. (3) and eq. (6), it is obvious that the variation of η has relatively less influence on the output current if the CC regulation is based on eq. (6). Then a higher output current precision can be achieved.

In order to obtain an unchanged product of T_D and F_S, the inductance compensation module detects the demagnetization time T_D and compares it with half a switching period, $1/2T_S$. If T_D is shorter than $1/2T_S$, the compensation module decreases I_{OSCadj} to increase I_{OSC} , which makes the switching period shorter. On the other hand, if T_D longer than $1/2T_S$, the compensation module increases I_{OSCadj} to decrease I_{OSC}, then the switching period becomes longer. After several switching periods for adjusting, T_D is forced to be equal to $1/2T_S$. In other words, the product of T_D and F_S remains a constant value 1/2.

The inductance compensation circuit includes four main parts: the control circuit, charge pump, V/I converter and compensation starting delay circuit. Each part plays an important role in the regulation process. These circuits are analyzed in detail.

1) Control Circuit: The control circuit is the core part of the inductance compensation module. It offers a control signal based on T_D and $1/2T_S$, as shown in Fig. 4. *COMP*2 is a comparator and *FF*1 is a rising-edge triggered D flip-flop. V_{demag} is the demagnetization signal from the Demag module, and CLK is the output signal of the OSC.

The length of T_D and $1/2T_S$ should be converted to the corresponding voltage in order to detect them conveniently. Based on the current equation of the capacitance:

$$I = C\frac{dV_C}{dt} \tag{7}$$

The voltage on the capacitor can be calculated as eq. (8) if the current I is constant.

$$V_C = \frac{I}{C}t \tag{8}$$

In Fig. 4, C_2=2C_1. Thus, the voltage of V_{C1} and V_{C2} represents the length of T_D and $1/2T_S$. The working process of the control circuit is shown in Fig. 5.

As shown in Fig. 5, two switching periods compose one working period. During the first switching period, M_{10} is turned on by the logic circuit and C_1 is charged by I_3 at the rising edge of the demagnetization signal V_{demag}, when the demagnetization occurs. M_{10} is turned off when the demagnetization is over and the voltage V_{C1} on the capacitor C_1 stays constant. In the whole second switching period, M_{11} is turned on and C_2 is charged by I_3. At the end, the voltage V_{C1} on the capacitor C_1 is compared with the voltage V_{C2} on the capacitor C_2. The result is then stored in D flip-flop and stays unchanged until the end of another two switching periods. In Fig. 5, *ctl* is at a low level when V_{C1}>V_{C2}. On the other hand, if V_{C1}<V_{C2}, *ctl* is switched to high.

After one working period, in order to not affect the next comparison, the charge on C_1 and C_2 should be immediately

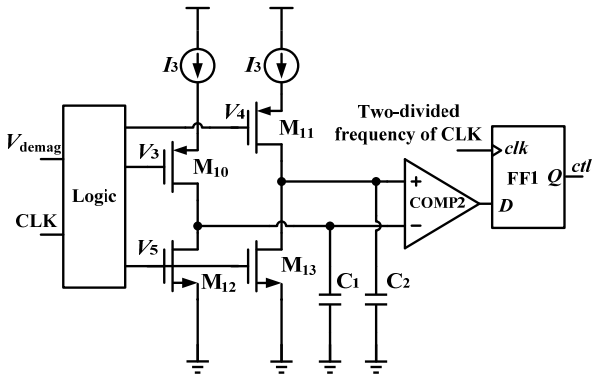


Fig. 4. Design implementation of control circuit.

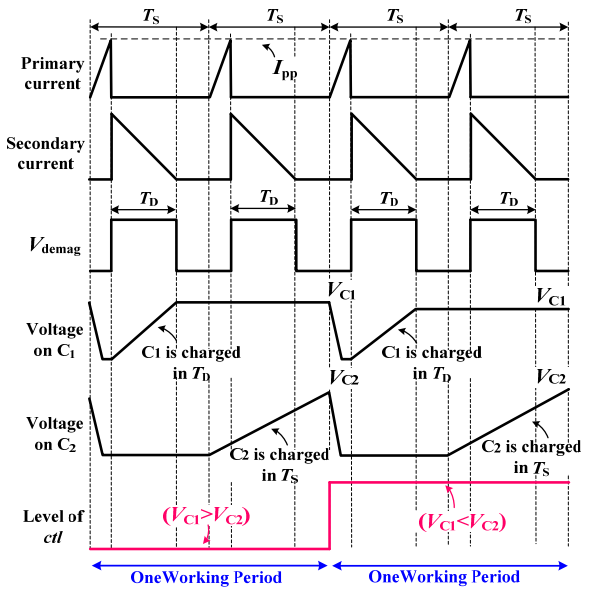


Fig. 5. Working process of the control circuit.

released. In Fig. 5, C_1 and C_2 are discharged quickly through M_{12} and M_{13} when V_5 is at a high level before the demagnetization in the first switching period.

2) Charge Pump Circuit: The charge pump is shown in Fig. 6. According to the output result of the control circuit, the charge pump offers the control voltage V_{ctl}, which is converted to the OSC charging current adjusting current, to improve or reduce the charging current of the OSC, for adjusting the switching frequency.

In Fig. 6, *en*1 (from the CC controller) and *en*2 (from the compensation starting delay circuit) are the active-low enable signals for the compensation module. The signal *ctl* (the output of the control circuit) is the input signal, and V_{ctl} is the output voltage.

Suppose the signal *ctl* is at a low level, M_{18} is in the ON state and M_{19} is OFF. The capacitor C_3 is charged by I_4 through the current mirror. At this moment, the voltage V_{ctl} is ramping up slowly. On the other hand, if *ctl* at a high level, M_{18} is in the OFF state and M_{19} is ON, the charge on C_3 is released by I_4 through the current mirror. As a result, V_{ctl} begins to ramp down.

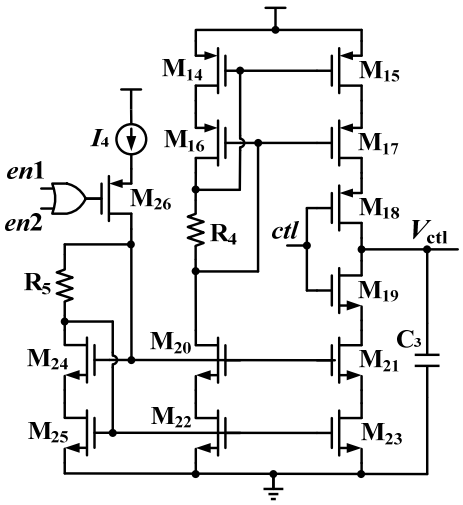


Fig. 6. Design implementation of charge pump circuit.

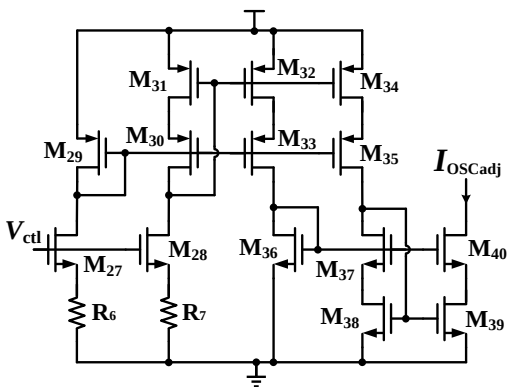


Fig. 7. Design implementation of V/I converter.

3) Voltage to Current Converter: The voltage to the current (V/I) converter receives a control voltage from the charge pump and regulates the switching frequency by adjusting the OSC charging current, to achieve a constant product of T_D and F_S. Fig. 7 shows the converter circuit.

In the circuit in Fig. 7, M_{27} and R_6 are identical to M_{28} and R_7, when converting V_{ctl} to the current which is in proportion with V_{ctl}. Then, this current is transported to the output I_{OSCadj} by the current mirror. I_{OSCadj} makes a fine regulation to I_{OSC}, which causes the switching frequency to vary with the demagnetization time. An unchanged product of T_D and F_S can be achieved after several working periods. Thus, a constant output current unrelated to the primary inductance is obtained.

Six working periods of the compensation adjustment are shown in Fig. 8, where the level of *ctl* is decided by T_D and $1/2T_S$. It can be seen that I_{OSCadj} increases with V_{ctl} in one working period while *ctl* is low and that it decreases while *ctl* is high. The switching frequency can be regulated well by the adjusting circuit.

4) Compensation Starting Delay Circuit: According to the above analysis, the inductance compensation adjustment is realized by moderately reducing the OSC charging current.

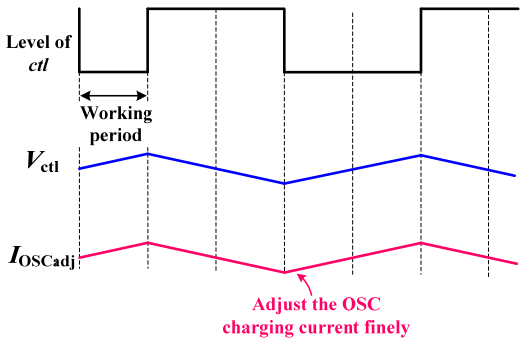


Fig. 8. Key waveform of inductance compensation adjustment.

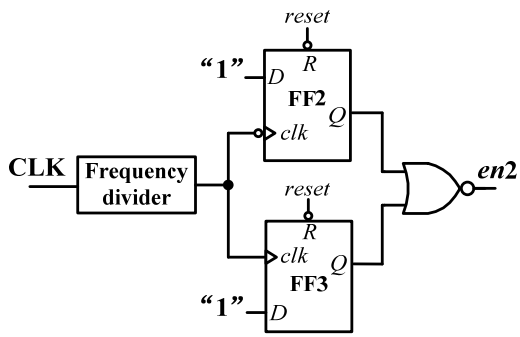


Fig. 9. Compensation starting delay circuit.

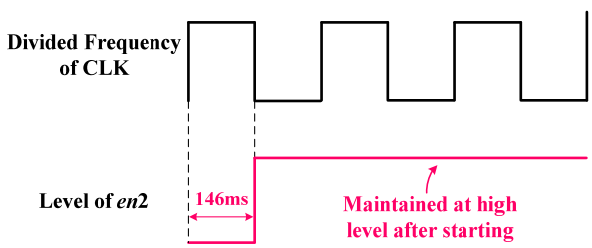


Fig. 10. Working process of the starting delay circuit.

Hence, in the start-up process of the system, the compensation module may decrease the switching frequency, which makes the CC controller start slowly. In order to avoid this problem, the operation of the compensation circuit should be delayed until after the system has completely started.

A compensation starting delay circuit is adopted in the inductance compensation module. Its function is to lock the compensation circuit at the beginning of the system's start-up and to enable it when the output current becomes relatively stable. As shown in Fig. 9, the circuit consists of a 4096 times frequency divider, a NOR gate, a falling-edge triggered D flip-flop *FF*2 and a rising-edge triggered D flip-flop *FF*3.

In Fig. 9, the output *Q* of the two D flip-flops are both reset to low levels by a transient low level pulse when the circuit just powered on. Since the start-up frequency is about 14kHz, a pulse with a period of about 292ms can be obtained by dividing the frequency of the CLK 4096 times. This signal is about to switch after 146ms from when the system starts. The two D flip-flops detect the rising or falling edges at this

moment. The signal *en*2 switches to high detecting the edge. Thus, the starting delay circuit does not unlock the compensation function until 146ms later after the start-up of the system. The working process of the starting delay circuit can be seen in Fig. 10.

III. Experimental Results

A. Layout Design of the Control IC

The proposed AC-DC converter is implemented in a TSMC 0.35μm 5V/40V BCD process and the area is 904×920μm^2, as is shown in Fig. 11. The key modules are marked in this photograph. The designed PCB is shown in the Fig. 12. Its size is about 5.9cm×3.4cm.

B. Test Results of the Proposed Control Chip

As shown in Fig. 1, the proposed AC-DC controller adopts the PSR flyback topology. The key components and parameters of the circuit are listed in Table I.

The related waveforms of the circuit operating in the CC mode are shown in Fig. 13. The input voltages are 90Vac/60Hz and 264Vac/50Hz, and the output voltages are 7V and 10V. The first curve from top to bottom is the output current, I_o; the second is the sampled voltage from the auxiliary winding, V_{INV}; the third is the sampled voltage across the primary current sense resistor, V_{CS}.

According to Fig. 13, the maximum of V_{CS} is fixed at 900mV, which indicates that the primary peak current I_{pp} is an unchanged value. The demagnetization time T_D is nearly equal to half of a switching period T_S. The output current in every figure is almost 1.1A, where the deviation is less than ±3%. The test results are in accordance with the analysis based on eq. (6).

Fig. 14 depicts the curves of the output current I_o when the output load voltage varies from 5V to 12V, under a 90Vac/60Hz-input and a 264Vac/50Hz-input, respectively. It is shown that the output current is kept constant at about 1.1A and that the deviation is less than ±3%.

In order to demonstrate the validity of the inductance compensation module, the transformer with a 0.8mH primary inductance on the demo board is substituted by other transformers with 0.7mH and 0.9mH primary inductances. Fig. 15 shows the output current with the different primary inductors when the input voltage is 220Vac/50Hz.

According to the curve drawn in Fig. 15, the primary inductance varies by over 10%. However, the output current can be kept constant and the variation is within ±1%. Since there exists a deviation in the conversion efficiency of the transformers, a variation of the output current is inevitable. This indicates that the inductance compensation module reduces the negative impact of the tolerance of the primary inductance.

The system efficiency in the CC mode is tested and depicted in Fig. 16, when input voltage is 90V/60Hz and

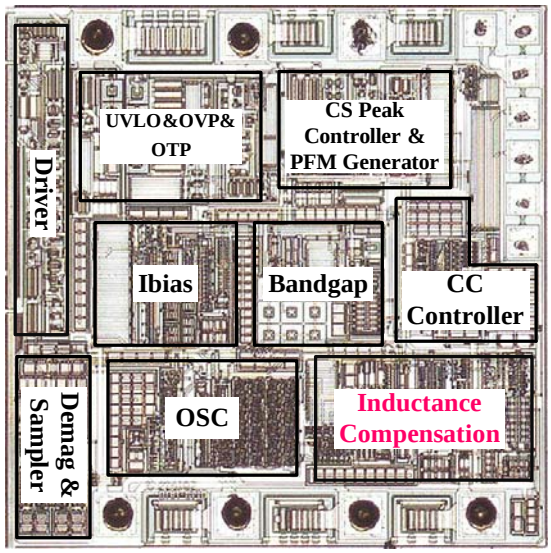


Fig. 11. Photograph of the implemented chip.

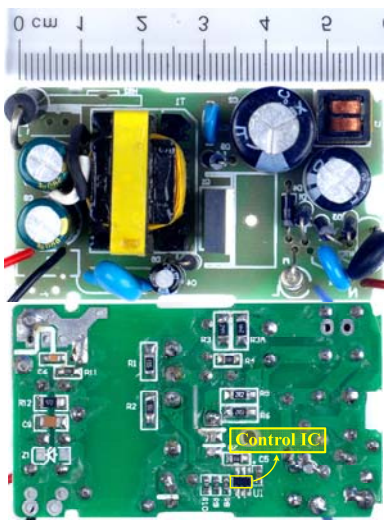
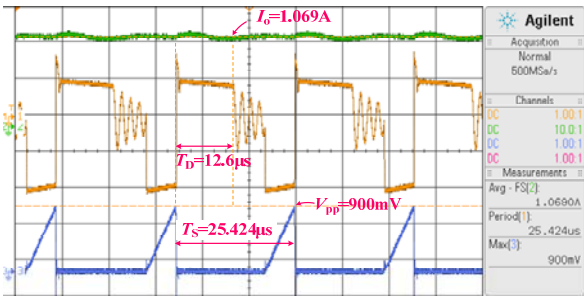


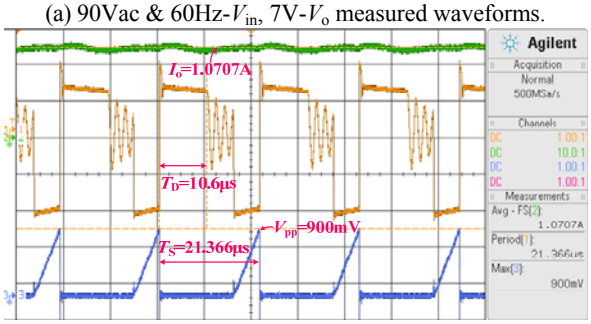
Fig. 12. Photograph of the fabricated PCB.

TABLE I
Key Components and Parameters

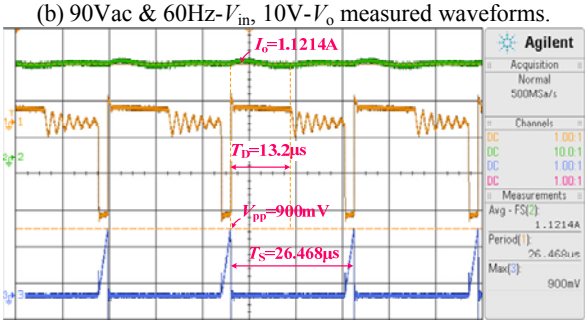
Components	Symbol	Value or Specification
Brige rectifier	BD	1N4007
Primary-side inductance	L_p	0.8mH
Transformer core	T	EE22
Power switch	M_1	2N60
Transformer turn's ratio	$N_P/N_S/N_{AUX}$	72/11/32
Pull-up resistor	R_1	30KΩ
Pull-down resistor	R_2	3.7KΩ
Auxiliary-side Freewheel diode	D_1	FR107
Primary current sense resistor	R_{CS}	1.05Ω
Output capacitor	C_o	900μF
Secondary-side Freewheel diode	D_o	SR3100



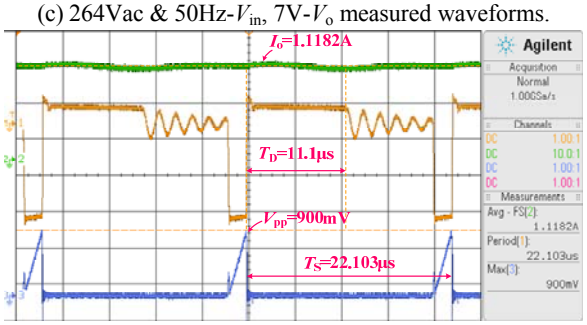
(a) 90Vac & 60Hz-V_{in}, 7V-V_o measured waveforms.



(b) 90Vac & 60Hz-V_{in}, 10V-V_o measured waveforms.



(c) 264Vac & 50Hz-V_{in}, 7V-V_o measured waveforms.



(d) 264Vac & 50Hz-V_{in}, 10V-V_o measured waveforms.

Fig. 13. Test results of output current with different load voltages. Top trace: I_o; second trace: V_{INV}; third trace: V_{CS}.

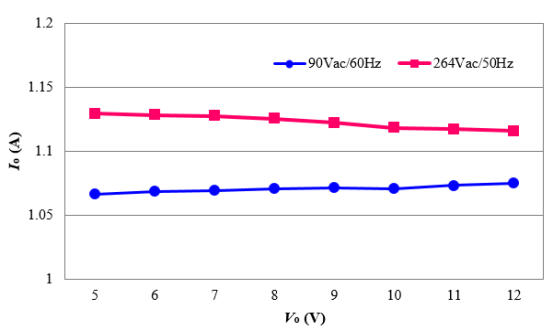


Fig. 14. Measured I_o curves versus V_o under 90Vac & 60Hz-input and 264Vac & 50Hz-input.

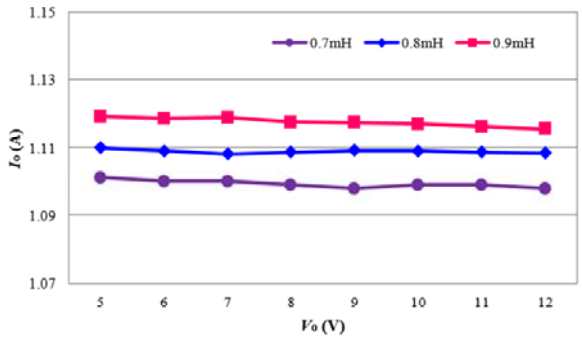


Fig. 15. Measured I_o curves versus V_o with Lp =0.7mH, 0.8mH, 0.9mH under 220Vac & 50Hz-input.

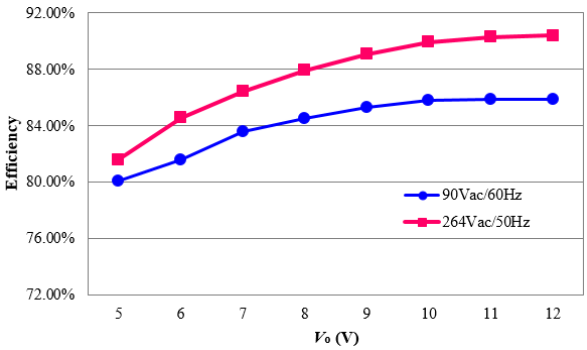


Fig. 16. Measured efficiency versus V_o under 90Vac & 60Hz-input and 264Vac & 50Hz-input.

TABLE II
PERFORMANCE INDEX

Parameters	Value
AC input voltage	90~264 Vac
AC input frequency	47~63Hz
Output current	1.1A
Max output voltage	12V
Max switching frequency	55kHz
System efficiency	>80%
Deviation of output current	<±3%
Variation of output current with Lp varying by 10%	<±1%

264V/50Hz, respectively. Obviously, the efficiency under a low input voltage is lower than that a under high input voltage. The minimum of the system efficiency can reach about 80%.

The performance of the proposed chip is listed in table 2. It can be seen that the accuracy of the output current is very high and that adopting the proposed inductance compensation technology produces a good effect.

IV. CONCLUSION

A PSR constant current AC-DC converter operating in the PFM mode with inductance compensation is designed and implemented. The primary-side regulation structure omits the

need for an optical-coupler or a precise voltage source to reduce the size and cost of the converter. The inductance compensation function eliminates the influence caused by the inductance tolerance of the primary windings, and a constant output current can be acquired. In order to verify the proposed compensation technology, a control chip adopting this method has been fabricated in the TSMC 0.35μm 5V/40V BCD process and a 12V/1.1A prototype has been built. Experimental results show that the deviation of the output current is within ±3%, and that the variation of the output current is less than 1%, when the variation of the primary inductance is ±10%.

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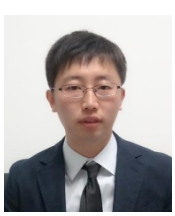

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