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An Active Voltage Doubling Rectifier with Unbalanced-Biased Comparators for Piezoelectric Energy Harvesters

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Abstract

For wearable health monitoring systems, a fundamental problem is the limited space for storing energy, which can be translated into a short operational life. In this paper, a highly efficient active voltage doubling rectifier with a wide input range for micro-piezoelectric energy harvesting systems is proposed. To obtain a higher output voltage, the Dickson charge pump topology is chosen in this design. By replacing the passive diodes with unbalanced-biased comparator-controlled active counterparts, the proposed rectifier minimizes the voltage losses along the conduction path and solves the reverse leakage problem caused by conventional comparator-controlled active diodes. To improve the rectifier input voltage sensitivity and decrease the minimum operational input voltage, two low power common-gate comparators are introduced in the proposed design. To keep the comparator from oscillating, a positive feedback loop formed by the capacitor C is added to it. Based on the SMIC 0.18-μm standard CMOS process, the proposed rectifier is simulated and implemented. The area of the whole chip is 0.91×0.97 mm^2, while the rectifier core occupies only 13% of this area. The measured results show that the proposed rectifier can operate properly with input amplitudes ranging from 0.2 to 1.0V and with frequencies ranging from 20 to 3000 Hz. The proposed rectifier can achieve a 92.5% power conversion efficiency (PCE) with input amplitudes equal to 0.6 V at 200 Hz. The voltage conversion efficiency (VCE) is around 93% for input amplitudes greater than 0.3 V and load resistances larger than 20kΩ.

Key words: Active diode, Common-gate comparator, Piezoelectric energy harvester, Reverse leakage current, Voltage doubling, Unbalanced-biased

I. INTRODUCTION

Due to the difficulty and cost of replacing the batteries in wireless body area network (WBAN) devices [1], harvesting energy from the environment (ultrasonic [2], thermal [3], vibration [4], solar [5], etc.) to self-power these devices is gradually becoming the most promising solution. Among alternative energy sources in the environment, piezoelectric vibrations are the most attractive since they are steady and have a large power density [6]. An AC to DC converter is required to extract the available power from a piezoelectric transducer in order to power an electronic device.

For instance, the output voltage amplitude range of a piezoelectric transducer generated by human motion can be from tens of millivolts to a thousand millivolts [7]. Therefore, the rectifier in this work should have a low input voltage threshold, a wide input voltage range and a high power conversion efficiency.

Active full-wave rectifiers are widely applied as interface circuits for piezoelectric energy harvesting. Therefore, a MOS switch is driven by a logic circuit which controls the 'on' and 'off' states according to the voltage difference across the switch itself [8]. The two-stage rectifier presented in [8], which consists of a negative voltage converter (NVC) and an active diode, can achieves about 95% power conversion efficiency (PCE) with input voltages ranging from 1.25 to 3.75 V. Niu D et al. [9] make use of a bulk-driven comparator to improve rectifier sensitivity. This made it

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possible to achieve an input voltage of 0.28 V and a PCE around 90%. To further reduce the rectifier sensitivity, Yang Z et al. [10] took advantage of an input-powered bulk-driven comparator in the active diode to achieve a rectifier sensitivity of 0.15 V. However, lowering the input voltage amplitude in [9] and [10] is done at the expense of reducing the input voltage range. The input voltage range is 0.28 to 0.7 V in [9] and 0.15 to 0.5 V in [10]. To minimize the switch on-resistance, very large transistors are needed in the NVC, which means a larger die area and cost. In addition, the delay time and offset voltage introduced by the comparator in the active diode [8]-[10] causes a reverse leakage current, which in turn significantly reduces the PCE.

Based on the cross-coupled active full-bridge (CCAF) structure, Lee H M et al. [11] present a novel offset-controlled comparator to minimize the reverse leakage current. The rectifier achieves a PCE equal to 80.5% while operating with an input frequency of 13.56 MHz and an amplitude of 3.8V. Based on the same CCAF structure, Sun Y et al. [12] apply an operational amplifier-controlled active diode and a switch in parallel with a transducer to improve the PCE by solving the dc-offset issue of the comparator-controlled active diode. This rectifier shows a PCE of 90% when operated with a 200 Hz sinusoidal voltage having an amplitude equal to 1.5 V and a resistive load of 95 kΩ. Although the rectifiers in [8], [11], and [12] achieve a higher PCE, the minimum required input voltage amplitude is too high (larger than 1.0 V) to operate the rectifier in a micro-energy environment. The minimum input voltage amplitude is lower in [9] and [10]. This is achieved at the expense of reducing the input voltage range. The vibration energy produced by the human motion is the main energy source for the wearable piezoelectric energy harvester, and the output voltage amplitude is in the range from 0.3 to 1.2 V [7]. Obviously, the above mentioned rectifiers are not suitable for wearable biomedical applications. Moreover, the reported rectifiers provide an output DC voltage that is lower than the maximum input AC amplitude. In [13] the output voltage is insufficient to supply energy to a useful load, especially when the maximum input amplitude is small.

This paper proposes a high efficient full-wave active rectifier based on a single stage Villard doubler with a wide input voltage range. The sensitivity of the rectifier can be as low as 200 mV by employing common-gate comparators with unbalanced bias currents as a part of the active diode, which eliminates the reverse leakage current. The power consumption of the unbalanced-biased comparators (UBCs) can be optimized leading to optimal VCE and PCE. The rest of this paper is organized as follows: section II introduces the basic principle of the Dickson charge pump and comparator-controlled active diode; section III describes the circuit design of the proposed rectifier in detail; simulated and measured results based on the SMIC 0.18-μm standard

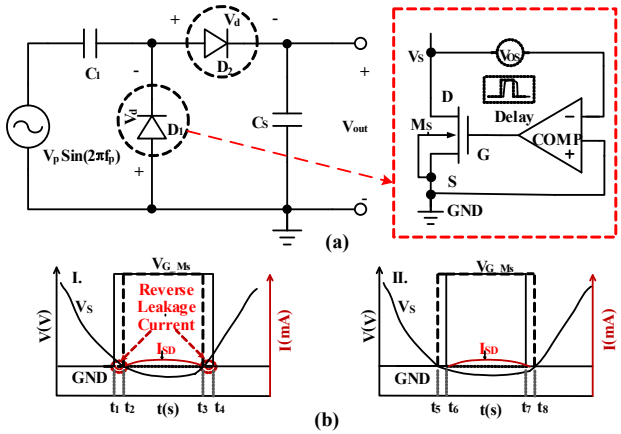


Fig. 1. (a) Conventional one-stage Dickson charge pump rectifier and the model of conventional comparator-controlled active diode with non-ideal Delay and offset V_{OS}. (b) The influence of mismatch (I) $V_{OS}>0$ (II)$V_{OS}<0$.

CMOS process are provided in section IV. Finally, some conclusions are given in section V.

II. Basic Structure and Principle

A basic circuit diagram of a one stage Dickson charge-pump rectifier is shown in Fig. 1(a), which consists of diodes D_1, D_2 and capacitors C_1, C_S. The forward voltage drop of diodes causes voltage loss in this conduction path, which seriously reduces the VCE and PCE of the rectifier. To cut down voltage drop and improve the performance of the rectifier, the comparator-controlled active diode, as shown in the dashed box in Fig. 1(a), is widely used to replace the passive diode in conventional Dickson charge pump rectifiers. The active diode consists of an NMOS switch and a control comparator [14]. The source and drain of the switch are connected to the non-inverting and inverting input terminals of the comparator, and are equivalent to the cathode and anode terminals of an ideal diode, respectively. The switches operate in the linear region during the on-state and a large size switch is chosen. Therefore, V_d is an extremely low value for the active diode. The output voltage of the charge-pump rectifier can be given as:

$$V_{out} = V_p - V_d + V_p - V_d = 2(V_p - V_d) \approx 2V_p \quad (1)$$

However, a signal delay or mismatch of the comparator may lead to a reverse leakage current in the charge pump rectifier, as shown in Fig. 1(a), which can significantly reduce the efficiency of rectifier [11], [12]. In Fig. 1(a), the delay represents the signal delay of the comparator COMP which is mainly caused by the parasitic capacitance of the large size switch M_S. In addition, V_{OS} is an offset voltage induced by random errors in the process.

Due to the requirements of a large output power and a small voltage drop, a large-size switch transistor M_S should be chosen. Therefore, the parasitical gate-capacitance of M_S

increases unavoidably. As a result, the time for charging or discharging this capacitance will be increased correspondingly.

Offset voltage V_{OS} is caused by a mismatch or another random error in the process [15]. As shown in Fig. 1(b), the output of an ideal comparator is illustrated as a dotted line, which turns the NMOS switch M_S on once V_S lower than GND (t_2 or t_5) and turns it off immediately when V_S is higher than GND (t_3 or t_8). When $V_{OS}=V_{S(t1)}-V_{S(t2)}=V_{S(t4)}-V_{S(t3)}>0$, as shown in Fig. 1(b)(I), M_S is turned on at t_1 and turned off at t_4, for the effect of V_{OS}, instead of t_2 and t_3. Although V_S is higher than GND during the phase of t_1-t_2, switch M_S is still turned on and the conduction path is formed for the reverse current I_{SD} from the drain to the source of M_S. Similarly, when $V_{OS}=V_{S(t6)}-V_{S(t5)}=V_{S(t7)}-V_{S(t8)}<0$, as shown in Fig. 1 (b)(II), M_S is turned on at t_6 and turned off at t_7, instead of t_5 and t_8. However, in this case, the negative offset voltage V_{OS} does not lead the reverse current through the switch M_S. Instead it makes the voltage drop across it increase. Therefore, when the offset voltage of the comparator $V_{OS}>0$, the terrible influences of the signal delay V_{Delay} will be superimposed with the effects of the offset voltage V_{OS}, which is the worst case in many applications. However, if $V_{OS}<0$, the influences of V_{Delay} can be cancelled out by the offset voltage V_{OS}. Generally, the equivalent offset voltage V_{Delay} is larger than the voltage V_{OS} especially for a high input frequency [12]. Therefore, even if the offset voltage $V_{OS}<0$ is taken into consideration, the signal delay of the comparator Delay still causes the reverse leakage problem, which decreases the efficiency of the rectifier.

In this paper, a built-in offset voltage ΔV is introduced into the comparator by the unbalanced bias schematic to compensate V_{Delay} and V_{OS}. Considering the worst case, in order to prevent a reverse leakage current as much as possible, the built-in offset voltage ΔV should be chosen appropriately and is set as $|\Delta V|\geq|V_{Delay}|+|V_{OS}|$ in this design. If the built-in offset voltage ΔV over compensates the reverse leakage, the voltage drop across M_S increases and the VCE of the rectifier decreases correspondingly. However, a large M_S is designed to meet the requirements of a large output power and a small voltage drop. Once the reverse leakage conduction path is formed, there will be a large reverse current distracting the energy stored in the capacitor C_S, which lead to drastic reductions in the PCE. Therefore, the performance of the PCE has been paid more attention to in this design example.

III. Proposed Active Voltage-Doubling Rectifier

Efficiency is one of the most important performance indicators for a rectifier, and it is influenced by three factors: 1) the power consumption dissipated by the on-resistance of the MOSFET switch in an active diode; 2) the power consumption dissipated by the active part of a rectifier (comparators and their bias circuits); 3) the power loss caused by the reverse leakage current mentioned in section II. In addition, the input voltage range of a rectifier should be as wide as possible to harvest more vibration energy with different amplitudes. Taking these factors into consideration, a high efficiency, wide input range active voltage doubling rectifier with unbalanced-biased comparators is proposed in this paper.

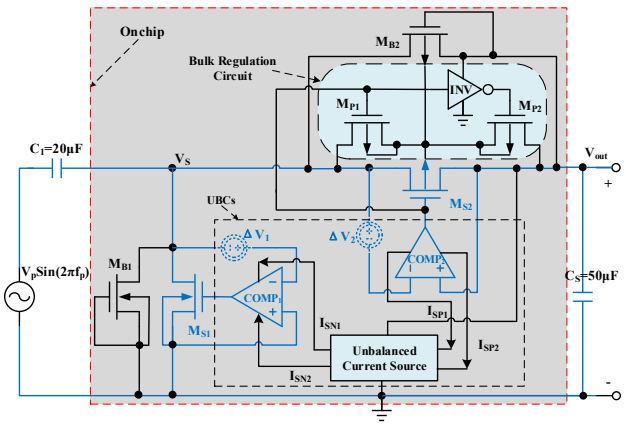


Fig. 2. Proposed active voltage doubling rectifier with UBCs.

A. The Proposed Active Voltage Doubling Rectifier

A schematic of the proposed active voltage doubling rectifier is shown in Fig. 2. The main schematic topology of the proposed active rectifier is based on an approach first presented in [16]. The proposed rectifier mainly consists of five parts: unbalanced-biased comparators (UBCs) $COMP_1$ and $COMP_2$, power transistors M_{S1} and M_{S2}, bypass transistors M_{B1} and M_{B2}, off-chip capacitors C_1 and C_S, and a bulk regulation circuit. The NMOS M_{S1} and the comparator $COMP_1$ constitute the active diode D_1, and the PMOS M_{S2} and the comparator $COMP_2$ constitute the active diode D_2. Both M_{S1} and M_{S2} operate in the linear region. Therefore, increasing the size of M_{S1} and M_{S2} leads to smaller on-resistances of the switches and a drain-source voltage drop, thereby maximizing the voltage conversion efficiency. ΔV_1 and ΔV_2 are the built-in offset voltages of the UBCs, which are generated by the unbalanced bias currents I_{SN1}, I_{SN2} and I_{SP1}, I_{SP2}, respectively. As previous analysis, a build-in offset voltage can prevent the reverse current induced by the random offset and delay of the comparator. To reduce the power consumption dissipated by the active part of the rectifier, the common-gate comparators $COMP_1$ and $COMP_2$ are biased in the subthreshold regions. As a result, they only dissipate several hundred nano-amperes of current. The proposed UBCs enable the rectifier to operate with a low amplitude input and minimize the leakage current to improve the rectifier efficiency by compensating the delay and mismatch.

To reduce the on-state resistor, the power transistors M_{S1} and M_{S2} should always have a large size. In this rectifier, two

bypass diodes M_{B1} and M_{B2} are added in parallel with the switches M_{S1} and M_{S2}, to promote the start-up performance especially in very low input voltage conditions. The bulk regulation circuit aims at preventing the forward bias between the source and body of M_{S2}, which may cause a latch-up. C_1 is a sampling capacitor, and the holding capacitor C_S stores the scavenged piezoelectric energy and delivers power to the rectifier and the load.

B. Design of the Unbalanced-biased Comparator

As analyzed in section II, the mismatch and delay of the comparators can cause performance degeneration of the rectifier. In this paper, an unbalanced-biased approach is adopted in the comparator design to form a built-in voltage difference ΔV [17]-[19] and then to compensate the non-ideal effects of the comparator. Fig. 3 shows a detailed circuit diagram of the proposed unbalanced-biased comparators. Due to the level of their input voltage ranges, $COMP_1$ and $COMP_2$ are symmetrical, and have to be supply compatible and ground compatible. Taking $COMP_1$ for example, the comparator consists of two pairs of common gate input stages (M_1, M_5 and M_2, M_6), a current mirror (M_3, M_4), a common source inverter (M_7, M_8), and a push-pull inverter (M_9, M_{10}). $COMP_1$ and $COMP_2$ are supplied by the output of the rectifier itself. Additionally, a positive feedback loop formed by the capacitor C can prevent the comparator from oscillating. Simulation results indicate that the value of the capacitor C can be set as 0.2pF and the resistor R can be set as 0.5MΩ.

As shown in Fig. 3, I_{SN1} and I_{SN2} are unbalanced current sources, which are mirrored by M_5 and M_6 to generate the unbalanced bias for M_1 and M_2. By setting the biasing current to $I_{SN1}\neq I_{SN2}$, the value of ΔV in the proposed unbalanced-biased comparator can be properly controlled by the difference between I_{SN1} and I_{SN2}. For the power consumption consideration, M_1 and M_2 are biased in the subthreshold, and the subthreshold current is expressed as:

$$I_{sub} = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{2}$$

Where K is W/L of the MOS transistor, $I_0=\mu C_{OX}(\eta\text{-}1)V_T^2$, η is a non-ideal factor which is estimated as a constant parameter equal to 1.14 and 1.40 for the PMOSFET and NMOSFET, respectively [20]. The subthreshold currents I_{SN1} and I_{SN2} flowing through M_1 and M_2 can be expressed as:

$$I_{SN1} = K_1 I_0 \exp\left(\frac{V_{GS1} - V_{TH}}{\eta V_T}\right);\ I_{SN2} = K_2 I_0 \exp\left(\frac{V_{GS2} - V_{TH}}{\eta V_T}\right) \tag{3}$$

The ΔV of $COMP_1$ can be obtained from (3).

$$\Delta V_1 = V_{GS1} - V_{GS2} = \eta V_T \ln\frac{I_{SN1}}{I_{SN2}} \tag{4}$$

As can be seen from (4), the built-in voltage difference mainly depends on the ratio of I_{SN1}/I_{SN2}. Take $I_{SN1}/I_{SN2}=3/4$, by setting the bias circuit properly (discussed in the following section), V_T=26mV and η=1.4 for the NMOS transistor. A negative offset voltage $\Delta V_1\approx$-10.5mV is obtained.

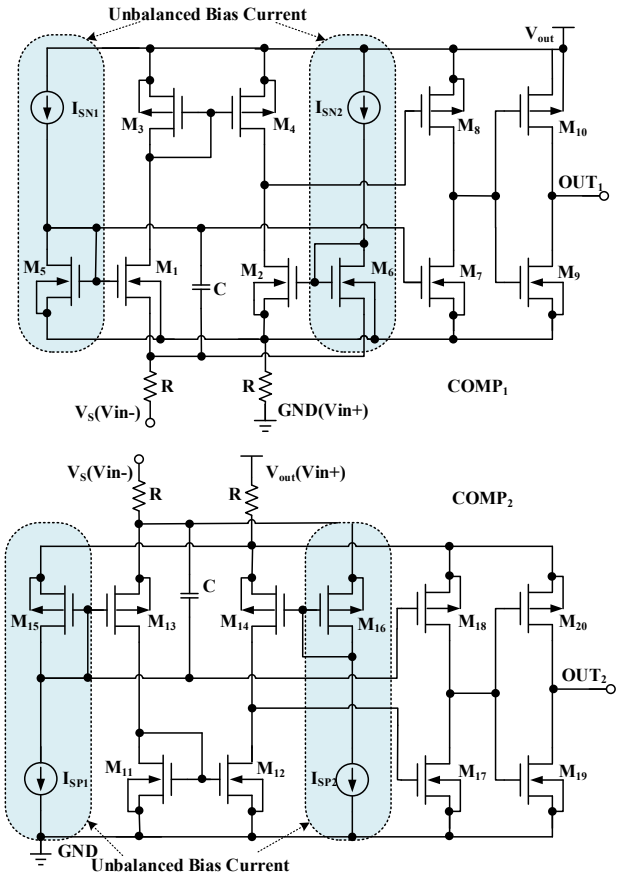


Fig. 3. Circuits of the UBC $COMP_1$ with NMOS input and $COMP_2$ with PMOS input.

The source terminals of the input MOSFET M_1 and bias MOSFET M_6 are connected as the inverted input terminal of $COMP_1$, and those of M_2 and M_5 are connected at the non-inverted input terminal. This structure realizes the push-pull output in the first stage of $COMP_1$, and then minimizes the delay time of the comparator [22]. Two inverters (M_7, M_8 and M_9, M_{10}) are used to increase the output swing and to improve the driving capability of $COMP_1$. The common gate structure is adopted as the input stage of $COMP_1$ to meet the low voltage input demand.

$COMP_1$ and $COMP_2$ are symmetrical. Therefore, in a similar way, by setting the biasing current to $I_{SP1}\neq I_{SP2}$, the built-in offset voltage ΔV_2 of $COMP_2$ can be expressed as (5). Take $I_{SP2}/I_{SP1}=4/3$, V_T=26mV and η=1.14 for the PMOS transistor. A positive offset voltage $\Delta V_2\approx$8.5mV is obtained.

$$\Delta V_2 = V_{SG14} - V_{SG13} = \eta_2 V_T \ln\frac{I_{SP2}}{I_{SP1}} \tag{5}$$

It is impossible for the built-in offset voltage ΔV to completely cancel the non-ideal effect, due to the randomness of the mismatch. However, a slightly larger ΔV is appropriate to minimize the reverse leakage current which is caused by the mismatch and delay of the comparator. It is worth mentioning that an excessive ΔV may lead to a voltage-drop

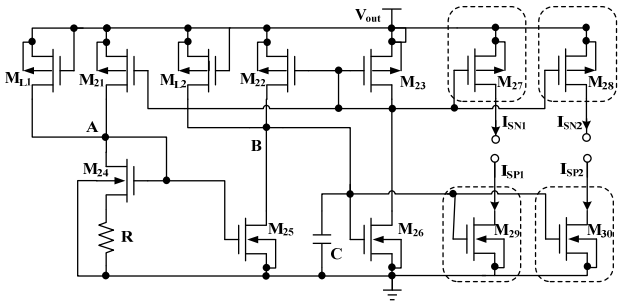


Fig. 4. Supply independent unbalanced current source.

increase of the active switch in the on-state, which can result in a performance degradation of the rectifier.

As shown in section III. A, the proposed rectifier is supplied by an output voltage, which varies widely in the start-up phase due to the wide input voltage range. In order to ensure the accuracy of the built-in offset voltage ΔV, the unbalanced bias currents of the comparators should be independent from the supply voltage. On the other hand, since the proposed rectifier is powered only by harvested energy, its own power dissipation should be as low as possible to deliver more energy to the load. Therefore, the bias circuits should keep the current consumption constant as the supply voltage increases. The proposed supply independent, unbalanced bias circuit is shown in Fig. 4. M_{21}-M_{23} operating in the subthreshold constitute the current mirrors. Therefore, the currents flowing through M_{24} and M_{25} are the same.

$$K_{24}I_0\exp\left(\frac{V_{GS24}-V_{TH}}{\eta V_T}\right)=K_{25}I_0\exp\left(\frac{V_{GS25}-V_{TH}}{\eta V_T}\right) \quad (6)$$

The current flowing through resistor R is:

$$I_R=\frac{\Delta V_R}{R}=\frac{V_{GS25}-V_{GS24}}{R}=\frac{\eta V_T}{R}\ln\frac{K_{24}}{K_{25}} \quad (7)$$

As shown in (7), this current only depends on the W/L ratio of M_{24} and M_{25} and the resistance of R. It can also be seen that it is independent of the supply voltage. By setting different W/L ratios of M_{27} and M_{28}, the unbalanced bias currents I_{SN1} and I_{SN2} are generated, which are used to bias $COMP_1$. Similarly, the unbalanced bias currents of $COMP_2$ I_{SP1} and I_{SP2} can be obtained by setting different W/L ratios of M_{29} and M_{30}. As shown in (5), the built-in offset voltage of the comparator can be adjusted by changing the W/L ratio of the MOSFETs in the bias circuit. Since the leakage of the body-drain diode was exploited to inject a current into nodes A and B, two dummy MOSFETs M_{L1} and M_{L2}, as shown in Fig. 4, are used to aid the start-up.

C. Bypass Diode and Bulk Regulate Circuit

Under some worst-case conditions, such as process variations with a high threshold and a low operating temperature, the comparator-based active diode may not work properly, especially in the start-up phase. In order to assure a safe and robust start-up of the active diode, two additional bypass MOS diodes (M_{B1} and M_{B2}) in parallel with the active diodes (M_{S1} and M_{S2}) can be used. The bypass MOS diodes ensure that there is a startup-aid current flowing through it, and minimize the setting time of the rectifier. After the active diode starts working, M_{B1} and M_{B2} are no longer operating and are always keep in a high impedance state, which guarantees that there is no reverse leakage current through the bypass diode. To insure a large drain current in a weak positive biased condition, the W/L ratio of M_{B1} and M_{B2} should be relatively large.

In CMOS technologies, the slightly p-doped bulk must always be connected to the lowest potential, and the n-doped well of a PMOS transistor must be connected to the highest potential. Then, the PN junctions are reversed biased and no leakage current or latch-up occurs. However, during the start-up phase, the source and drain of the PMOS M_{S2} are floating and alternating, which makes it unclear how to connect its substrate. In consideration of performance, a dynamic bulk regulation circuit is added to make sure that the bulk of the PMOS M_{S2} is always connected to the highest potential between V_S and V_{out}. The W/L ratio of the switch M_{P1} (and M_{P2}) is small. Therefore, it can be directly controlled by the output of the comparator.

IV. Results and Discussions

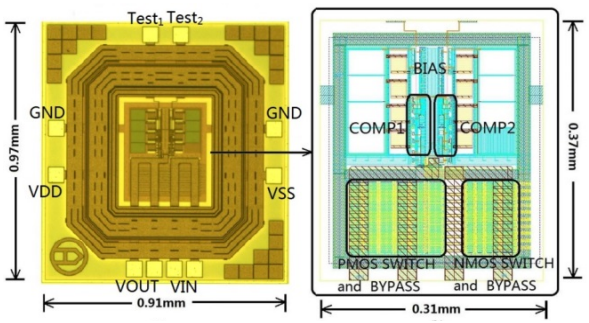
The proposed wide input range active voltage doubling rectifier is implemented and simulated with the SMIC 0.18μm standard CMOS process. Table I shows the size of all of the transistors in the proposed rectifier. The integral layout of the proposed rectifier is shown in Fig. 5(a), and Fig. 5(b) presents more layout details of the core circuit. The area cost of the whole rectifier chip and the core circuit are $0.91\times0.97mm^2$ and $0.31\times0.37mm^2$, respectively. All of the main switches are surrounded by guard rings to isolate them from adjacent cells. Pads with electro-static discharge (ESD) protection are used to feed the input source signal into the chip. The ESD supply voltages (VDD and VSS) are directly accessible. The parasitic parameters of the rectifier are extracted to simulate the post-layout for more accurate results. In addition, some measurement results are given in the following part of this section as well.

To verify the performance of the proposed active voltage doubling rectifier, the PCB Demo board is designed as shown in Fig. 6(a). A sinusoidal signal generator is connected to the input of the proposed rectifier, and the output is connected to an oscilloscope. The experimental platform is shown in Fig.6 (b).

Fig. 7(a) shows the waveforms of the output voltage under different input signal amplitudes with an input AC frequency of 200Hz. The range of the input amplitude can be from 0.2V to 1.0V, and the corresponding stable output DC voltage range is about 0.4 to 2.0V, which is double that of the input voltage amplitude. The minimum input amplitude is as low as

TABLE I
SIZE OF ALL TRANSISTORS IN THE PROPOSED RECTIFIER

Device	Size	Device	Size
M_{S1}	1000μm/0.2μm	M_1, M_2, M_5, M_6, M_{11}, M_{12}	8μm/1μm
M_{S2}	2000μm/0.2μm	M_3, M_4, M_{13}, M_{14}, M_{15}, M_{16}	32μm/1μm
M_{B1}	5000μm/0.2μm	M_9, M_{19}	4μm/0.2μm
M_{B2}	10000μm/0.2μm	M_{10}, M_{20}	16μm/0.2μm
M_{P1}, M_{P2}	0.5μm/0.2μm	M_{21}, M_{22}, M_{23}, M_{29}, M_{30}, M_{L1}, M_{L2}	12μm/3μm
M_7, M_{17}	16μm/1μm	M_{24}	24μm/3μm
M_8, M_{18}	64μm/1μm	M_{25}, M_{26}, M_{27}, M_{28}	3μm/3μm



(a) (b)

Fig. 5. (a) Integral layout of proposed rectifier. (b) Core circuit layout of proposed rectifier.

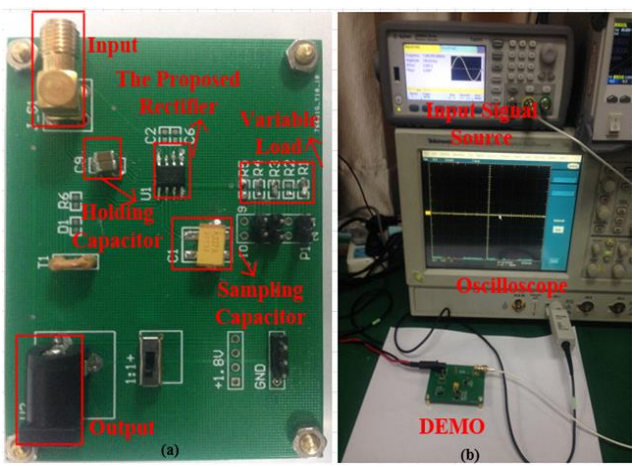


Fig. 6. (a) The PE harvester Demo. (b) The experimental platform.

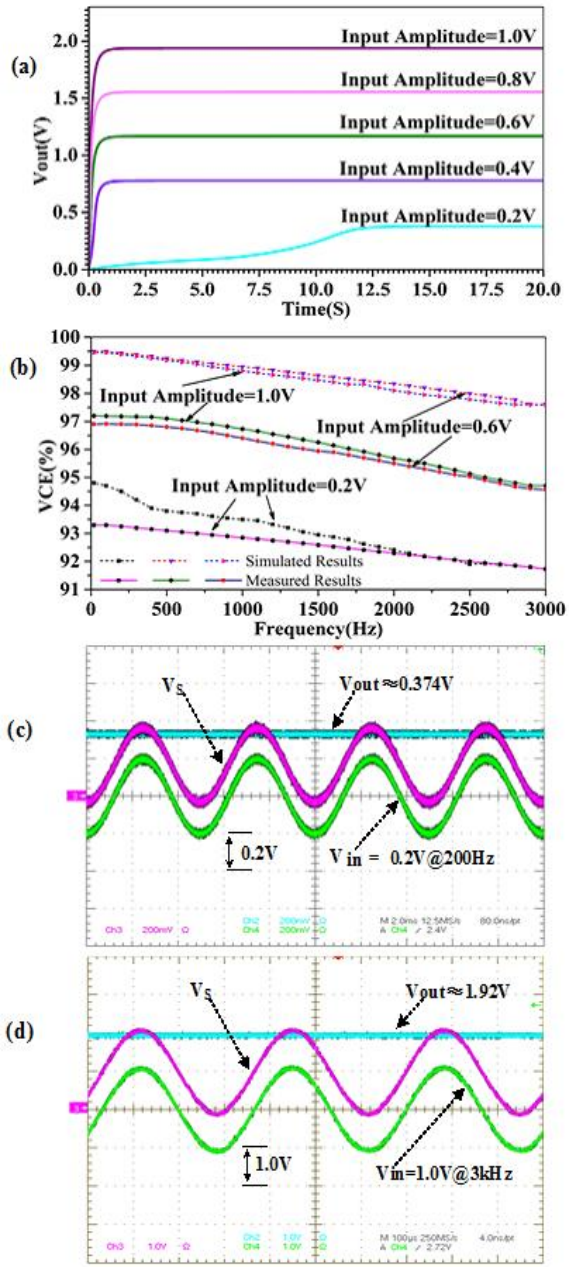


Fig. 7. (a) Output voltage with different input signal amplitudes (b) VCE versus input signal frequency. Measured voltages of the proposed rectifier with (c) V_{in}=0.2V@200Hz. (d) V_{in}=1.0V@3kHz.

0.2V. However, the setup time becomes as long as 12.5s under this condition. Fig. 7(b) demonstrates the effects of different input frequencies and amplitudes on the voltage conversion efficiencies of the rectifier with a 100kΩ load. As shown in Fig. 7(b), when the amplitude of the input signal is 0.2V, the switch transistors M_{S1} and M_{S2} operates in the subthreshold region. Therefore, the on-resistance of these switches increases, which causes a significant decrease in the VCE. In addition, when the amplitude of the input signal is 0.6 or 1.0V, the two switch transistors operate in the linear region, and the measured results of the VCE are above 95% with the frequency of the input signal ranging from 20 to 3000Hz. In addition, as can be seen from Fig. 7(b), the VCE decreases slightly with an increase of the input signal frequency. This is based on the fact that the impact of the delay on the switches is worse when the signal cycle becomes smaller. The measured output voltage V_{out}, V_S of the proposed rectifier and the input AC signal V_{in} at different frequency are shown in Fig. 7(c) and 7(d), respectively. With $|V_{in}|$=0.2V and a 20kΩ load resistance, the proposed rectifier provides a V_{out} of about 0.374V at a frequency of 200Hz and 1.92V at a frequency of 3kHz, respectively.

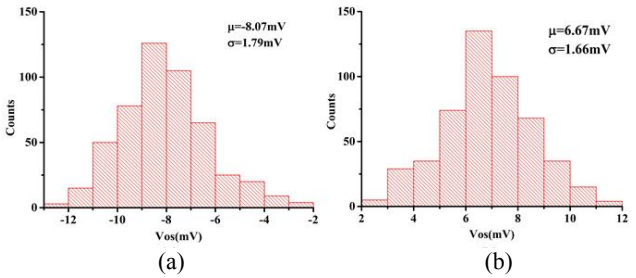


Fig. 8. Monte Carlo simulation of the offset voltages of the comparators with UBS. (a) $COMP_1$. (b) $COMP_2$.

Fig. 8(a) and 8(b) presents the simulation results of 500 Monte Carlo iterations of the two proposed comparators with the unbalanced biasing scheme. As shown in Fig. 8(a), the mean value (μ) of the offset voltage is -8.07mV, with a standard deviation (σ) of 1.79mV for the proposed comparator $COMP_1$. These two parameter values are 6.76mV and 1.66mV for the comparator $COMP_2$, as shown in Fig. 8 (b). Even with a 3σ variation (99.7%), the possible spread of the offset voltages in two comparators is sufficiently small. Therefore, the build-in offset voltage ΔV does not change its sign. As mentioned in section II, the correct sign of the voltage ΔV can effectively reduce the reverse leakage current, and then improve the PCE of the proposed rectifier.

As shown in Fig. 9(a), a rectifier without unbalanced biased comparators presents a reverse leakage in both the negative and positive half circle of the input signal. As a result, this reverse leakage current problem severely degrades the conversion efficiency of the rectifier. Fig. 9(b) presents a waveform of the proposed rectifier with unbalanced biased comparators. As can be seen in Fig.9(b), the switches M_{S1} and M_{S2} are turned off opportunely, and there is seldom a reverse leakage current. The output of $COMP_1$, $COMP_2$ and the voltage of V_S are measured and shown in Fig.9(c) with $|V_{in}|$=0.6V at a frequency of 200Hz. It can be seen from the output voltage waveforms of $COMP_1$ and $COMP_2$ that the two comparators turn off timely to reduce the reverse leakage current. As a single stage Dickson charge pump rectifier, the VCE of the proposed rectifier is given by:

$$\eta_v = \frac{V_{out}}{2V_p} \times 100\% \tag{8}$$

Where V_{out} is the stable output DC voltage, and V_p is the amplitude of the input signal. The PCE of the rectifier is given by (9), where P_{load} is the output power consumed on the load resistor R_L, P_{active} is the power dissipated by the active parts of the rectifier (comparators and bias circuit), and P_{loss} is the total loss power dominated mainly by the R_{on} loss of the switches.

$$\eta_p = \frac{P_{load}}{P_{load} + P_{loss} + P_{active}} \times 100\% \tag{9}$$

Fig. 10(a) and 10(b) show the effect of the unbalanced biased comparators on the power conversion efficiency and

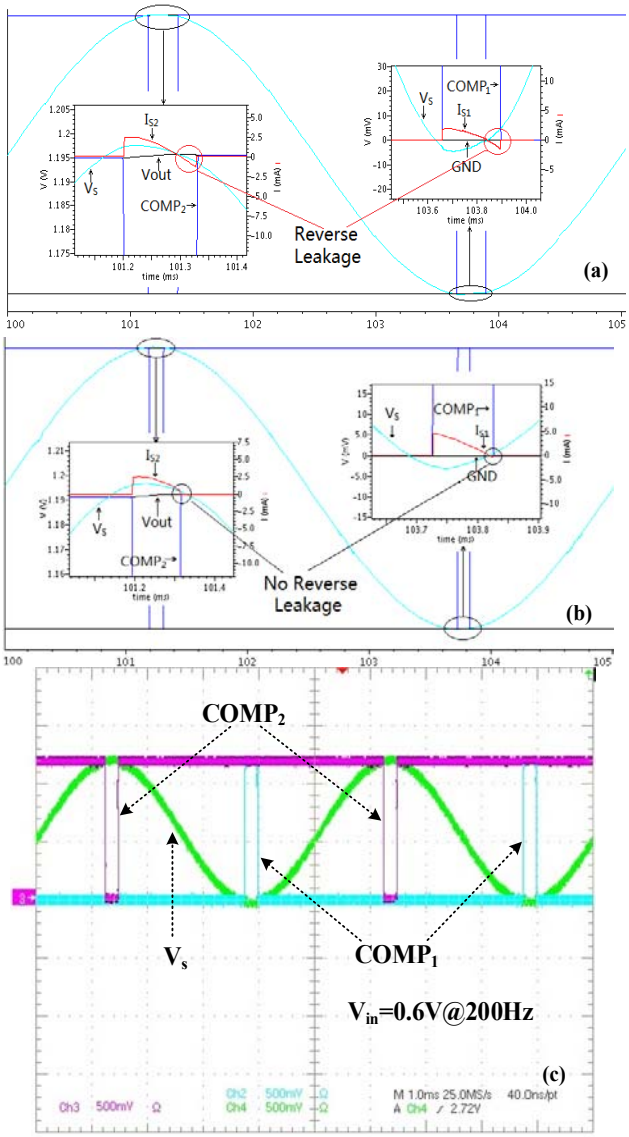


Fig. 9. (a) Post-simulated waveforms of the reverse leakage current in Common rectifier without UBCs. (b) Post simulated waveforms of the reverse leakage current in proposed rectifier with UBCs. (c) Measured voltages of proposed rectifier with UBCs.

voltage conversion efficiency of rectifiers with different loads. As a typical description, the input source is set as a sinusoidal signal at a frequency of 1000Hz. As can be seen from Fig. 10(a), the measured peak PCE of the proposed rectifier reaches 92.5% with an input amplitude of 0.6V and a load resistance of 20kΩ. For two different load conditions and input amplitudes ranging from 0.2 to 1.0V, when compared with the simulated results of a rectifier without the UBCs, the measured PCE of the proposed rectifier in improved by 12%-14%. With the load resistance increasing, the power consumption on the load of P load decreases, and the PCE of the rectifier decreases as illustrated in (9). It is worth noting that the switches M_{S1} and M_{S2} operate in the subthreshold region when the input voltage amplitude is less than 0.3V.

TABLE II
PERFORMANCE AND COMPARISON WITH PRIOR ART

	Technology	Input Range (V)	Vout/Vin	Peak Power Efficiency	Frequency (Hz)
[8]	0.35μm	1.25-3.75	---	95% @R_L=50kΩ	1-100K
[9]	0.18μm	0.3-0.7	>88%	94% @R_L=40kΩ	10-3K
[10]	0.18μm	0.15-0.5	>80%	90% @R_L=40kΩ	100
[12]	0.18μm	2.8	---	90% @R_L=95kΩ	200
[16]	0.35μm	1.2-2.4	>84%	87% @R_L=100Ω	0.2-1.5M
[17]	0.5μm	0.68-4.8	---	90% @R_L=200kΩ	200
[21]	0.35μm	0.35-0.6	>70%	90% @R_L=50kΩ	100-5K
This Work	0.18μm	0.2-1.0	>180%	92.5% @R_L=20kΩ	20-3K

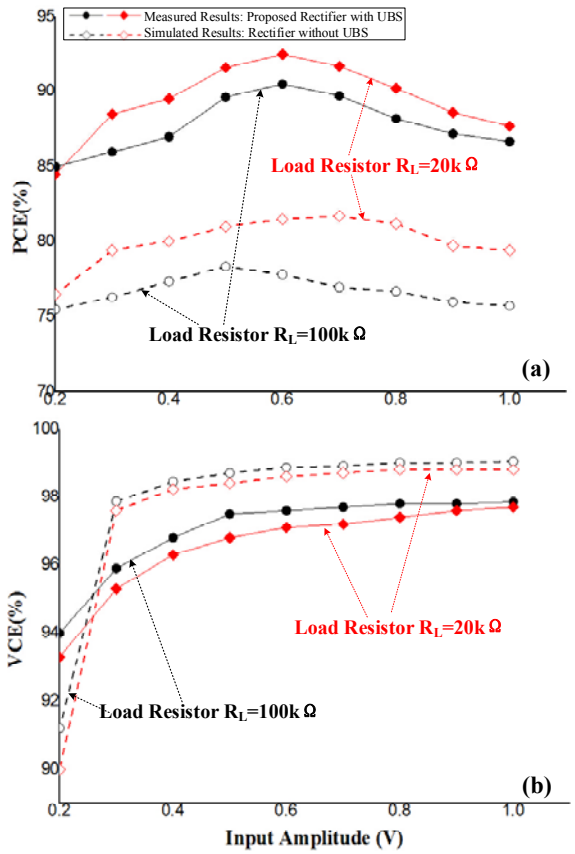


Fig. 10. Simulated and measured. (a) PCE. (b) VCE versus the amplitude of input signal with different loads.

This causes the on-resistance of these switches to increase and the conversion efficiency to decrease. As shown in Fig. 10(b), the measured average VCE of proposed rectifier is higher than 95% when the input amplitude is greater than 0.3V and the load resistance is larger than 20kΩ. When compared with the simulated VCE of a rectifier without the UBCs, the VCE of the proposed rectifier decreases by about 1%-2%. To prevent the reverse leakage current as much as possible, the built-in compensate voltage ΔV should be set large than $|V_{Delay}|+|V_{OS}|$ as mentioned in section III. B. Therefore, the voltage ΔV may be overcompensation for the non-ideal effect. An excessive ΔV can lead to a voltage-drop of the active switch increase in the on-state. This in turn result in VCE performance degradation of the rectifier. Compared with the obvious improvement of the PCE, the slight performance degradation in the VCE can be neglected.

Table II presents the performance of the proposed rectifier and a comparison with previously published state-of-the-art works. The proposed rectifier exhibits excellent performance in terms of power conversion efficiency and a wide input amplitude range. It also achieves the output voltage double. The proposed rectifier can source a 100μA output current into a 20kΩ load resistance, operate at a 200mV input amplitude, and achieve the highest voltage conversion ratio and power efficiency when compared to its counterparts. Therefore, the proposed rectifier is suitable for power transmission systems with a wide input range and a high current output for improving system power efficiency.

V. CONCLUSIONS

In this paper, a highly efficient integrated active voltage doubling rectifier is proposed with a wide input range for piezoelectric energy harvesting systems. The voltage drop along the conduction path is minimized by replacing the passive diode with a comparator-controlled active diode. By using the charge pump topology, the output of the proposed rectifier can boost the input signal amplitude. The common-gate input comparators biased in the subthreshold region effectively reduce the minimum start up voltage of the proposed rectifier. The built-in offset voltages in the comparators implemented by the unbalanced biases suppress the reverse leakage current caused by the delay and process deviations, and improve the efficiency performances of the rectifier. In addition, two bypass MOS diodes and a bulk regulating circuit are added in the proposed rectifier to achieve a safe and robust start-up. The proposed rectifier is simulated and implemented with the SMIC 0.18-μm standard CMOS process. The measured results show that proposed rectifier achieves favorable performances in terms of the input voltage range and conversion efficiency. The proposed

rectifier is very suitable for harvesting ultralow piezoelectric energy for portable and wearable electronic biomedical applications.

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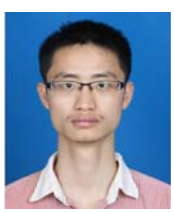

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