JPE 16-3-38

http://dx.doi.org/10.6113/JPE.2016.16.3.1218
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Modeling and Analysis of an Avionic Battery Discharge Regulator

Qian Chen*, Haihong Yu*, Xiaoming Huang*, Yi Lu*, Peng Qiu*, Kai Tong*, Jiazhuo Xuan*, Feng Xu*, Xiaohua Xuan*, Weibo Huang**, and Yajing Zhang†

*Zhejiang Electric Power Corporation Research Institute, Hangzhou, China
**Department of Electronic and Electrical Engineering, Beijing Jiaotong University, Beijing, China
†College of Information Science & Technology, Beijing University of Chemical Technology, Beijing, China

Abstract

The avionic battery discharge regulator (BDR) plays an important role in a power-conditioning unit. With its merits of high efficiency, stable transfer function, and continuous input and output currents, the non-isolated Weinberg converter (NIWC) is suitable for avionic BDR. An improved peak current control strategy is proposed to achieve high current-sharing accuracy. Current and voltage regulators are designed based on a small signal model of a three-module NIWC system. The system with the designed regulators operates stably under any condition and achieves excellent transient response and current-sharing accuracy.

Key words: BDR, Current sharing, Modeling, Peak-current mode control, Weinberg

I. INTRODUCTION

The power-conditioning unit (PCU) balances the power among new energy sources to keep the bus voltage constant. According to various bus voltages, PCU is divided into three categories, namely, 28, 42, and 100 V. The avionic battery discharge regulator (BDR), which controls the discharging procedure of a battery, plays an important role in PCU [1]. The non-isolated Weinberg converter (NIWC) is suitable for BDR because of its merits, such as high efficiency, no right-half-plane (RHP) zeroes, and continuous current.

Many scholars have conducted research on NIWC in the past few years. Lei derived a small signal model of NIWC [2], [3]. Ejea–Marti J. established a small signal model based on peak current control and analyzed stability under a small duty cycle [4]–[6]. Chen analyzed the effect of leakage inductance on the steady-state performance of NIWC [7]. However, the small signal model and controller design of parallel NIWC systems have not been analyzed to date.

This paper presents an improved peak current control strategy to achieve excellent current-sharing accuracy and reliability. Based on a 42 V-level PCU, the small signal model and controller design of a three-module NIWC system under current continuous mode (CCM) are presented.

The transfer functions utilized in the following analysis are defined as follows.

$G_v(s)$:	Voltage regulator
$G_i(s)$:	Current regulator
R_{eq1}:	Sampling coefficient of peak current
R_{eq2}:	Sampling coefficient of average current
$K_v(s)$:	Sampling coefficient of output voltage
F_m:	Current modulator gain
$G_{id}(s)$:	Transfer function of $\hat{i}_{out}(s)$ to $\hat{d}(s)$
$Z_{out}(s)$:	Transfer function of output impedance
$H_{e1}(s)$:	Transfer function describing the sampled data effect on peak current
$H_{e2}(s)$:	Transfer function describing the sampled data effect on average current

II. OPERATING PRINCIPLE

The NIWC is shown in Fig. 1. Couple inductor L_{couple} and transformer T make the input and output current continuous by properly controlling Q_1 and Q_2. The input-damping filter, including L_f, C_{f1}, C_{f2}, and R_f, smoothens the input current to make current sampling convenient and extend the battery

Manuscript received Nov. 16, 2015; accepted Dec. 28, 2015
Recommended for publication by Associate Editor Jee-Hoon Jung.
†Corresponding Author: chenqian05291148@126.com
Tel: +86-13811915954, Beijing University of Chemical Technology
*Zhejiang Electric Power Corporation Research Institute, China
**Dept. of Electronic and Electrical Eng., Beijing Jiaotong Univ., China

© 2016 KIPE

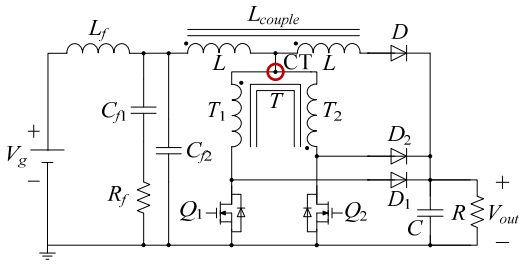


Fig. 1. NIWC.

service life. The operating principle of NIWC is analyzed with Maset E [8], [9].

In consideration of efficiency and reliability, three NIWCs power the main bus in parallel at a rated condition of 1200 W. The control strategy should keep bus voltage stable at 42 V and limit the current-sharing error to 1%.

The control diagram of the three-module NIWC system is shown in Fig. 2. An improved peak current control strategy that includes a voltage regulator, an average current regulator, and a peak current comparator is proposed to avoid transformer saturation and enhance current-sharing accuracy and reliability. The voltage regulator whose output is the reference of the average current regulator stabilizes the bus voltage. The average current loop significantly enhances current-sharing accuracy. The improved peak current control strategy is suitable for system-level applications that focus on current-sharing accuracy and integrity.

III. Power Stage Model

The input filter designed according to the Middlebrook theorem can be neglected in a small signal model [10]. A power stage model of the three-module NIWC system is established in reference to the state-space averaging method, as shown in Fig. 3. Supposing that the duty cycle disturbance $\hat{d}$ of each module is equal, the equivalent inductance is $4L/3$, and the inductance of the single-module power stage model is $4L$ [11]. When the disturbance of input voltage $\hat{v}_g$ is zero, control-to-output current transfer function G_{id}(s) can be derived as Eqn. (1). The power stage model is established in CCM.

$$G_{id}(s)=\left.\frac{\hat{i}_{out}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0}=\frac{V_g(RCs+1)}{4RLCs^2/3+4Ls/3+R} \tag{1}$$

The control-to-output current transfer function G_{id}(s) of the three-module NIWC system is similar to that of the buck converter. Therefore, NIWC easily stabilizes because RHP zeroes do not exist in the transfer functions.

IV. Small Signal Model of the System

In reference to the small signal model of peak current control in [12], the disturbance of duty cycle $\hat{d}(t)$ is related to control current $\hat{i}_c(t)$, output current $\hat{i}_{out}(t)$, input voltage $\hat{v}_g(t)$, and output voltage $\hat{v}_{out}(t)$, as shown below.

$$\hat{d}(t)=F_m[\hat{i}_c(t)-\hat{i}_{out}(t)-F_g\hat{v}_g(t)-F_v\hat{v}_{out}(t)], \tag{2}$$

where $F_m=1/M_aT_s$, $F_g=(D^2+2D-1)T_s/8L$, and $F_v=(1-2D)T_s/8L$. D is the sum of the duty cycles of Q_1 and Q_2, and T_s is half of the period of Q_1. M_a is the slope of the saw-tooth wave used for slope compensation.

According to Eqn. (2), the small signal model of the three-module NIWC system is built and shown in Fig. 4. The sampling coefficients of peak and average currents are one-third of those of the single-module small signal model. F_g and F_v can be disregarded if the current ripple is small. With this simplification, the small signal model of the system is constructed in Fig. 5.

The additional phase delay and disability at half of the equivalent frequency are reflected in the small signal model by introducing $H_{e1}(s)$ and $H_{e2}(s)$[13]. The following equation makes the small signal model close to reality.

$$H_{e1}(s)=H_{e2}(s)=1+\frac{s}{\omega_nQ_z}+\frac{s^2}{\omega_n^2}, \tag{3}$$

where $\omega_n=\pi/T_s$ and $Q_z=-2/\pi$.

V. Converter Design

The system specifications are described in Table I.

In reference to the space engineering electrical and electronic standard established by the European Space Agency (ESA) [14], the requirements of a 42 V regulated-bus PCU are as follows.

- Steady-state characteristic: The peak-to-peak ripple of output voltage is required to be lower than 0.1 V.
- Transient-state characteristic: When the output current changes by 10 A, the voltage spike is required to be lower than ±0.42 V. The duration of the voltage spike over ±0.1 V is required to be less than 7.5 ms.
- The gain margin is higher than 10 dB.
- The phase margin is higher than 60°.
- The closed-loop output impedance is lower than 50 mΩ.
- The current-sharing error should be less than 1%.

The design of the controller should satisfy the aforementioned requirements. When the input voltage is 26 V and the output current is 30 A, the controller is more difficult to design than in other conditions. Thus, the controller is designed under this condition.

A. Current Regulator Design

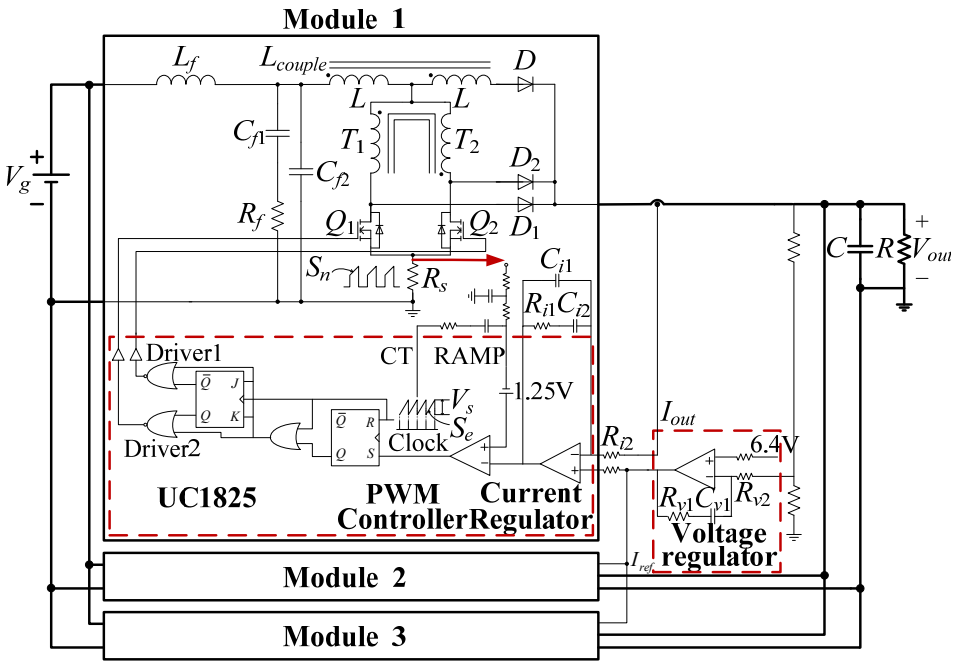


Fig. 2. Three-module NIWC system under improved peak current control.

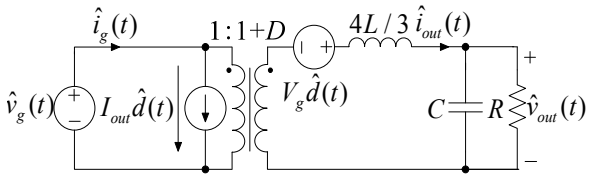


Fig. 3. Power stage model of the three-module NIWC system.

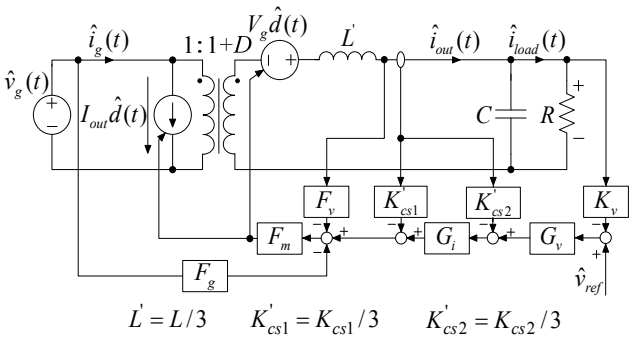


Fig. 4. Small signal model of the three-module NIWC system.

In Fig. 5, the control object of the average current loop is

$$A_{peak}(s)=\frac{\hat{i}_{out}}{\hat{i}_c}=\frac{F_m G_{id}(s)}{1+F_m G_{id}(s)K_{cs1}^{'}(s)}. \quad (4)$$

The loop gain of the average current loop is

$$T_i(s)=G_i(s)A_{peak}(s)K_{cs2}^{'}(s). \quad (5)$$

The uncompensated loop gain of current loop $T_{io}(s)$ with unity compensator gain $G_i(s)$ is depicted in Fig. 6. The cut-off frequency is 19.4 kHz, the gain margin is 9.9 dB, and the phase margin is 92.1°. The DC gain of $T_{io}(s)$ at a low frequency is not sufficiently high to reduce the steady-state

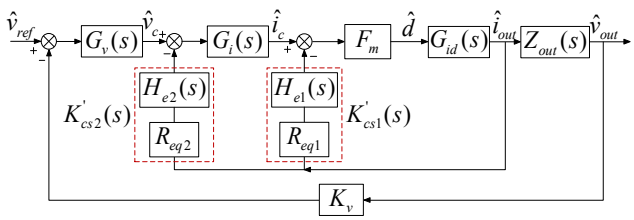


Fig. 5. Modified small signal model of the system.

TABLE I
SYSTEM PARAMETERS

Input voltage (V_{in})	26–38 V
Output current (I_{out})	0–30 A
Output voltage (V_{out})	42 V
Switching frequency (f)	100 kHz
Output capacitor (C)	2 mF
Self-inductance of the couple inductor (L)	20 uH
Sampling coefficient of output voltage (K_v)	6.4/42
Sampling coefficient of average current (R_{eq2})	0.0587
Sampling coefficient of peak current (R_{eq1})	0.333

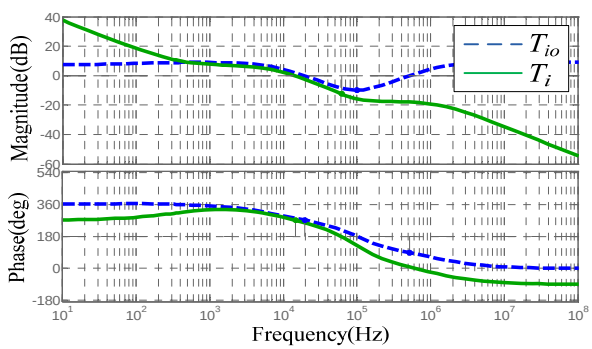


Fig. 6. Bode plots of current loop gains T_i(s) and T_{io}(s).

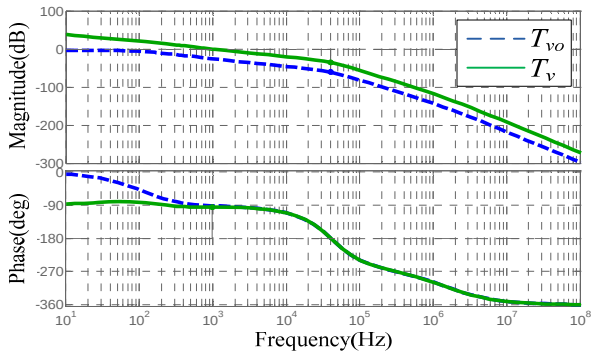


Fig. 7. Bode plots of voltage loop gains $T_v(s)$ and $T_{vo}(s)$.

error. Hence, a low-frequency pole should be added to enhance the DC gain. $|T_{io}(j\omega)|_{dB}$ at high frequencies is higher than 0, which amplifies high-frequency noise. A high-frequency pole should therefore be added to improve anti-interference capability. Based on this analysis, a single-zero double-pole compensator is selected as the current regulator. The current regulator, which is presented in Fig. 2, is expressed as

$$G_i(s)=\frac{K_i(1+s/\omega_{zi})}{s(1+s/\omega_{pi})}, \tag{6}$$

where $K_i=1/R_{i2}(C_{i1}+C_{i2})$, $\omega_{zi}=1/R_{i1}C_{i2}$, and $\omega_{pi}=(C_{i1}+C_{i2})/R_{i1}C_{i1}C_{i2}$.

The parameters are $R_{i1}=8k\Omega$, $R_{i2}=10k\Omega$, $C_{i1}=240pF$, and $C_{i2}=50nF$.

The compensated loop gain of current loop $T_i(s)$ is also shown in Fig. 6. For $T_i(s)$, the cut-off frequency is 14.45 kHz, the gain margin is 12.3 dB, and the phase margin is 91.5°.

B. Voltage Regulator Design

After designing the current regulator, the control object of voltage loop is derived from Fig. 5, as shown below.

$$A_i(s)=\frac{\hat{v}_{out}}{\hat{v}_c}=\frac{G_i(s)A_{peak}(s)Z_{out}(s)}{1+G_i(s)A_{peak}(s)K_{cs2}^{'}(s)} \tag{7}$$

The loop gain of the voltage loop is

$$T_v(s)=G_v(s)A_i(s)K_v. \tag{8}$$

The uncompensated loop gain of voltage loop $T_{vo}(s)$ with unity compensator gain $G_v(s)$ is depicted in Fig. 7. The cut-off frequency of $T_v(s)$ is designed to be approximately 1 kHz to satisfy the requirement that the cut-off frequency of the voltage loop should be lower than that of the current loop. In Fig. 7, the amplitude–frequency curve of $T_{vo}(s)$ is lower than 0 dB, which means the system is unstable. A single-zero single-pole compensator is selected as the voltage regulator to enhance DC gain and stability. The voltage regulator, which is presented in Fig. 2 is expressed as

$$G_v(s)=\frac{K_v(1+s/\omega_{zv})}{s}, \tag{9}$$

where $K_v=1/R_{v2}C_{v1}$ and $\omega_{zv}=1/R_{v1}C_{v1}$.

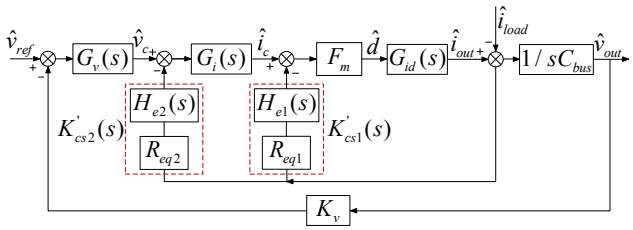


Fig. 8. Small signal model of output impedance.

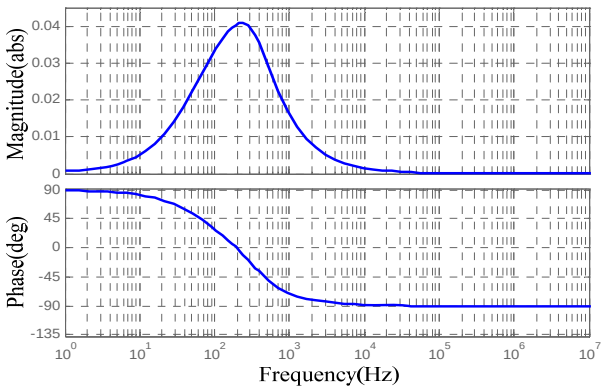


Fig. 9. Bode plots of output impedance.

The gain of $T_{vo}(s)$ at 1 kHz is −25.5 dB. The cut-off frequency of $T_v(s)$ is designed to be 1 kHz; thus, $20\log(|R_{v1}/R_{v2}|)$=25.5 dB. If R_{v2}=10 *k*Ω, then R_{v1}≈300 *k*Ω. The zero frequency of the voltage regulator is designed to be 100 Hz, so C_{v1}≈5.4 *n*F.

The compensated loop gain of voltage loop $T_v(s)$ is also shown in Fig. 7. For $T_v(s)$, the cut-off frequency is 1 kHz, the gain margin is 35.5 dB, and the phase margin is 84.7°, which satisfies the requirements of ESA. Accordingly, the system is stable.

C. Analysis of Closed-Loop Output Impedance

The small signal model of close-loop output impedance when the disturbance of input voltage $\hat{v}_g$ is zero is shown in Fig. 8 by introducing the disturbance of load current $\hat{i}_{load}(s)$. The transfer function of close-loop output impedance is

$$Z_{out}(s)=-\frac{\hat{v}_{out}(s)}{\hat{i}_{load}(s)}=\frac{\frac{1}{C_{bus}s}}{1+\frac{K_vG_v(s)G_i(s)F_mG_{id}(s)}{C_{bus}s(1+F_mG_{id}(s)K_{cs1}^{'}(s)+G_i(s)F_mG_{id}(s)K_{cs2}^{'}(s))}}. \tag{10}$$

In Fig. 9, the maximum output impedance is 41.4 *m*Ω, which satisfies the requirements. Hence, NIWC has a good load adjustment rate.

VI. Experimental Confirmation

A 1200 W prototype (shown in Fig. 10) is built with a two-layer power printed circuit board to confirm the superiority of the improved peak current control strategy and

Fig. 10. Experimental platform of the three-module NIWC system.

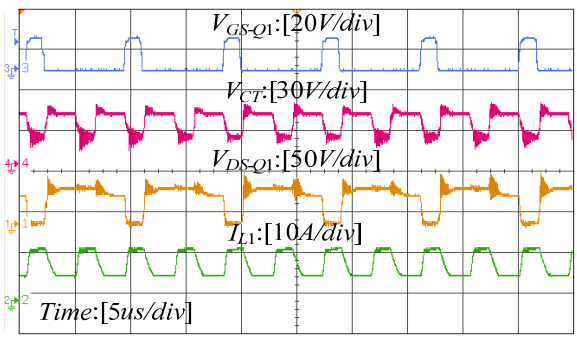


Fig. 11. Key waveforms of NIWC.

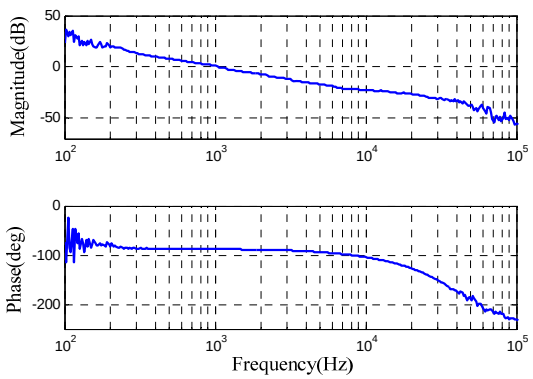


Fig. 12. Measured voltage loop gain T_v(s).

the rationality of regulator design.

Fig. 11 shows the drive signal, the voltage of the current transformer, the drain-to-source voltage of the metal–oxide–semiconductor field-effect transistor, and the primary current of the couple inductor when the input voltage is 32 V. Under any condition, the input and output currents are continuous, and the bus voltage is stable at 42 V.

The Bode plots of voltage loop gain T_v(s) and output impedance Z_{out}(s) are measured with gain-phase analyzer N4L_PSM1735. Given that the operating frequency of the test transformer is constrained, the test frequency range varies from 100 Hz to 100 kHz. Fig. 12 shows that measured voltage loop gain T_v(s) presents a good agreement with the calculated one in Fig. 7, which verifies the correction of the small signal model. The magnitude and phase margins satisfy

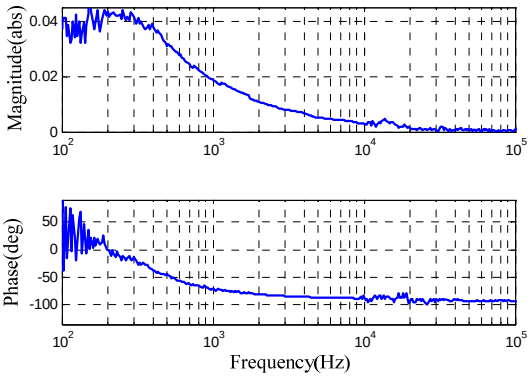


Fig. 13. Measured closed-loop output impedance Z_{out}(s).

the requirements of ESA, so the system is stable. In Fig. 13, measured closed-loop output impedance Z_{out}(s) agrees with the calculated results in Fig. 9. The maximum output impedance is lower than 50 $m\Omega$ during the entire frequency band, which satisfies the requirements. Therefore, NIWC has a good load adjustment rate.

Table II represents the current-sharing performance without a current-sharing strategy when the input voltage is 32 V. Table III shows the current-sharing performance with the peak current control strategy, and Table IV presents the current-sharing performance with the improved peak current control strategy. The current-sharing error is calculated according to the following equation.

$$CS_{error}\% = \frac{\max[abs(I_i - \sum_{k=1}^{n} I_k / n)]}{\sum_{k=1}^{n} I_k / n}, \quad (11)$$

where $\sum_{k=1}^{n} I_k / n$ is the average output current and $\max[abs(I_i - \sum_{k=1}^{n} I_k / n)]$ is the maximum difference between the output current of each module and the average output current.

From Tables II–IV, conclusions can be drawn as follows.

- The current-sharing performance without a current-sharing strategy is the worst among all performances.
- The current-sharing performance with the peak current control strategy is good but still cannot satisfy the 1% requirement.
- The current-sharing performance with the improved peak current control strategy satisfies the 1% requirement under any condition.

These conclusions demonstrate the superiority of the improved peak current control strategy.

Fig. 14 shows the transient response of the output voltage when the load changes by 10 A. The bus voltage ripple is

TABLE II
CURRENT-SHARING PERFORMANCE WITHOUT A CURRENT-SHARING CONTROL STRATEGY

$I_1(A)$	$I_2(A)$	$I_3(A)$	$CS_{error}\%$
2.892	1.851	1.228	45.3%
5.123	3.376	2.595	38.5%
6.983	5.345	3.681	31.02%
8.565	7.252	5.248	25.25%
10.372	8.651	6.985	19.64%
11.389	9.475	8.152	17.75%

TABLE III
CURRENT-SHARING PERFORMANCE WITH THE PEAK CURRENT CONTROL STRATEGY

$I_1(A)$	$I_2(A)$	$I_3(A)$	$CS_{error}\%$
2.332	2.023	1.679	16.52%
3.921	3.825	3.291	10.55%
5.875	5.328	4.805	10.1%
7.561	6.936	6.484	8.11%
9.413	8.541	8.174	8.08%
10.353	9.451	9.212	7.04%

TABLE IV
CURRENT-SHARING PERFORMANCE WITH THE IMPROVED PEAK CURRENT CONTROL STRATEGY

$I_1(A)$	$I_2(A)$	$I_3(A)$	$CS_{error}\%$
2.018	2.003	1.999	0.56%
3.682	3.651	3.687	0.608%
5.371	5.323	5.316	0.643%
7.031	7.015	6.934	0.848%
8.701	8.674	8.645	0.327%
9.69	9.665	9.641	0.255%

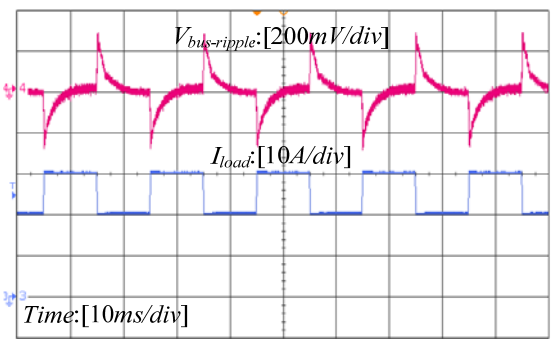


Fig. 14. Transient response for load changes from 20 A to 30 A.

constrained within 40 mV. When the output current changes from 20 A to 30 A, the voltage spike is 0.28 V. The duration of the voltage spike that exceeds −0.1 V is 1.65 ms. When the output current changes from 30 A to 20 A, the voltage spike is 0.29 V. The duration of the voltage spike that exceeds 0.1 V is 1.68 ms. The steady and transient characteristics of output voltage satisfy the requirements with a large margin.

Fig. 15 shows the transient response of the output current for each module when the load changes by 10 A (20 A to 30 A). Figs. 14 and 15 show that the system gains an excellent transient response and current-sharing accuracy under the improved peak current control strategy.

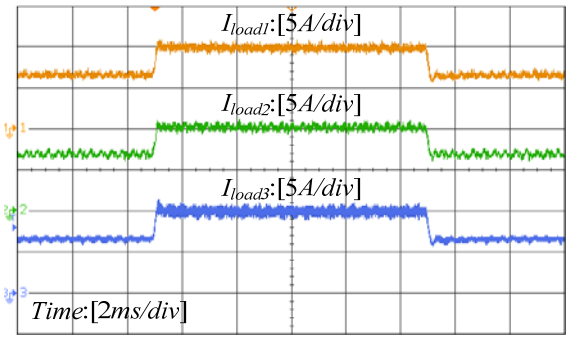


Fig. 15. Transient current-sharing performance for load changes from 20 A to 30 A.

VII. CONCLUSION

Based on the three-module NIWC system, the power stage model is derived. Improved peak current control strategy is proposed to avoid the saturation of the transformer and enhance the current sharing accuracy and reliability. The current and voltage regulators are designed according to the requirements. Finally, the experimental results are given to verify that the system gains an excellent transient response and current sharing accuracy under improved peak current control strategy by a 1200W prototype. This control strategy is suitable for the system-level application which is strict on the current sharing accuracy and integrity.

REFERENCES

[1] K. H. Park, C. H. Kim, and H. K. Cho, "Design considerations of a lithium ion battery management system (BMS) for the STSAT-3 satellite," *Journal of Power Electronics*, Vol. 10, No. 2, pp. 210-217, Mar. 2010.

[2] W. Lei, C. Wan, and B. Han, "Modeling analysis and study of the Weinberg converter with current programming control for space application," *in Proceedings of the 8th European Space Power Conference*, Konstanz, 2008.

[3] W. Lei and Y. Li, "Small-signal modeling and analysis of the weinberg converter for high-power satellites bus application," *Chinese Journal of Electronics*, Vol. 18, No. 1, pp. 171-176, 2009.

[4] J. Ejea-Marti, E. Sanchis-Kilders, E. Maset, A. Ferreres, J. M. Blanes, A. Garrigos, J. Jordan, and V. Esteve, "Phase margin degradation of a peak current controlled converter at reduced duty cycle," *IEEE Trans. Power Electron.*, Vol. 25, No. 4, pp. 863-874, Apr. 2010.

[5] J. Ejea-Marti, E. Sanchis-Kilders, E. Maset, A. Ferreres, J. Jordan, and V. Esteve,"Stability problems of peak current control at narrow duty cycles," in *Proc. IEEE Conference on Applied Power Electronics*, 2008.

[6] J. Ejea-Marti, E. Sanchis-Kilders, E. Maset, A. Ferreres, J. Jordan, and V. Esteve, "Peak current control instabilities at

narrow duty cycles," in *Proc. IEEE Conference on Computational Intelligence and Security Workshops*, 2008.
[7] Q. Chen, T. Q. Zheng, Y. Li, and T. Shao, "The effect of transformer leakage inductance on the steady state performance of push-pull based converter with continuous current," *Journal of Power Electronics*, Vol. 13, No. 3, pp. 349-361, May 2013.
[8] E. Masetand and A. Ferreres, "5kW Weinberg converter for battery discharging in high-power communications satellites," in *Proc. IEEE Conference on Power Electronics Specialists*, 2005.
[9] E. Maset, J. B. Ejea, A. Ferreres, E. Sanchis-Kilders, J. Jordan, and V. Esteve "High-efficiency weinberg converter for battery discharging in aerospace applications," in *Proc. IEEE Conference on Applied Power Electronics*, 2006.
[10] R. D. Middlebrook, "Design techniques for preventing input-filter oscillations in switched-mode regulators," in *Proc. Powercon 5*, 1978.
[11] B. Choi, B. H. Cho, R. B. Ridley, and F. C. Lee, "Control strategy for multi-module parallel converter system," in *Proc. IEEE Conference on Power Electronics Specialists*, 1990.
[12] R. W Erickso, *Fundamentals of Power Electronics,* 2nd ed., Massachusetts: Kluwer Academic Publisher, pp. 462-504, 2001.
[13] M. K. Kazimierczuk, "Transfer function of current modulator in PWM converters with current-mode control," *IEEE Trans. Circuits Syst. I, Fundam. Theory*, Vol. 47, No. 9, pp. 1407-1412, Sep. 2000.
[14] ECSS-E-20A: Space engineering electrical and electronic, October 4th 1999.

Qian Chen was born in Zhejiang Province, China, in 1987. He received his B.S. and Ph.D. degrees in electrical engineering from Beijing Jiao Tong University, Beijing, China, in 2009 and 2015, respectively. He is currently an engineer at Zhejiang Electric Power Corporation Research Institute, Hang Zhou, China. His current research interests include HVDC, FACTS, and DC grids.

Haihong Yu is the deputy manager of Power Transmission Center of Electric Power Research Institute of Zhejiang Provincial Electric Power Corporation (a subsidiary of SGCC). He worked for four years with the National Grid Power Corporation of the Philippines as the head of the Transmission Planning Department under a technical assistance programmer provided by SGCC. Power transmission planning and modeling are the main areas where he has specialized in for his 22 years with the electric power sector.

Xiaoming Huang received his B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 1991. He is currently the deputy manager at Electric Power Research Institute of State Grid Zhejiang Electric Power Corporation, Hang Zhou, China. His current research interests include relay protection and HVDC.

Yi Lu received his B.S. degree in electrical engineering from North China Electric Power University, Baoding, China, in 2001. He received his M.S. and Ph.D. degrees in intelligence engineering and electrical engineering from the University of Liverpool, Liverpool, U.K., in 2002 and 2007, respectively. In 2008, he joined the Zhejiang Electric Power Corporation Research Institute, Hangzhou, China. He is currently a senior engineer, and his research interests include HVDC and FACTS.

Peng Qiu received his B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2011, respectively. Since 2011, he has been an engineer at Zhejiang Electric Power Corporation Research Institute, Hang Zhou, China. His current research interests include HVDC and FACTS.

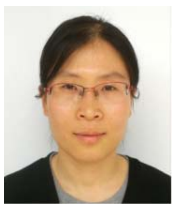
Kai Tong received his B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2006. Since 2006, he has been an engineer at Zhejiang Electric Power Corporation Research Institute, Hang Zhou, China. His current research interests include relay protection and HVDC.

Jiazhuo Xuan received his B.S degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and his M.S degree in renewable energy engineering from the University of New South Wales, Sydney, Australia, in 2012. Since 2012, he has been an engineer at Zhejiang Electric Power Corporation Research Institute, Hangzhou, China. His current interests include relay protection and HVDC.

Feng Xu was born in Zhejiang, China, in February 1988. He received his B.S. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2010 and 2015, respectively. He currently works at Zhejiang Electric Power Corporation Research Institute. His research focus is on high power electronics technology, LCC-HVDC transmission systems, VSC-HVDC transmission systems, and DC grids.

Xiaohua Xuan received his B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 1987. He is currently the deputy manager at Electric Power Research Institute of State Grid Zhejiang Electric Power Corporation, Hang Zhou, China. His current research interests include management of power system technology.

Weibo Huang received his B.S. and M.S. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2012 and 2015, respectively. Since 2015, he has been working for his Ph.D. degree at the Department of Electronic and Electrical Engineering, Beijing Jiaotong University, Beijing, China. His research interests include high-power converters for flexible HVDC applications and protection and control of flexible multi-terminal DC power distribution systems.



Yajing Zhang was born in Hebei Province, China. She received his B.S. degree in Electrical Engineering from the Beijing Jiaotong University, Beijing, China, in 2008; and hers Ph.D. degree in Electrical Engineering from Beijing Jiaotong University, Beijing, China, in 2015. In 2015, she joined the College of Information Science & Technology, Beijing University of Chemical Technology, Beijing, China, where she is presently working as a Post Doctorate. Her current research interests include power systems, Wide band gap semiconductor devices, Wireless power transmission and renewable resource generation.