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Dickson Charge Pump with Gate Drive Enhancement and Area Saving

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Abstract

This paper presents a novel charge pump scheme that combines the advantages of Fibonacci and Dickson charge pumps to obtain 30 V voltage for display driver integrated circuit application. This design only requires four external capacitors, which is suitable for a small-package application, such as smart card displays. High-amplitude (<6.6 V) clocks are produced to enhance the gate drive of a Dickson charge pump and improve the system's current drivability by using a voltage-doubler charge pump with a pulse skip regulator. This regulation engages many middle-voltage devices, and approximately 30% of chip size is saved. Further optimization of flying capacitors tends to decrease the total chip size by 2.1%. A precise and simple model for a one-stage Fibonacci charge pump with current load is also proposed for further efficiency optimization. In a practical design, its voltage error is within 0.12% for 1 mA of current load, and it maintains a 2.83% error even for 10 mA of current load. This charge pump is fabricated through a 0.11 μm 1.5 V/6 V/32 V process, and two regulators, namely, a pulse skip one and a linear one, are operated to maintain the output of the charge pump at 30 V. The performances of the two regulators in terms of ripple, efficiency, line regulation, and load regulation are investigated.

Key words: Chip size, Dickson charge pump, Efficiency, External capacitor, Fibonacci charge pump, High amplitude

I. INTRODUCTION

With the continuing development of handheld devices, such as cell phones, laptops, and digital cameras, switched-capacitor converters or charge pumps have become highly attractive in high-voltage applications. A boost converter using an inductor to transfer energy has high power efficiency, but its bulky inductors occupy a large area of the printed circuit board and result in the electromagnetic interference (EMI) problem [1]. A low drop-out regulator can be entirely on-chip and occupies a small chip size. This regulator outputs a small ripple and has no EMI problem, but it can only generate voltage that is smaller than the input voltage. Efficiency is also reduced linearly with the increase in the voltage difference between the input and output. A charge pump that consists only of switches and capacitors but supplies a higher voltage than the input is desirable. Without magnetic components, such a charge pump is promising for integration and small-package applications. However, the numerous external capacitors required increase the total cost and reduce the integration. For a display driver integrated circuit (IC), its driving power is 30 V, with a minimum current of 200 μA. A charge pump with moderate current drivability to boost voltage from the input voltage of VCI to 30 V is required because the range of global power VCI is normally from 2.4 V to 3.6 V. A traditional scheme with voltage doublers in series, as shown in Fig. 1, or its enhanced scheme in [2] needs eight or five external capacitors, respectively. The enhanced scheme saves three external components but entails compromises in ripple and efficiency performance. A complex 16-phase non-overlapping clock control is also necessary. Another design still requires at least seven external capacitors [3]. Previous designs can achieve high efficiency and small chip size contributed by power switches with many external capacitors, but their use is

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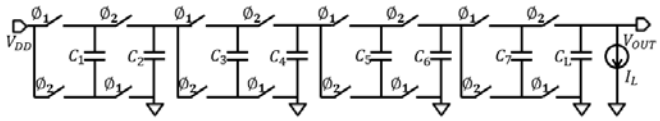


Fig. 1. Traditional charge pump with voltage doubler in series.

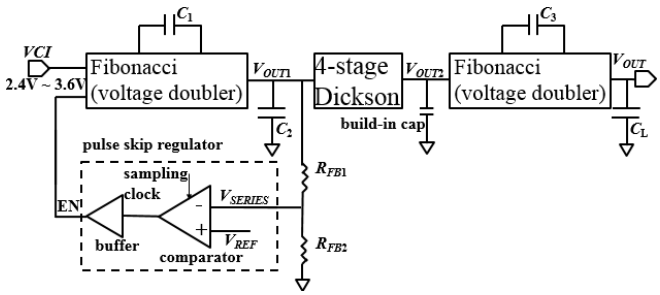


Fig. 2. Proposed charge pump core to enhance current drivability and save on external capacitors.

limited when applied to small-sized package applications, such as smart cards.

In this work, a mixed-type charge pump with minimal external components is proposed to produce 30 V of output voltage to support display driver ICs. The pump also reduces pin-outs, reduces the bonding cost, and improves reliability, particularly in a harsh environment. By combining the advantages of Dickson and Fibonacci charge pumps, this design achieves the area advantage because of the Dickson charge pump and requires minimal external components because of the Fibonacci charge pump. A double input voltage is produced to enhance the gate drive of each power switch to improve the current drivability of the Dickson charge pump. A pulse skip regulator is utilized to constrain the supply voltage of the Dickson charge pump to a safe voltage (6.6 V) to meet the voltage limit of middle-voltage (MV) transistors. This design reduces the total chip size. It only uses four external capacitors and saves four external capacitors compared with traditional schemes. In addition, precise and simple models of Fibonacci and Dickson charge pumps are provided for further system optimization.

II. Proposed Charge Pump Architecture

The proposed charge pump core is shown in Fig. 2. Considering that the breakdown voltage of the metal–insulator–metal (MIM) capacitor in this process is only 17.6 V, another voltage doubler charge pump is added to the following Dickson charge pump. This charge pump boosts the output voltage of the Dickson pump to 30 V, and its two capacitors are all external to improve current drivability. The voltage doubler charge pump thus requires less stages of the Dickson charge pump.

Through a 0.11 μm process, the maximum voltages for low-voltage (LV), MV, and high-voltage (HV) transistors are determined to be 1.5, 6, and 32 V, respectively.

The first output (V_{OUT1}) of the Fibonacci charge pump is regulated within 6.6 V, as shown in Fig. 2, considering the tolerance of the MV transistors. A pulse skip regulator is utilized in the regulation for efficiency consideration. Only MV power switches are allowed to be used in the first Fibonacci charge pump to save on chip size. For the Dickson charge pump, the power switch and flying capacitor in its first stage can all be MV devices, and all clock buffers are also MV transistors. Compared with the traditional HV buffer design, this design, with the regulation of V_{OUT1}, saves approximately 30% of chip size by engaging more MV devices and improves power efficiency simultaneously. A total of four external capacitors (C_1, C_2, C_3, C_L) are utilized in the charge pump system, as shown in Fig. 2.

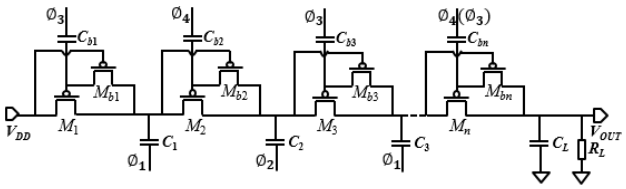


Fig. 3. (N-1)-stage Dickson charge pump core.

III. Four-Phase Dickson Charge Pump

For the area-driven scheme, Dickson, series–parallel, and Fibonacci are good choices for the built-in capacitor situation if the voltage conversion ratio (VCR) is larger than 8/5. Among the three, Dickson is better owing to its shorter charging chain and lower power consumption with parasitic capacitors. Its minimal chip size is mostly decided by its capacitor size and is calculated in [4] as

$$C_{TOT} = 4\frac{I_{out}}{f}\frac{V_{out}-V_{in}}{V_{in}}. \quad (1)$$

For the complete (N-1)-stage Dickson charge pump shown in Fig. 3, a four-phase clock with bootstrap gate control is utilized to avoid threshold voltage loss in each stage to improve power efficiency [5]. The body of each transfer transistor M_i is biased to a high voltage between the source and drain to avoid leakage current of parasitic bipolar [6] [7]. We define the output voltage as I_{load}, the operation frequency as f, and the flying capacitance for the corresponding stage as C_i. Given that charging/discharging completely is easy, the voltage drop for the i-th stage can be provided by

$$\Delta V_i = I_{load}/(fC_i). \quad (2)$$

The total voltage loss ΔV can be provided by

$$\Delta V = \frac{I_{load}}{f}\sum_{i=1}^{n-1}\frac{1}{C_i}. \quad (3)$$

The current drivability can then be optimized because it is relevant to the calculated voltage loss.

With the system design in Fig. 2, the power supply of the Dickson charge pump is approximately $4.4\,V$ to $6.6\,V$, and gate capacitors are used in the first stage of the pump as flying capacitors because they have larger sheet capacitance than MIM capacitors. The capacitors should be optimized

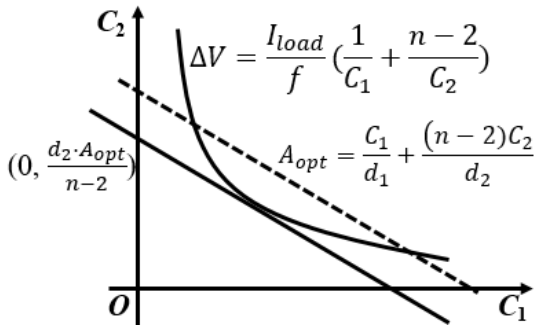


Fig. 4. Optimized curves for capacitances.

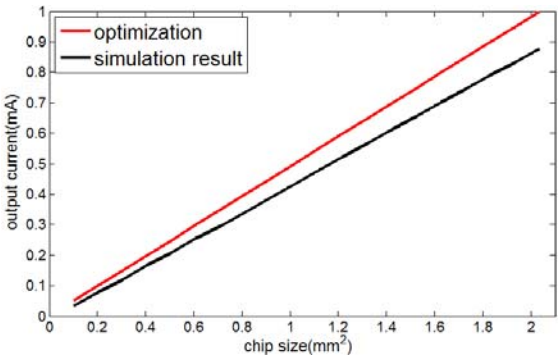


Fig. 5. Optimized chip size versus output current.

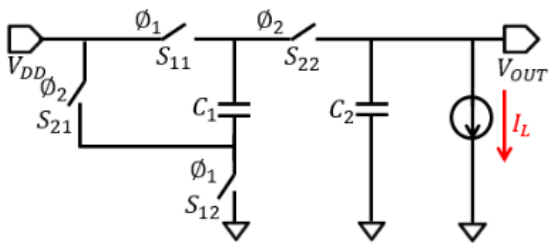


Fig. 6. One-stage Fibonacci charge pump.

over the required current drivability because the capacitors occupy most of the chip. We define the sheet capacitances of gate and MIM capacitors as d_1 and d_2, respectively. The optimized chip size can be obtained by

$$A_{opt} = \frac{C_1}{d_1} + \frac{1}{d_2}\sum_{i=2}^{n-1} C_i. \quad (4)$$

By combining Equs. (3) and (4), we find that $C_2, C_3, \cdots, C_{n-1}$ are at equal positions. Therefore, they can also be equal during the simplification (denoted as C_2). Equs. (3) and (4) can then be simplified as

$$\Delta V = \frac{I_{load}}{f}\left(\frac{1}{C_1} + \frac{n-2}{C_2}\right), \quad (5)$$

$$A_{opt} = \frac{C_1}{d_1} + \frac{(n-2)C_2}{d_2}. \quad (6)$$

For a certain system, the pump stage, total voltage loss, operation frequency, and output current are all determined. For different values (C_1, C_2), Equ. (5) describes the correlation between C_1 and C_2 as a hyperbolic trend, and Equ. (6) refers to a monotone-decreasing line with intercept of $d_2 \cdot A_{opt}/(n-2)$. The two curves should have at least one crossover point, as shown in Fig. 4. Optimized chip size A_{opt} is obtained when the straight line remains tangent to the hyperbola. This condition can be expressed as

$$C_2^2 \cdot \frac{n-2}{d_2} - C_2\left(A_{opt} + \left(\frac{(n-2)^2 d_1}{d_2} - 1\right)\frac{I_{load}}{f \cdot \Delta V \cdot d_1}\right) + \frac{(n-2) I_{load} A_{opt}}{f \Delta V}, \quad (7)$$

$$\left(A_{opt} + \left(\frac{(n-2)^2 d_1}{d_2} - 1\right)\frac{I_{load}}{f \Delta V d_1}\right)^2 - \frac{4(n-2)^2 \cdot I_{load} \cdot A_{opt}}{f \cdot \Delta V \cdot d_2} = 0. \quad (8)$$

A_{opt} can then be solved by Equ. (8). A_{opt} is proportional to $I_{load}/f/\Delta V$, and the capacitances C_1 and C_2 are provided by

$$C_2 = \left(A_{opt} + \left((n-2)^2 \frac{d_1}{d_2} - 1\right)\frac{I_{load}}{d_1 \cdot f \cdot \Delta V}\right)\frac{d_2}{2(n-2)}, \quad (9)$$

$$C_1 = d_1\left(A_{opt} - \frac{(n-2)C_2}{d_2}\right). \quad (10)$$

In the charge pump system in Fig. 2, a four-stage Dickson charge pump is constructed, followed by a voltage doubler to achieve 30 V at the output terminal. Obtaining 15.3 V at the output terminal of the Dickson charge pump is then reasonable. In a practical design, the minimum power supply is approximately 4.4 V (VCI = 2.4 V at full load condition), and the total voltage loss is $\Delta V = 6.7\,V$. The optimized chip size for various output currents is obtained by setting the operation frequency to 1 MHz, as shown in Fig. 5. For a certain chip size, the simulation result on output current is smaller than the theoretical calculation because the coupled capacitors (C_{gs}, C_{gd}) of the auxiliary transistor M_{bi} result in a voltage drop during the charging phase. A large operation frequency will reduce the total chip size because A_{opt} is proportional to $(I_{load}/f)/\Delta V$.

Another case with equal performance but using equal flying capacitance per stage is also calculated for chip size comparison. Its chip size is 2.1% larger than the most optimized one.

IV. Precise and Simple Model for One-Stage Fibonacci Charge Pump

A Fibonacci charge pump is considered a two-phase charge pump with a small number of external capacitors to achieve the same voltage ratio. A one-stage Fibonacci charge pump can output $2V_{DD}$ at the output terminal ideally, which is similar to a voltage doubler topology. Its topology is shown in Fig. 6. R_{ij} represents the turn-on resistance of each switch S_{ij}.

Researchers have established a model for situations with resistor load [8], but the model includes highly complex formulas to use for the output current design. In practical applications, current drivability needs to be considered in particular. Given that the load current is constant, the term V_{OUT} related to the load condition can be eliminated. A precise and simple model is proposed in this study, based on which both efficiency and chip size can be optimized.

The equivalent circuit when the pump reaches its

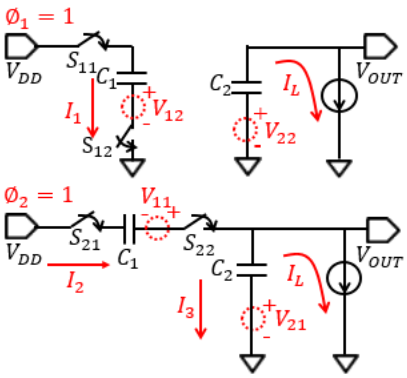


Fig. 7. Equivalent circuit for each phase when the pump reaches equilibrium.

equilibrium state is shown in Fig. 7, where V_{i1} represents the final voltage for capacitor i at phase $\emptyset_1 = 1$ and V_{i2} represents the final voltage for capacitor i at phase $\emptyset_2 = 1$. We define V_{C1}^I and V_{C2}^I as the voltages of the corresponding capacitors during phase $\emptyset_1 = 1$. V_{C1}^{II} and V_{C2}^{II} represent those in the other phase. The s-domain voltage formulas for each capacitor are then derived.

During the phase $\emptyset_1 = 1$, three formulas are constructed as

$$I_1 = (V_{C1}^I(s) - V_{12}/s) \cdot C_1 s, \quad (11)$$

$$I_1 = (V_{DD}/s - V_{C1}^I(s))/(R_{11} + R_{12}), \quad (12)$$

$$I_L/s = (V_{22}/s - V_{C2}^I(s)) \cdot C_2 s. \quad (13)$$

Solving Equs. (11) to (13) results in

$$V_{C1}^I(s) = V_{DD}/s - (V_{DD} - V_{12})\tau_1/(1 + s\tau_1), \quad (14)$$

$$V_{C2}^I(s) = V_{22}/s - I_L/(C_2 s^2)), \quad (15)$$

$$\tau_1 = (R_{11} + R_{12}) \cdot C_1. \quad (16)$$

Changing the s-domain function to a time-domain one yields

$$V_{C1}^I(t) = V_{DD} + (V_{12} - V_{DD}) \cdot exp(-t/\tau_1), \quad (17)$$

$$V_{C2}^I(t) = V_{22} - I_L \cdot t/C_2). \quad (18)$$

During the phase $\emptyset_2 = 1$,

$$I_2 = -(V_{C1}^{II}(s) - V_{11}/s) \cdot C_1 s, \quad (19)$$

$$I_2 = I_3 + I_L/s, \quad (20)$$

$$I_2 = (V_{DD}/s - V_{C2}^{II}(s) + V_{C1}^{II}(s))/(R_{21} + R_{22}), \quad (21)$$

$$I_3 = (V_{C2}^{II}(s) - V_{21}/s) \cdot C_2 s. \quad (22)$$

By solving Equs. (19) to (22) and changing the s-domain function to a time-domain one, we obtain

$$V_{C2}^{II}(t) = \left(\frac{V_{21} - V_{11} - V_{DD}}{1 + \frac{C_2}{C_1}} - \frac{I_L(R_{21} + R_{22})}{\left(1 + \frac{C_2}{C_1}\right)^2}\right) \cdot \exp\left(-\frac{t}{\tau_2}\right), \quad (23)$$

$$V_{C1}^{II}(t) = V_{11} + V_{21}C_2/C_1 - I_L \cdot t/C_1 - V_{C2}^{II}(t)C_2/C_1, \quad (24)$$

$$\tau_2 = (R_{21} + R_{22}) \cdot C_2/(1 + C_2/C_1). \quad (25)$$

We define the clock period and operation frequency as T and f, respectively, and we assume that the duty ratio is exactly 50%. The voltage of each capacitor when the system is in equilibrium is shown in Fig. 8. Hence,

$$V_{C1}^{II}(T/2) = V_{12}, \quad (26)$$

$$V_{C2}^{II}(T/2) = V_{22}, \quad (27)$$

$$V_{C1}^{I}(T/2) = V_{11}, \quad (28)$$

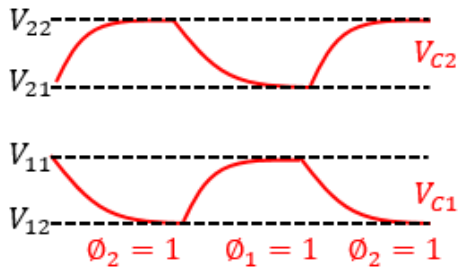


Fig. 8. Equilibrium voltage for each capacitor.

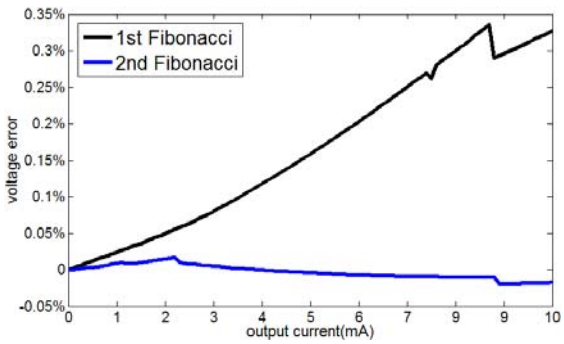


Fig. 9. Error of the output voltage with ideal switches for the Fibonacci charge pumps in the two stages of the design.

$$V_{C2}^I(T/2) = V_{21}. \quad (29)$$

The specification of output voltage V_{OUT} is always provided by the average voltage of the waveform as

$$V_{OUT} = \frac{1}{T}\left(\int_0^{\frac{T}{2}} V_{C2}^I(t)dt + \int_0^{\frac{T}{2}} V_{C2}^{II}(t)dt\right). \quad (30)$$

By combining Equs. (16) to (18) and (23) to (30), we solve the output voltage as

$$V_{OUT} = 2V_{DD} - \frac{I_L(R_{21}+R_{22})}{1+\frac{C_2}{C_1}} - \frac{\frac{I_L T}{2}\left(\frac{2}{C_1}+\frac{1}{C_2}\right)}{1-\exp(-\alpha_2)} - \frac{I_L T}{C_1}\frac{\exp(-\alpha_1)}{1-\exp(-\alpha_1)} + \frac{I_L T}{4C_2}, \quad (31)$$

$$\alpha_1 = T/(2\tau_1), \quad (32)$$

$$\alpha_2 = T/(2\tau_2). \quad (33)$$

For the system in Fig. 2, two Fibonacci charge pumps are adopted. The simulation results based on this system are aligned with what the model reveals. The corresponding output voltage errors of the two charge pumps when the power supplies are set to 2.4 and 15.3 V are shown in Fig. 9. For output currents of 0 mA to 10 mA, the errors are maintained within 0.35% and 0.02%.

In a practical design, a p-type metal oxide semiconductor is commonly used (M_{11}, M_{21}, M_{22} in Fig. 6) for switches S_{11}, S_{21}, and S_{22} to achieve fast start-up, whereas an n-type metal oxide semiconductor (M_{12} in Fig. 6) is employed for S_{12} to save on size. For a metal oxide semiconductor transistor with a size of W/L and gate-to-source voltage of V_{GS}, the turn-on resistance is defined as

$$R_{on} = \frac{1}{\mu C_{ox}(W/L)(V_{GS} - V_T)}. \quad (34)$$

For a certain V_{DD}, the turn-on resistance of M_{11}, M_{12}, M_{21} can be precisely calculated, whereas that of M_{22} is difficult

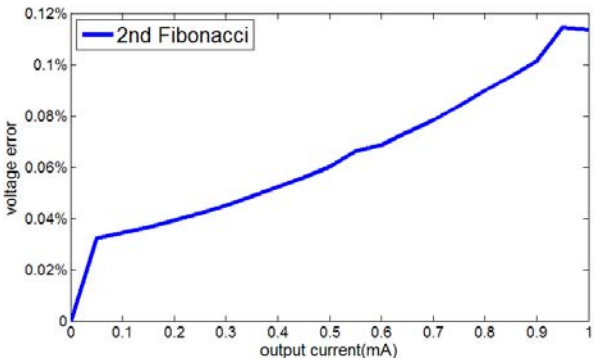


Fig. 10. Error of the output voltage in practical design for the second Fibonacci charge pump.

to calculate because it changes with output voltage V_{OUT}. For the second Fibonacci charge pump, a stable, high-voltage (30 V) output is obtained because a pulse skip regulator is utilized and moderate current (<1 mA) is required. Such an output is much larger than threshold voltage V_T. Thus, the turn-on resistance of M_{22} is precise as well. Fig. 10 shows that the theoretical error is within 0.12% for the output current range of 0 mA to 1 mA. The first Fibonacci charge pump sustains a wide output current range (0 mA to 10 mA), and its output voltage changes with the output current. Consequently, the turn-on resistance of M_{22} may not be precise, and 2.9% of theoretical error is observed.

V. Discussion on Circuit Design Issues

Based on the models of Dickson and Fibonacci charge pumps, the core of the charge pump in Fig. 2 is constructed for chip size and power efficiency optimization. The core only requires four external capacitors and sustains an output current that is larger than 200 μA even in low-voltage supply (VCI = 2.4 V). As the power management of a display driver IC, the core needs a stable power supply of 30 V in both light-load and full-load conditions. Two regulators, namely, pulse skip and linear, are utilized, and their performances are compared. The entire system is shown in Fig. 11. A multi-ratio setting block is added for automatic ratio selection in consideration of the different input voltages to improve ripple and efficiency performance.

A. Multi-ratio Setting

This design focuses on adjusting the topology open loop based on input voltage VCI with output current bound to 200 μA, rather than including the voltage drop in a closed loop [9] [10] or adjusting the voltage ratio by sensing the output current [11]. In this design, voltage ratios of 12, 16, and 20 are adopted depending on the alternative stage number of the Dickson charge pump. Turning points of 2.8 V and 3.3 V are selected, and the ratio setting for the total input range of 2.4 V to 3.6 V is given in Table I.

Fig. 12 shows the circuit of the multi-ratio setting block.

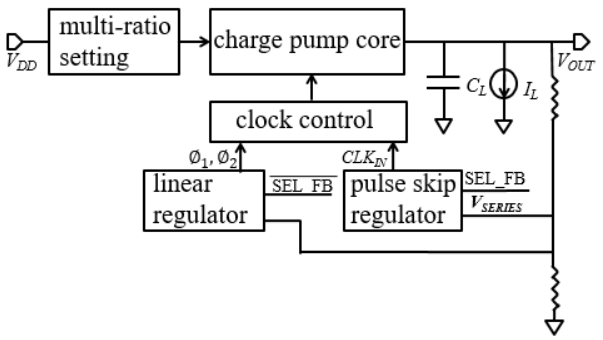


Fig. 11. Charge pump system with a feedback control circuit.

TABLE I
Multi-ratio Setting

Input voltage	2.4 V to 2.8 V	2.8 V to 3.3 V	3.3 V to 3.6 V
Voltage ratio	20	16	12

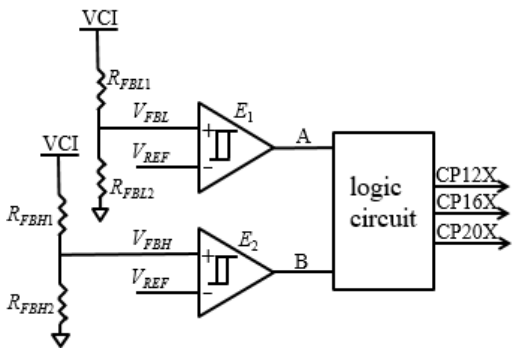


Fig. 12. Schematic of the multi-ratio setting.

TABLE II
Truth Table for Multi-ratio Setting

A	B	CP12X	CP16X	CP20X
0	0	0	0	1
0	1	X	X	X
1	0	0	1	0
1	1	1	0	0

"X" in the table means that the case never occurs.

This circuit is realized with two hysteresis comparators, E_1 and E_2, which compare the input voltage VCI with the turning points, 2.8 and 3.3 V, respectively. By operating the output signals (A and B) with the truth table shown in Table II, the enabled signals of CP12X, CP16X, and CP20X are obtained to drive the following charge pump and determine the suitable voltage ratio constantly.

The topology of the hysteresis comparator is shown in Fig. 13. For a symmetrical design, $(W/L)_3 = (W/L)_4$ and $(W/L)_6$=$(W/L)_7$. The transistors M_3, M_4, M_6, M_7 introduce hysteresis and guarantee that

$$(W/L)_6/(W/L)_3 > 1. \quad (35)$$

For the turning points of 2.8 and 3.3 V in this design, the corresponding hysteresis zones are approximately 110 mV (±55 mV) and 130 mV (±65 mV), respectively. The hysteresis zones eliminate the glitch and avoid sharp

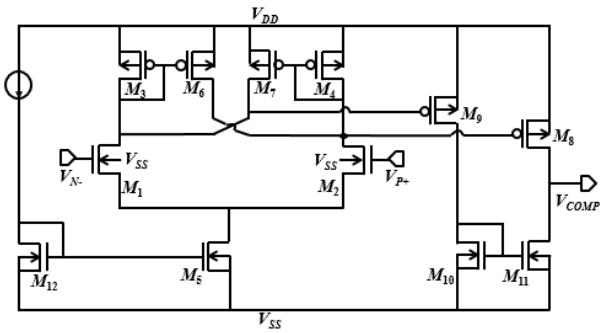


Fig. 13. Complete comparator with internal hysteresis.

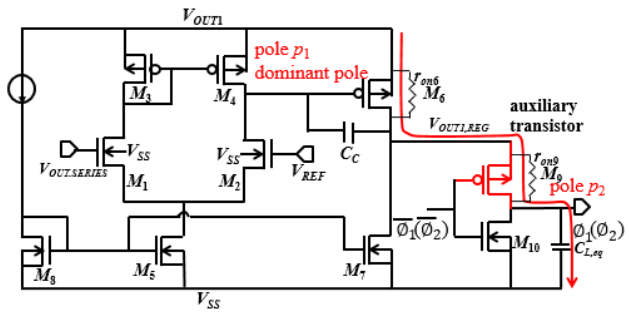


Fig. 14. Error amplifier with an auxiliary transistor in the linear regulator application.

switching when the input voltage varies around the turning points.

B. Pulse Skip Regulator

A pulse skip regulator is utilized to keep the charge pump output voltage stable at approximately 30 V. The operation mechanism of a high-speed comparator is to turn off the system when its output is higher than the target voltage and to turn on the system again when the output is below the target voltage [12]. For system stability, the poles at the output terminal V_{OUT} and the comparator circuit are significant, whereas the pole at node V_{SERIES} can be ignored. Given that the pump operates in turn on/off state, a low-frequency pole ($s = 0$) is given at V_{OUT}. When the two-stage comparator is utilized, its poles at each stage are close to each other at approximately 2 MHz. Its voltage gain is moderate at approximately 75 dB. Therefore, system stability is guaranteed.

C. Linear Regulator

A linear regulator is also adopted to further maintain the stability of the system output at approximately 30 V, as presented in Fig. 11. For the open-loop Dickson charge pump in Fig. 3, the amplitudes for clock signals $\emptyset_1$ and $\emptyset_2$ are both V_{OUT1}. As the clock signal goes down, the capacitor in the stage stores charges and then charges the following capacitor during the other phase. The function of the linear regulator is to regulate the high level of the clock signal because it controls the charges pumped to the subsequent stage to regulate the output voltage of the pump. In our

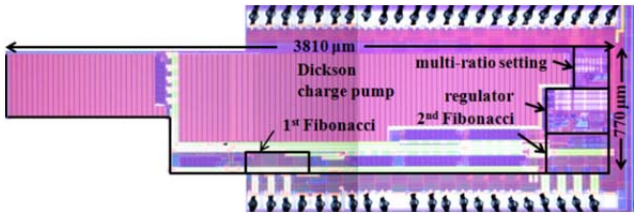


Fig. 15. Optical photograph of the die of the charge pump system.

design, a liner regulator with an auxiliary transistor [13] is used, as shown in Fig. 14. By comparing the charge pump's output and the reference voltage, the power supply of the clock buffer is generated, and the high level of the clock signal is regulated.

The charge pump core causes no stability problem for its large signal operation, and its output voltage (VCR = 20) can be estimated with state-space averaging theory in [14] as follows:

$$V_{OUT} = 20V_{CI} - 200I_L(R_{X1} + R_{Y1}) - 2I_L(R_{X2} + R_{Y2}) - 4I_L/f \cdot \sum_{i=1}^{4} 1/C_{di}, \quad (36)$$

where $R_{x1}, R_{Y1}, R_{x2}, R_{Y2}$ are the on-resistance of the two Fibonacci charge pumps for each phase and $C_{di}(i = 1,2,3,4)$ defines the corresponding flying capacitance in each stage of the Dickson charge pump.

For the error amplifier, its dominant pole p_1 and non-dominant pole p_2 are set to

$$p_1 = 1/(2\pi \cdot A_{v2} \cdot C_c \cdot r_{out1}), \quad (37)$$

$$p_2 = g_{m6}/(2\pi \cdot C_{L,eq}), \quad (38)$$

where g_{m6} and A_{v2} are the input transconductance and voltage gain of the second stage, respectively. $C_{L,eq}$ is the capacitance of two series flying capacitors. r_{out1} is the output resistance of the first stage.

In this design, three stages of the Dickson charge pump are regulated. This pump system suffers from poor stability with light load assuming a load current = 4 μA for the consumption of the driver, and 42° phase margin with direct current gain = 96 dB is measured for equivalent series resistance = 0 Ω.

Considering that the turn-on resistors of auxiliary transistor M_9 and power-switching transistor (defined as r_{on}) are connected in series with the equivalent load capacitor, $C_{L,eq}$, a negative zero, as given in Equ. (39), is introduced to improve system stability.

$$z_1 = -1/(2\pi \cdot r_{on} \cdot C_{L,eq}) \quad (39)$$

VI. Silicon Results and Evaluation

Fig. 15 shows the complete die photograph of the charge pump system fabricated through a 0.11 μm process. The complete system, including charge pump core (Dickson and Fibonacci), multi-ratio setting, and regulator, occupies 3810 μm × 770 μm.

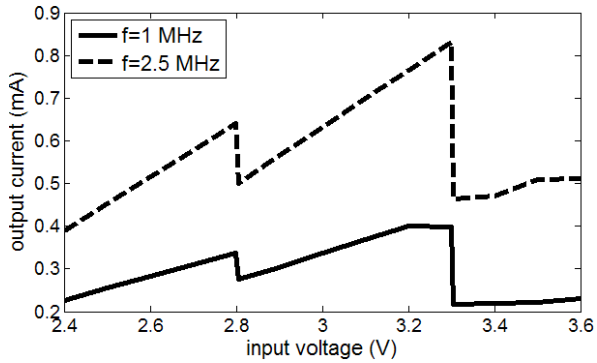


Fig. 16. Maximum output current performance of the charge pump.

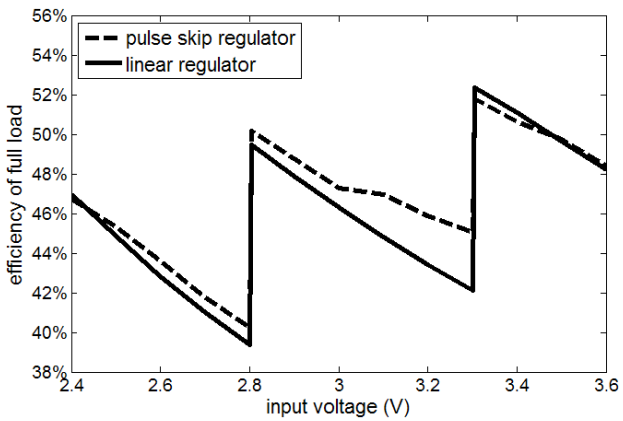
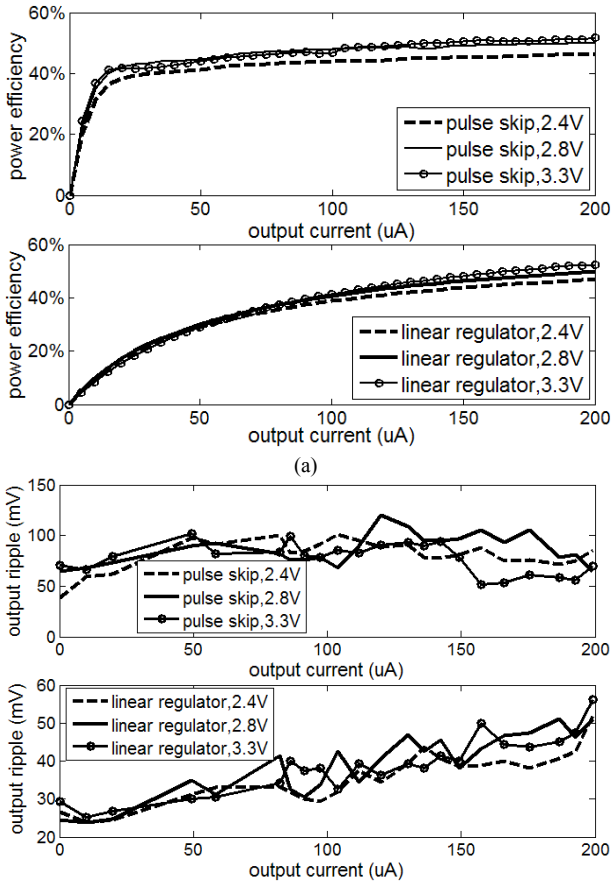


Fig. 17. Efficiency of the charge pump at load current = 200 μA.

In this design, the operation frequency of the Dickson charge pump is set to the default value of 1 MHz. A proper large frequency will result in a small chip size proportionally. The capacitances C_3, C_L in Fig. 3 are selected as 0.1 μF for cost saving, although it affects the ripple performance. The measured results with the multi-ratio setting are given below.

The performance at the maximum output current is shown in Fig. 16. For 30 V output voltage with default 1 MHz operation frequency, a current of 226 μA can be supplied even in low input voltage (2.4 V). For 2.5 MHz operation frequency, this charge pump system can supply at least 390 μA current, and its corresponding efficiency is close to the default one. Thus, a proper high operation frequency can increase the output current drivability, and a small chip size can be obtained in further design with the same performance. For the following measured result, the operation frequency is set to 1 MHz. While the pulse skip regulator is utilized in the first Fibonacci charge pump to guarantee middle voltage (6.2 V for more margin) for the following Dickson charge pump to reduce the chip size, the output current increases gradually when input voltage $\mathrm{VCI} > 3.2\,V$ because the regulator functions and decreases the output of the first Fibonacci charge pump to a value within 6.2 V.

The power efficiencies of the two regulators for various input voltages are compared in Fig. 17. With a load current of



(a)

(b)

Fig. 18. (a) Efficiency and (b) ripple of the charge pump at all load conditions at VCI = 2.4 V, VCR = 20, VCI = 2.8 V, VCR = 16, VCI = 3.3 V, and VCR = 12.

200 μA, the power efficiency of the two regulators remain above 39%. The linear regulator manifests poor efficiency with approximately 1% decrease but retains a small ripple.

The power efficiency and output ripple at various load conditions are compared in Fig. 18. Compared with the linear regulator, the charge pump maintains high efficiency even under a light load. In the full-load condition, they are close to each other, that is, approximately 48%, 50%, and 52% for VCI = 2.4, 2.8, 3.3 V, respectively. With regard to ripple performance, the linear regulator has a smaller ripple (<60 mV) than the pulse skip one (as large as 120 mV).

For the performances in line regulation, with the input voltage changing from 2.4 V to 3.6 V (full load = 200 μA; smaller loop gain, worst case), the line regulations are 50 and 40 mV/V for the pulse skip scheme and the linear regulator, respectively. For load regulation, with the load current changing from 0 μA to 200 μA, the corresponding load regulations (VCI = 3.0 V case) are 480 and 500 mV/mA.

VII. Conclusion

A novel charge pump that caters to display driver IC with

30 V output voltage and moderate current drivability (larger than 200 μA) was developed. The design focuses on reducing the components to fit small-package applications, and only four external capacitors are required. The proposed design utilizes a Fibonacci charge pump to generate the power supply for driving the following Dickson charge pump to enhance its gate drive. A pulse skip regulator is used in this Fibonacci block to generate middle voltage to drive certain devices, and more than 30% of the chip area is saved. This design results in minimal current drivability loss when the input voltage is larger than 3.2 V. For the Dickson and Fibonacci charge pumps, simple and precise models were proposed and proven to be useful for further chip size and power efficiency optimization. With regard to system stability, a pulse skip regulator and a linear regulator were utilized. Their performances in ripple, efficiency, load regulation, and line regulation were compared. The two systems maintain high efficiency (>39%) for various input voltages with full load. The pulse skip regulator maintains high efficiency even in a light-load condition, but it exhibits poor ripple performance (as large as 120 mV). By contrast, the linear regulator is superior, particularly in light-load conditions (25 mV).

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