JPE 16-2-30

http://dx.doi.org/10.6113/JPE.2016.16.2.704
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Single-Phase Inverter for Grid-Connected and Intentional Islanding Operations in Electric Utility Systems

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Abstract

Small distributed generation units are usually connected to the main electric grid through single-phase voltage source inverters. Grid operating conditions such as voltage and frequency are not constant and can fluctuate within the range values established by international standards. Furthermore, the requirements in terms of power factor correction, total harmonic distortion, and reliability are getting tighter day by day. As a result, the implementation of reliable and efficient control algorithms, which are able to adjust their control parameters in response to changeable grid operating conditions, is essential. This paper investigates the configuration topology and control algorithm of a single-phase inverter with the purpose of achieving high performance in terms of efficiency as well as total harmonic distortion of the output current. Accordingly, a Second Order Generalized Integrator with a suitable Phase Locked Loop (SOGI-PLL) is the basis of the proposed current and voltage regulation. Some practical issues related to the control algorithm are addressed, and a solution for the control architecture is proposed, based on resonant controllers that are continuously tuned on the basis of the actual grid frequency. Further, intentional islanding operation is investigated and a possible procedure for switching from grid-tied to islanding operation and vice-versa is proposed.

Key words: Distributed power generation, Intentional islanding operation, Single-phase inverters, SOGI-PLL, Tuned resonant controller

I. INTRODUCTION

Distributed generation based on consumer-owned generation units is spreading all over the world to meet the increasing energy demands as well to reduce the environmental impact of fossil fuel based power generation. With respect to conventional electric power plants, which are generally located far from load areas, distributed generating units are normally easy to install at the distribution level, close to energy end-users, and able to integrate different types of energy generators (photovoltaic arrays, wind turbines, small hydro turbines, fuel cells, etc.) [1], [2]. However, due to differences in their intrinsic natures and variable output voltages, as well the desire to achieve the maximum power extraction, these sources are commonly coupled by means of specific converters to a common DC bus. This distributed DC bus is then connected to the grid with a suitable power electronic converter. Among the power electronic converter topologies, the single-phase voltage source inverter (1PH-VSI) configuration is frequently used as a power interface for low power consumer-owned renewable generators.

The power interface mainly supplies active power to the grid. However, European Standard EN 50438 prescribes supporting the grid quality of service by also sourcing or sinking reactive power, as well as allowing the inverter to operate in local islanding mode in order to minimize possible power outages.

The quality of the produced energy relies on both the hardware (HW) and software (SW) architectures. From the

Manuscript received Apr. 22, 2015; accepted Sep. 22, 2015
Recommended for publication by Associate Editor Jae-Do Park.
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SW point of view, in order to assure a low current-total harmonic distortion (THD) in the grid-tied mode, as well as a low voltage-THD when supplying non-linear loads in the intentional islanding mode, resonant controllers were demonstrated to be more effective [3], [4] with respect to standard PI controllers in the synchronous frame.

This paper describes solutions for a hardware topology as well as a control architecture for a single phase inverter in order to achieve low current THD during grid-tied operation and low voltage distortion in the islanding mode. A dedicated single-phase PLL operating with a proper islanding detection algorithm is illustrated in the proposed work. A voltage and current low THD control strategy is also presented. It is composed of a single control loop that is continuously tuned to follow grid frequency variations in order to overcome the potential degradation of the regulation performance [4]. The same control structure is proposed for used in both the grid-tied and islanding modes of operation. A suitable LC filter topology is suggested in order to achieve high filtering capabilities [5] in both the grid-tied and stand-alone modes of operation.

The proposed 1PH-VSI is expected to draw energy from the distributed generation DC common power bus, where various types of generating and storage units can be connected in a microgrid-like configuration. For this reason, the system architecture is conceived to receive a high level directive, as the active and reactive power amount to supply, from a higher order level entity. In this scenario, it can be identified in the integrated manager as the one in Fig.1. This entity acts in order to coordinate the distributed generation nodes and to provide a control interface between a microgrid, the end-users and the distributor [6], [7].

II. 1PH-SVS Topology

In this section, the HW structure of the proposed inverter is described. Several HW topologies and output filter configurations have been proposed in the literature. For the proposed application, a 3-level neutral point clamped full-bridge topology and a LC filter equipped with both damping and trap sections are chosen.

A. Inverter Topology

Low power (<10 kW) distributed power generation clusters are usually connected to the ac grid by means of a 1PH-VSI at a low voltage level (230 V). Over the years, many VSI hardware topologies have been investigated in the literature. Among them, the most commonly used are the half-bridge (HB) and full-bridge (FB) configurations. With respect to the HB configuration, the FB configuration uses twice the number of switches. On the other hand, the FB topology does not need a split dc link capacitor and it is allowed to operate with half the dc link voltage. Consequently, the voltage stress on the switches is reduced. This allows for the use of reduced

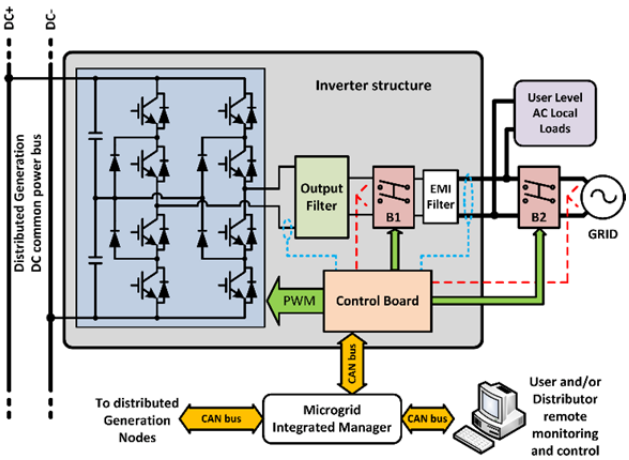


Fig. 1. 1PH transformer-less 3-level NPC FB configuration.

rating power modules (or devices) which in turn results in lower switching and conduction losses. Additionally, the use of a lower voltage dc power source presents some advantages. For example, it opens up the possibility of reducing the number of units in the series connection in a photovoltaic array, as well as enhancing the reliability and fault tolerance of the system. Additionally, the FB configuration, in combination with unipolar pulse width modulation, allows for effectively doubling the output switching harmonics to twice the switching frequency. In this way, it is possible to either reduce the size of the filtering passive components or to limit the amplitudes of the voltage and current ripples, achieving loss reductions and increased conversion efficiency.

Both the HB and FB topologies are easy to arrange in multilevel configurations. Concerning the FB configuration, the use of a 3-level topology further halves the voltage stress on the switches. In 230 V ac output (i.e. 325 V_{pk}) applications, a 390 V dc-link is high enough to assure the desired output voltage. As a result, the voltage across a 3-level FB single switch is less than 200 V, which allows for the use of future power MOSFET switches rather than IGBTs. As previously mentioned, a 3-level topology, using the same passive components as the 2-level topology, shows half the voltage and current ripples and a consequent reduction in the losses in the switches and hardware filters which increases the efficiency [8], [9]. With reference to the previous discussion, a 3-level neutral point clamped (NPC) FB topology, which is depicted in Fig. 1, is chosen in order to achieve high efficiency as well as a ripple reduction.

B. Output Filter Configuration

The grid connection of the proposed VSI configuration is achieved by means of a passive output filter rather than a transformer. In fact, the insulation provided by a transformer is not needed in most home installations. Therefore, a passive output filter represents a solution balanced between costs, efficiency and performances. Unlike inverters with an output line transformer, transformer-less inverters have reduced

dimensions and weight, making them suitable for use in home appliances at a reasonable cost. In addition, they show better efficiency due to the absence of transformer related losses.

Several filter configurations for grid-tied inverter applications have been discussed in the literature. The most widely used circuital schemes are the LC and LCL filters [10]. An LCL type filter is recommended in particular for grid connected applications, since the presence of a second inductor makes the filter response more immune to grid parameters variations. This configuration makes it possible to obtain an output ripple current that is extremely reduced using inductors with a relatively small value when compared to those of LC configurations with similar performance. However, an excessive reduction of the inverter side inductor significantly increases the current ripple flowing through the power electronic devices.

Recent publications have introduced a filter configuration derived from an LCL which is referred to as the LLCL [11]. In this configuration, the capacitor is replaced with an LC series circuit that is tuned to resonate at the switching frequency. The presence of the LC circuit is intended to present a quasi-zero impedance path for the residual switching component flowing in the main inductor. This feature, causes the output switching component to be greatly reduced when compared to a conventional LCL filter with same values. It also causes a reduction in the filter roll-off due to the high impedance of the LC series circuit at a high frequency.

An alternative to the above mentioned configurations is an LC filter followed by a trap filter section [12]-[14] which is tuned at the output line current ripple frequency. In the investigated application, the effect of unipolar PWM modulation assures that the trap filter is tuned at twice the switching frequency. This filter gives a quasi-zero impedance path for the fundamental switching component of the output current, and it is proposed to reduce the switching ripple injected into the grid. In this way, results similar to those of an LLCL filter can be achieved, while using only one line current sized inductor. However, the characteristic frequency of the LC filter requires it to be suitably damped through a proper resistor, and to be placed either in parallel or in series with respectively the LC inductor or capacitor. Conventional schemes show this resistor in series with the capacitor. When the resistor is sized for a Butterworth-type response, the filter roll-off at a high frequency decays from -40dB/dec to nearly -20dB/dec. This drawback can be avoided by using a properly tuned series RLC circuit section to selectively damp the LC characteristic resonance. In fact, with respect to its resonance frequency, a series RLC circuit shows a high impedance at low and high frequencies and an impedance equal to R at the resonance frequency. For these reasons, the proposed inverter is equipped with an output LC filter selectively damped by means of a suitably tuned circuit and followed by a tuned trap filter section as depicted in Fig. 2. The presence of the selective damping circuit allows it to effectively damp the LC filter while assuring the standard -40dB/dec roll-off at high frequencies, as shown in Fig. 3.

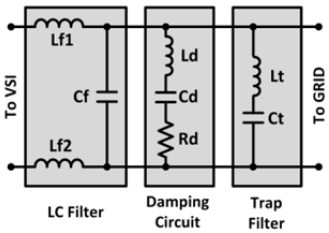


Fig. 2. 1PH transformer-less inverter output filter topology.

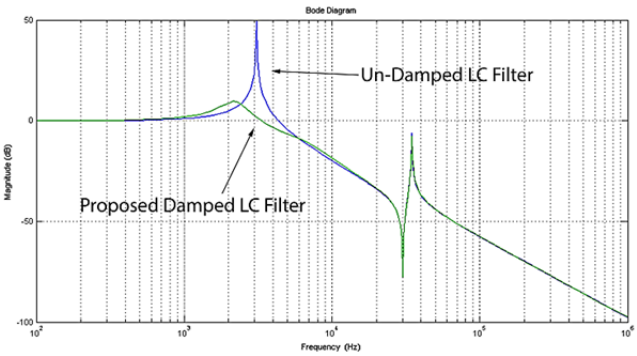


Fig. 3. Simulated LC+trap filter frequency response with and without damping circuit.

TABLE I
1-PH NPC FB COMPONENTS

L_{f1}, L_{f2}	1mH
C_f	1uF
L_d	1mH
C_d	1.2uF
R_d	40Ω
L_t	85µH
C_t	0.33µF
V_{DC}	390V
$C_{DC\text{-}Link}$	400µF
$V_{AC\text{-}RMS}$	$230V_{RMS}$
IGBT Phase-Leg Module	APTGF50TL60T3G
Rated Power	3.5kW

The maximum current ripple value is considered as the specification for the Lf1 and Lf2 inductors sizing. A filter cut-off frequency of approximately 3 kHz gives the desired value of the capacitor C. The cut-off frequency is chosen for the purpose of assuring that there is enough attenuation at a switching frequency of 15 kHz, to provide high bandwidth control and to reduce size of the passive components. The selected values for both the passive components and the power electronic devices of the proposed 1PH NPC FB prototype, are listed in Table I. In the proposed application, the output LC filter is used in conjunction with a commercially available EMC filter, in order to reduce the

common mode current and very high frequency remaining ripples.

III. Control Architecture

The control architecture scheme for the proposed 1PH-VSI is depicted in Fig. 4. Voltage and current measurements from the transducers located in the power layer are acquired, properly scaled and conditioned by the measures acquisition block. The phase-locked loop (PLL) algorithm generates a synchronism signal related to the grid electrical angle and estimates the grid frequency to be used as a reference by the voltage and current loop block, the system supervisor block and the reference generator block. The system supervisor has monitoring and control tasks. It monitors the VSI inputs and outputs (the dc-link voltage, output line current, and leakage current), the measured grid voltage and the frequency previously estimated by the PLL. It also commands a disconnection of the VSI from the grid when a fault condition is found. In addition, in coordination with the active islanding detection, it provides actions in the case of islanding by using both active and passive detection methods.

The system supervisor block acts as a bridge between the VSI and the microgrid integrated manager through a CAN bus, making all of the acquired measures available to the end user and acquiring the high level requests of the active and reactive power.

The reference generator block generates the reference signals for the voltage and current loop. In fact, based on the possibility of operating in either the grid connected or islanding mode, the 1PH-VSI has to act as either a current or a voltage generator, respectively.

The active and reactive power references from the system supervisor are translated, by means of the grid parameters estimated by the PLL, to sinusoidal reference signals for the control loop. In particular, when operating in the grid-tied mode, the reactive power is regulated, on the basis of the grid distributor requests, by properly shifting the current reference with respect to the PLL estimated grid reference angle. In the intentional islanding mode of operation, the proposed VSI acts as a voltage generator. Thus, exchanged reactive power is a consequence of the connected loads requirement. Under this condition, the inverter can operate even with very low power factor values within the limits of the maximum allowable output current peak value. The PWM signals for the power layer are generated through a 3-level modulator on the basis of the phase disposition modulation. The switching frequency is set to 15 kHz, meaning that the first harmonic in the output ripple is at 30 kHz. This is due to the unipolar PWM scheme.

The behavior of the proposed 1PH-VSI changes from the current generator mode to the voltage generator mode, and vice-versa, requiring a switch between the current and

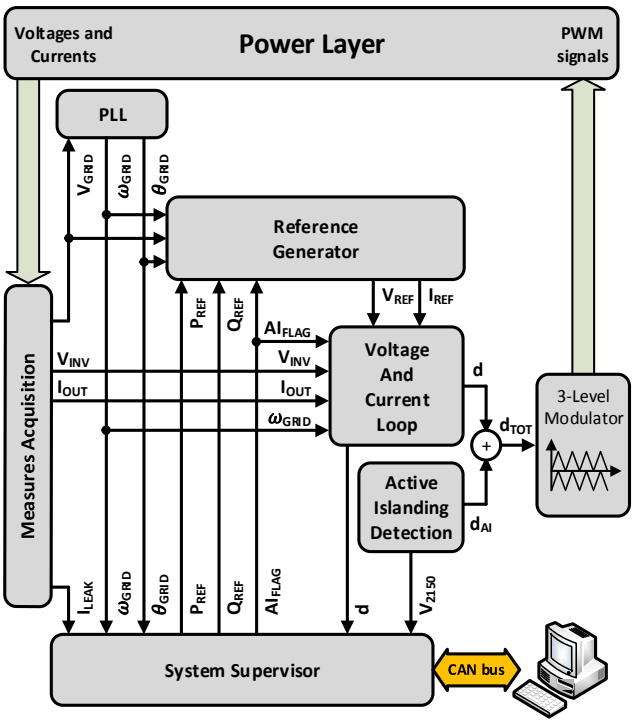


Fig. 4. Proposed control architecture.

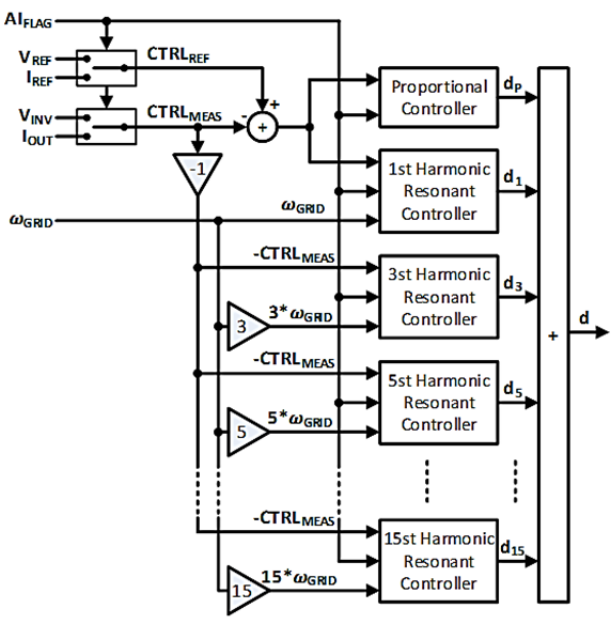


Fig. 5. Proposed Voltage and Current Loop block architecture.

voltage measures and references. Accordingly, the control gains and tuning parameters need to be changed due to modifications in the system equivalent transfer function. For these reasons, the voltage and current loop has an islanding detection flag input (AI_{flag}), which allows the control loop to re-configure itself according to the requested operating mode. The implemented voltage and current loop block scheme is depicted in Fig. 5, where a proportional-resonant configuration is applied. Resonant controllers, also referred to as harmonic compensators, are a relatively novel and

promising type of controllers [15]-[19]. They work in the stationary frame and, in the parallel configuration shown in Fig. 5, can ensure low THD values even in the case of heavily polluted grids.

Resonant controllers have the same transfer function as notch filters with extremely selective behavior. In order to obtain low THD values and avoid reciprocal mis-interactions, they need to be properly tuned at the grid fundamental frequency and its multiples of interest. Because the grid frequency is not constant, in a fixed frequency tuned regulators scenario, the effectiveness of the resonant controllers rapidly decreases as the grid frequency drifts from its rated value. Auto-tuning resonant controllers have been discussed in the literature [15]. However, instead of adding an additional integrator and a feedback loop, the investigated 1PH-VSI adopts resonant controllers with online tuning capabilities based on the PLL-estimated grid frequency. A Second Order Generalized Integrator (SOGI) [16] is used to generate two quadrature signals, starting from the single phase voltage measure. These signals are then fed to a standard Park-type PLL. The whole control algorithm runs synchronously with PWM at a sampling frequency of 15 kHz and is implemented on a designed control board, which is equipped with all of the necessary analog circuitry for measures acquisition, power supply, and data exchange interfaces. The board uses a Texas Instruments TMS320F28335 DSP, which runs the entire control algorithm within a switching period. The voltage and current loop, based on an on-line tuned resonant controller, is discretized with the Tustin discretization method with the addition of a pre-warp factor. The same discretization method is also used for the PLL and islanding detection algorithms that are illustrated in the next sections.

IV. Phase-Locked Loop

One of the main sections of the control architecture is the PLL. Measuring the grid line voltage allows the PLL algorithm to generate the electrical angle required for the generation of the voltage and current references, as well to provide a reliable measure of the grid frequency for resonant controllers tuning and system supervisor monitoring purposes. The most common type of PLL algorithm is based on the use of the Park transformation and is depicted in Fig. 6. However, its application to single-phase systems requires the generation of two signals that are 90 degrees phase shifted, as expected by the Park transformation.

As previously mentioned, a Second Order Generalized Integrator (SOGI) [20]-[23] is used for this purpose in the described activity. This type of quadrature signals generation (QSG) is preferred with respect to the transport delay for two main reasons. First, the transport delay requires storage memory for sampled measurements and this memory has a

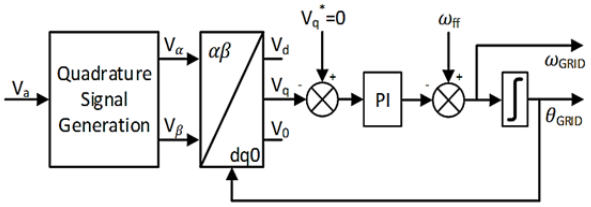


Fig. 6. Single-phase PLL structure.

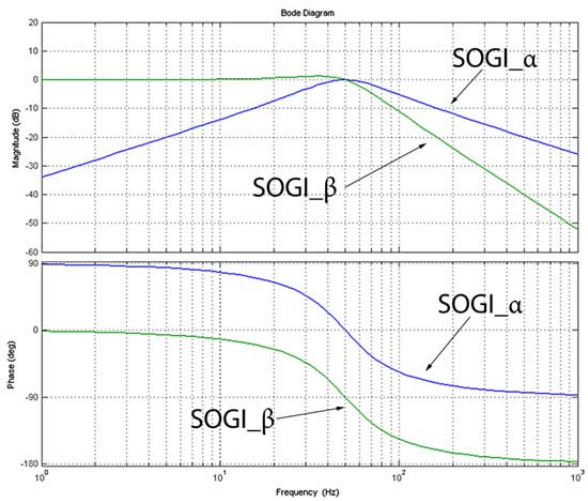


Fig. 7. Bode plot of SOGI 90 degrees phase shifted signals.

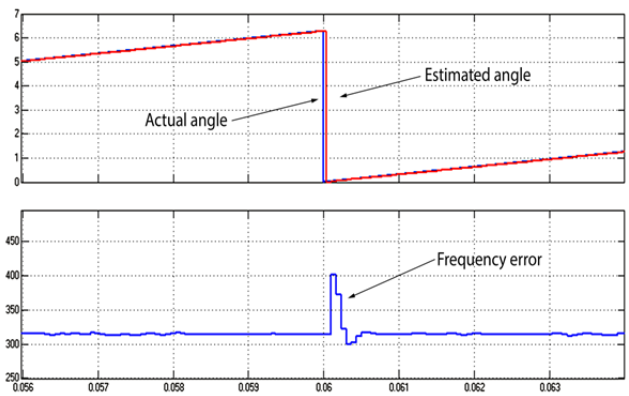


Fig. 8. Estimated frequency error due to reset delay.

static dimension. This second characteristic requires a constant measured grid frequency to make the PLL work properly. However, this is impossible in practice because the grid frequency varies continuously within the admitted values of international standards. Second, a QSG based on a SOGI allows for obtaining acceptable 90 degree phase shifted signals (1) and (2), as is shown in Fig. 7, in a sufficiently wide range of working frequencies and centered on the rated grid frequency.

$$H_\alpha(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \quad (1)$$

$$H_\beta(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \quad (2)$$

The filtering effect of two channels of SOGI also makes

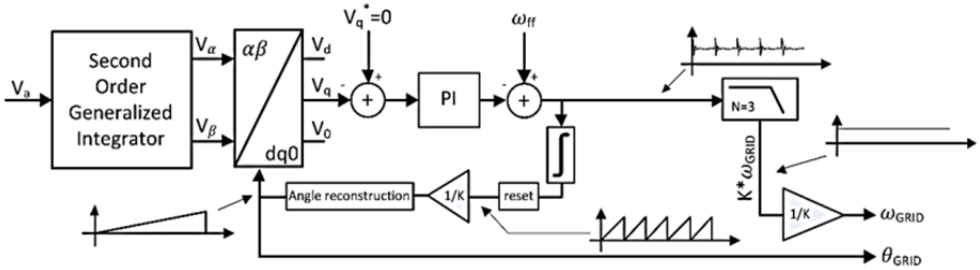


Fig. 9. Modified PLL structure.

the PLL more immune, when compared to two standard PLLs, to two voltage harmonic distortion often related to the presence of non-linear loads. This allows for correct operation even on heavily distorted grids.

However, processing the digital implementation of a PLL produces some undesired effects during the reset action of the electrical angle. This is mainly due to the discretization process of the control algorithm. In fact, with respect to Fig. 6, in order to limit the span of the grid angle to the range 0-2π, a reset procedure is implemented in the integrator block. Due to the discrete time nature of control algorithms, the reset action from 2π to 0 of the electrical angle variable occurs with a maximum delay of one sampling period. In the proposed system this is equal to the inverter switching period.

As a result, a significant error is generated in the main frequency estimation of any reset action, as shown in Fig. 8, where the grid frequency is set to 50 Hz (i.e. 314.16 rad/s). The amplitude of this error depends on two PLL's PI regulator bandwidth. A fast tracking PLL (i.e. a high bandwidth PI) shows a larger error amplitude when compared with a slow tracking PLL. In fact, it temporarily increases the estimated frequency in order to make the estimated grid angle reach the actual grid angle. Then, it settles at the actual frequency value. Despite these characteristics, a fast tracking PLL is preferable due to its ability to accurately follow grid changes and detect the islanding condition. The fast PLL performances are not affected by the estimated frequency error, since it occurs for a very short time with respect to the main grid period. However, the achieved error amplitude in the frequency estimation is not suitable for the online direct tuning of the control loop regulators, as previously discussed in Section III.

The estimated frequency signal can be filtered by means of a low cut-off frequency filter. However, the resulting discretization error significantly affects the results. Further, the adoption of a very low cut-off frequency filter compromises the proper detection of grid frequency variations because of grid faults. Oversampling can dramatically reduce the estimated frequency error in the PLL algorithm section. It also provides very stable information about the estimated frequency. However, oversampling requires that the PLL algorithm be executed on a time basis other than the one used for the control algorithm. Therefore, a multiple interrupt digital control architecture is required. Commercially available DSPs with cost/performance characteristics suitable for 1PH-VSI applications show limited computational capabilities in terms of multiple interrupt control architectures.

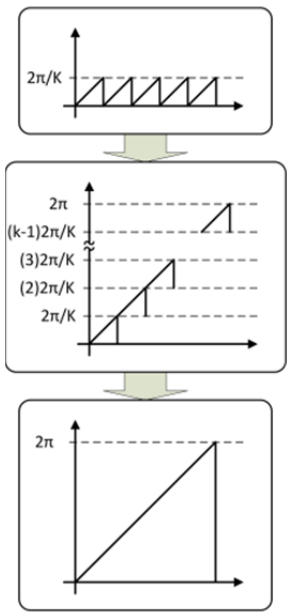
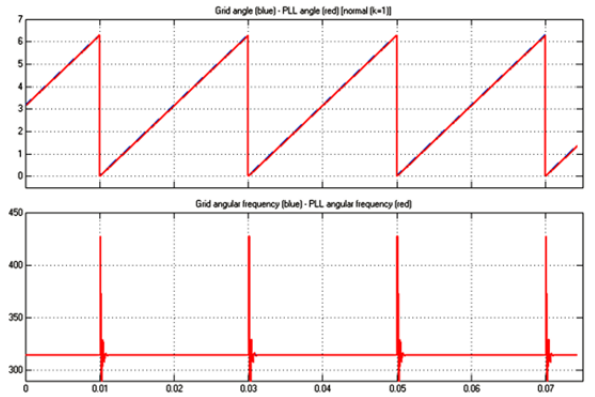


Fig. 10. Angle Reconstruction block operation.

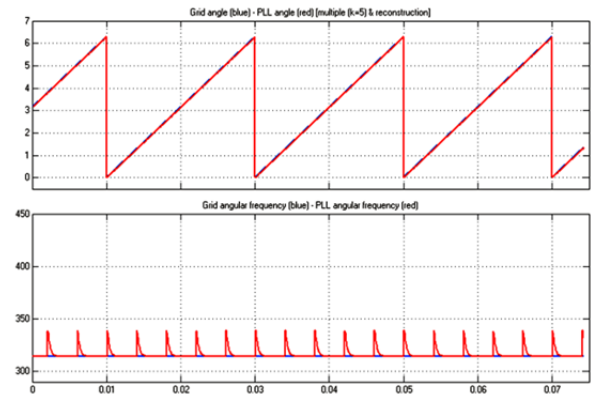
A more effective solution to reduce the estimated frequency error is achieved through a modification of the conventional PLL structure as depicted in Fig. 9. The resulting frequency estimation can be suitably used in the voltage and current loop compensator tuning as well as for monitoring and protection purposes.

A gain of 1/K is introduced in the feedback loop. As a result, the input of the integrator block is forced to be a frequency K-times multiple of the grid frequency. The modified PLL locks at K-times the grid frequency, and the reset of the integrator still occurs when it reaches 2π. Then, an additional block is used to reconstruct the correct grid angle.

This task is performed by the angle reconstruction block, whose operation is illustrated in Fig. 10. The reset of the integrator in the proposed method occurs at K-times the fundamental frequency. This makes it easier to filter out the estimated frequency errors previously shown in Fig. 8. As a result, high values of the K parameter have the benefits of



(a)



(b)

Fig. 11. PLL simulation results. (a) SOGI + Park Transformation PLL. (b) SOGI + Park Transformation PLL with modified feedback loop (K=5).

increasing the estimated angle reset frequency and reducing the amplitude of the generated frequency error.

However, the K value should be limited in order to avoid interference between two consecutive reset actions, as shown in Fig. 11(a).

As a tradeoff in terms of the above mentioned effects, K=5 is chosen in the proposed 1PH-VSI.

Simulation results for both the SOGI + Park Transformation PLL and the SOGI + Park Transformation PLL with the proposed modified feedback loop are depicted in Fig. 11(b). In the proposed PLL, the estimated frequency errors due to the reset of the integrator are successfully filtered even with a low order low pass filter with a relatively high cut-off frequency.

V. Islanding Detection

In residential distributed generation scenarios, it is important that the protection algorithms exhibit a high degree of reliability. In addition to the basic protections relating to the identification of network off-specifications or malfunctions, such as under voltage/over voltage detection algorithms, the recognition of islanding operation is essential, both when islanding is forbidden and when it is allowed. In the first case, fast disconnection action is required according to the imposed standards [24]. In the second case, the inverter has to switch as fast as possible to voltage mode control, in order to supply local islanded loads, and to separate the isle from the out-of-service grid.

Based on these assumptions, the proposed inverter is equipped with multiple islanding condition identification schemes, which include both active and passive detection methods. When connected to the grid, the proposed 1PH-VSI acts as an ideal current generator, where the amplitude of the current injected into the grid is set by a microgrid integrated manager, and modulated on the basis of the actual energy production of the other generation nodes and limits imposed by the distributor. This means that when disconnected from the grid, but not from the loads, the VSI keeps trying to push the previously set current at its output, acting in variation with its internal duty cycles. There are three possible scenarios, when the power required by the loads is lower than the actual output power of the inverter, when the power required by the loads is higher than the actual output power of the inverter, and when the power required by the loads is in the order of the actual output power of the inverter.

In the first case, the loads act as a sort of large value resistor, in order to maintain the output current, and the VSI is forced to increase its output voltage, which saturates its internal duty cycles. In the second case, the loads act as a sort of low value resistor. In this case, the inverter reduces its output voltage, leading to abnormally low internal duty cycles and an abnormally low output voltage. In the third case, before entering islanding, the inverter was providing the same amount of power required by the local loads. This represents the worst case because apparently nothing happens to the duty cycle or to the output voltage if they remain within the normal range. For this reason, the islanding condition cannot be detected through duty cycle monitoring. To avoid this issue, it is possible to exploit the feed-forward grid frequency (ω_{ff}) input of the PLL shown in Fig. 9, making it possible for the inverter to detect the islanding condition even in the previously discussed worst case. In fact, when the grid is present, the PLL tries to lock at ω_{ff}. However, due to the presence of the grid this is not possible and the PLL is forced to lock at the grid frequency instead of ω_{ff}. When the inverter is operated in the islanding mode, the PLL still tries to lock at ω_{ff}. As a result, due to the absence of the grid, the output voltage frequency drifts toward ω_{ff} with a rate of change that depends on the connected loads and the tracking PI parameters.

Using this characteristic and setting the value of ω_{ff} above the maximum grid frequency imposed by international regulations, it is possible to automatically drive the inverter in the off-specification over-frequency point of operation, which allows the supervisor to recognize the anomaly.

However, during frequency drift transients, the

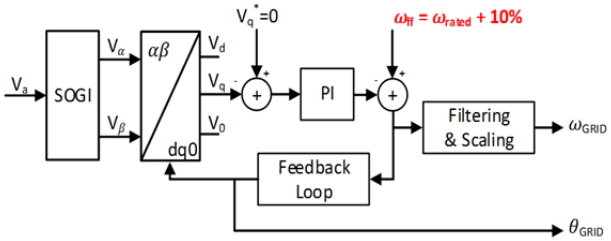


Fig. 12. Frequency Drift islanding detection.

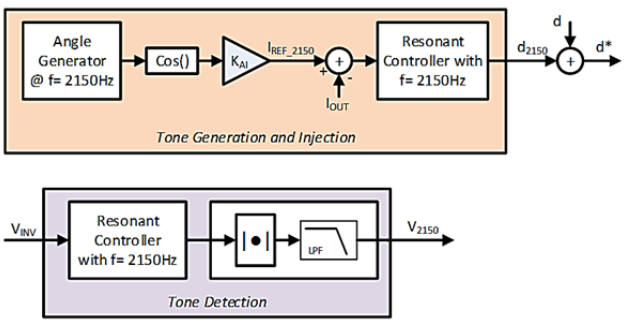


Fig. 13. Active islanding detection with fixed frequency injection.

instantaneous voltage and current frequency should not damage the connected loads. Hence, as a trade-off value between safe operation and accurate islanding detection, ff has been set to 110% of the rated grid frequency.

This method is known as "frequency drift", and it is the simplest implementation of a more complex family of islanding detection algorithms based on frequency drifting techniques [25]-[28]. With respect to the active frequency drift algorithm, this method has a simpler implementation, is not influenced by dead time related effects and does not introduce degradation into the output current quality, even if its performances are more dependent on local grid parameters. Fig. 12 shows how this type of islanding detection scheme can be added to the proposed PLL structure, when the feed-forward grid frequency (ω_{ff}) is set at 110% of the rated grid frequency.

In terms of duty cycle observation, this method also has a weak point since the "drift rate" depends on the connected loads (the type and required power). This means that, under particular conditions, the tripping time may be larger than the one allowed by the standards. For this reason, an additional active islanding detection method [29]-[32] has been added in the proposed 1PH-VSI. The 1PH-VSI injects a small current at a fixed frequency into the grid and "searches for" this frequency in the grid voltage. In case of a grid connection, negligible voltage contributions at the injection frequency are found due to the grid's small impedance. However, when the grid is absent (i.e. in the islanding operation), the small injected current causes a significant voltage contribution at the injection frequency. As a result, the no grid condition can be quickly detected. Common techniques use FFT algorithms to detect the injected tone on the grid voltage. However, a

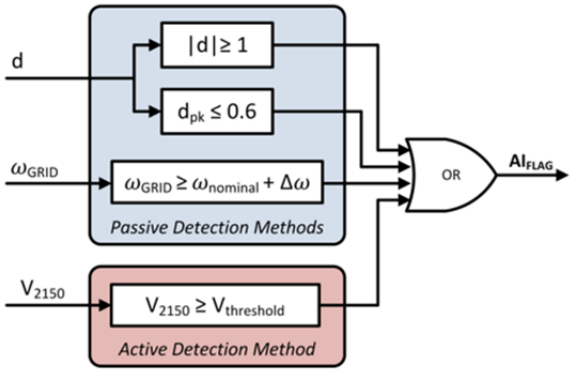


Fig. 14. Block diagram of islanding detection algorithm.

simpler and effective algorithm can be used. The proposed strategy uses a fixed tuned resonant controller to inject a test current into the grid, as depicted in Fig. 13. The amplitude of this current is selected by the K_{AI} parameter in order to be adapted to the grid voltage pollution. The frequency of the injected current is chosen to be 2150 Hz in order to not deteriorate the current THD calculated in the frequency span prescribed by current standards. Moreover, the selected injected frequency should not be attenuated by the output power filter. Therefore, it must be designed accordingly as depicted in Fig. 3. The use of a resonant controller, rather than fixed duty cycle injection, allows for keeping the test current amplitude as small as needed. Meanwhile, the inverter control algorithm and modulator apply the duty-cycle based on the grid passive parameters and operating conditions.

In order to detect a test frequency in the grid voltage, the highly selective filter nature of a resonant controller can be used as a replacement for complex FFT algorithms. In fact, the resonant controller employed for the generation of the injection test current is suitable for detecting the voltage contribution at the injection frequency at the inverter outputs. The achieved measure of the detected voltage is then scaled to compensate the resonant controller gain. Then, it is rectified and filtered to extract the DC value. Fig. 13 shows the details of both the injection and detection procedure schemes.

The output of the tone detection section, the duty-cycle value from the voltage and current loop, and the PLL estimated grid frequency are routed to the system supervisor block that monitors these parameters to find one of the previously illustrated islanding "evidences". When one of these evidences is found, the supervisor reacts to manage the islanding condition. A block diagram of the islanding detection algorithm implemented in the system supervisor is depicted in Fig. 14. In the proposed application, the frequency deviation Δω is chosen to be equal to 1% of the rated grid frequency value as trip threshold. Unexpected low and high duty-cycle peak values of 0.6 and 1 are chosen as the peak values, respectively. In this way there is no risk of spurious tripping during grid voltage sags. Regarding the

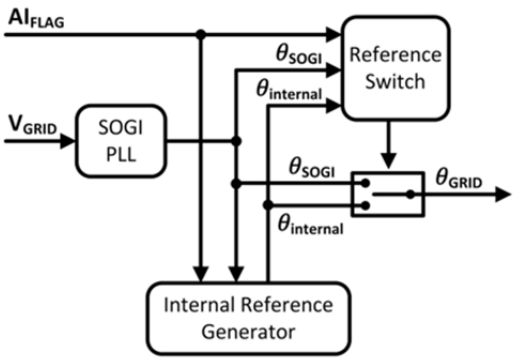


Fig. 15. Generation of the reference angle for Grid-Tied and Intentional Islanding operation.

active detection scheme, the detected test-tone threshold voltage is regulated on the basis of the dedicated resonant controller parameters at about 7V.

VI. Intentional Islanding Operation

Recent modifications in international standards have introduced the possibility to intentionally operating in the islanding mode, in order to supply privileged loads instead of using UPS systems. In addition, some control structures for 3-phase inverters able to operate in the islanding mode have been proposed in the literature [33]. However, these algorithms have no harmonic compensation capabilities when non-linear loads have to be fed. As previously mentioned, the proposed 1PH-VSI has the ability to operate in both the grid-tied mode and the islanding mode. This result is obtained by properly managing detected islanding events and switching between the two modes of operation. To operate in the islanding mode, the proposed VSI uses an internal fixed-frequency reference angle generator until leaving the islanding mode of operation. This internal generator, when in the grid-tied mode, is always synchronized with the actual grid angle coming from the PLL block. When the islanding condition is detected, it starts generating a PLL-independent reference angle at the grid rated frequency. It starts from the last "non-islanded" reference angle acquired from the PLL. The output of the internal reference generator is multiplexed by the PLL output and a reference switch determines which one is to be fed to the rest of the system. This operation is depicted in Fig. 15.

When leaving the islanding mode because of a return of the grid to its operating condition, the reference switch waits until the difference between the internal generated reference angle and the PLL reference angle is lower than the selected threshold. Then, it switches to the PLL-generated reference. This action can be performed because the two reference generators work at different frequencies, the fixed and stable DSP generated internal frequency, and the rated, but slowly fluctuating, grid frequency. Even if the proposed control

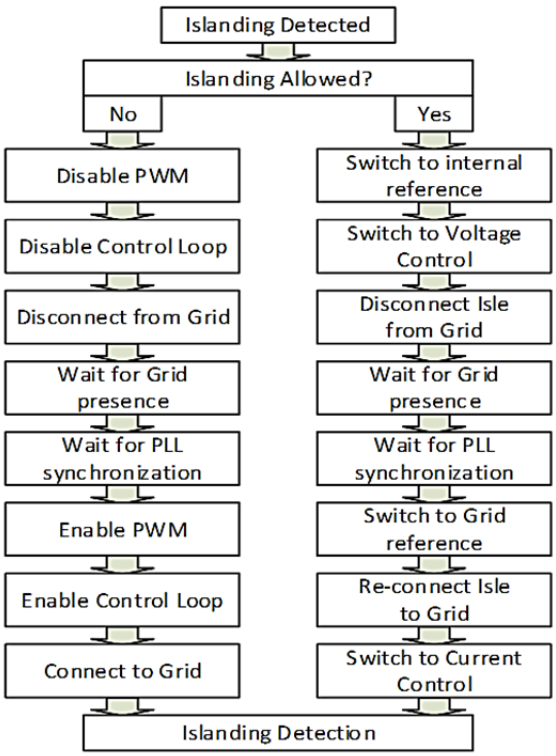


Fig. 16. Islanding detection operating rules.

architecture is able to easily switch between the grid-connected and islanding operations, the supervisor block has to take different actions depending on whether the islanding mode is forbidden (or not required) or allowed. In the first case, safety is preferred over quality of service. Therefore, the first action when islanding is detected is to stop the 1PH-VSI from generating any output by opening the PWM at the hardware level and disabling the control loop. A contactor-opening signal is also sent. However, its operation requires time before it can physically take place due to the electromechanical nature of the contactor. When the 1PH-VSI is disconnected, it starts to monitor the grid parameters to detect the presence of the grid, so that it can be ready to reconnect when grid comes up again.

If islanding operation is allowed, the quality of service becomes the focus. This means that efforts are directed towards the continuation of service for local loads, while still granting standard levels of safety. For these reasons, when islanding is detected, the reference angle is switched to the internal source and the control loop is commutated to the voltage control, as previously described in this paper. The island is then disconnected from the grid using a second contactor, as in B2 of Fig. 1. During the islanding operation, the 1PH-VSI keeps supplying local loads, based on the distributed generating unit capability, until the grid comes up again.

In this mode of operation, the active and reactive power depend on the load characteristics. The 1PH-VSI acts as an ideal voltage generator. If the required active power is higher

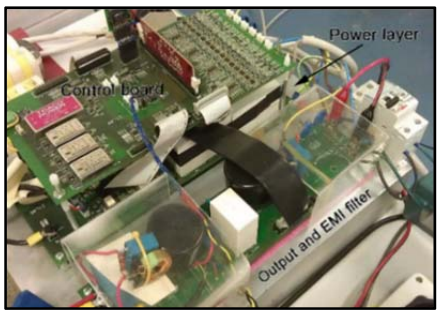


Fig. 17. Single-phase transformer-less 3-level NPC FB prototype.

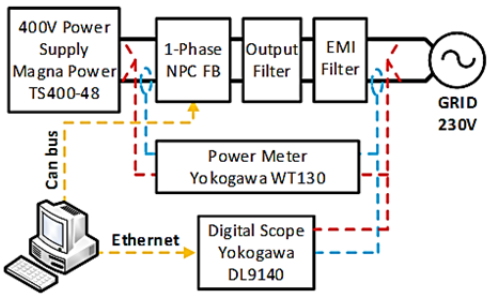


Fig. 18. Laboratory experimental set-up.

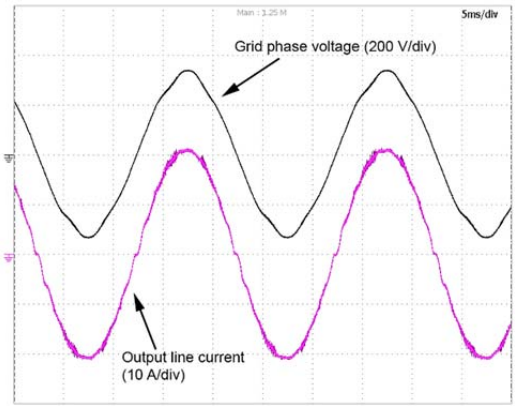
than the distributed generation actual produced power, the microgrid integrated manager has to run either the load shedding or VSI shutdown functions. When the grid returns to active, the reference angle is switched to the PLL source, the island is reconnected to the grid, and the control loop is switched to the current mode. In Fig. 16, the two proposed operating rules are illustrated. The proposed system architecture is suitable for use in the multiple inverter islanding scenario, provided that the microgrid integrated manager is running in the master-slave mode of operation.

VII. Experimental Results

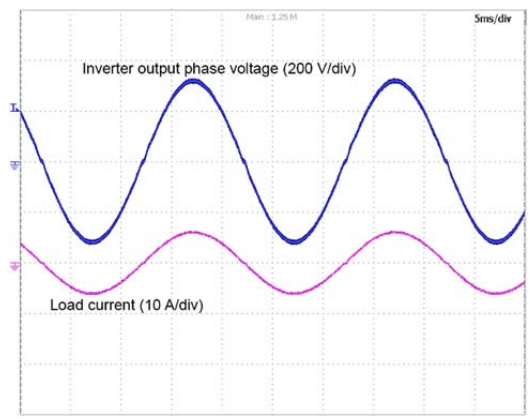
A prototype of the 1PH transformer-less 3-level NPC FB configuration has been built and tested, as depicted in Fig. 17, where the main parts of the inverter are highlighted. The laboratory set-up has been arranged for experimental purposes, as schematically illustrated in Fig. 18.

A Magna Power TS400-48 power supply is used as a 400Vdc power source, while a Yokogawa WT130 power meter is used to perform the efficiency and THD measures. The experimental results show a 98% efficiency at full power while the measured current THD is 1.75%. Fig. 19a depicts the laboratory utility grid voltage and the proposed VSI output current during operation at the rated power.

The inverter is also operated under different operating conditions. It is operated at 100% and 20% of the rated power and shows, even for a utility grid phase voltage with a 4.5% THD as shown in Fig. 19(a), current THDs of 1.75% and 2.91%, respectively. Fig. 19(b) depicts the output voltage and load current during the islanding operation. This test



(a)



(b)

Fig. 19. Experimental results at rated power, prototype output line current (10A/div) and phase voltage (200V/div). (a) Grid connected operation. (b) Intentional islanding operation.

highlights the almost ideal voltage generator behavior of the proposed 1PH-VSI, when it is operated in the intentional islanding mode. A harmonic analysis of the proposed VSI output current, up to the 40th harmonic order (as prescribed by EN50438), is performed by means of the WT130 power meter and compared with respect to the EN50438 Class A limits.

The results of Fig. 20 show that the proposed inverter and control strategy completely comply with the standards requirements. Testing of the active islanding detection algorithm has been accomplished by running the 1PH-VSI prototype in the islanding condition, while a fictitious grid angle is generated and all of the other protections are disabled. A 1 kW load is connected to the VSI output while operating the inverter in the current mode, and a reference current of about 4.1 A_{rms} is forced. This makes it possible for the inverter to provide a standard voltage of 230 V_{rms} at its output. Through the CAN bus interface, a command is sent to start the injection of the test frequency and one DSP flag is used to show when the injected tone is detected.

Fig. 21 shows the experimental results achieved during an evaluation of the islanding detection time using the proposed

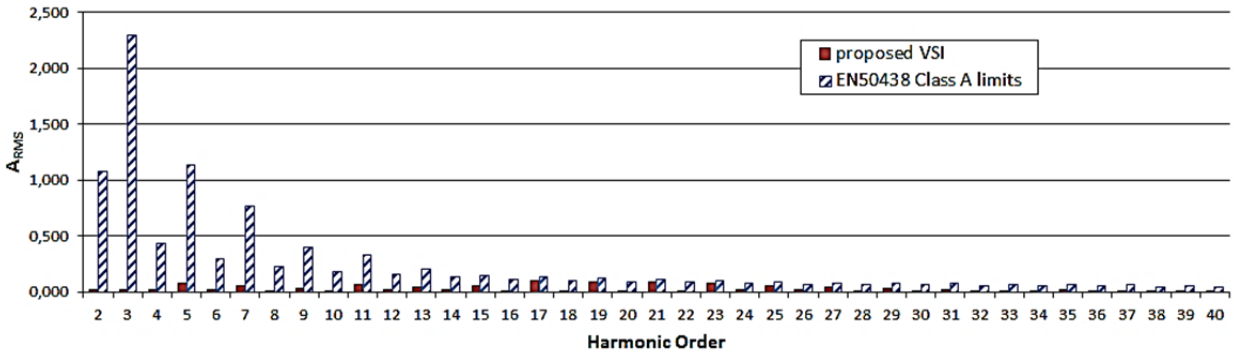


Fig. 20. Harmonic Analysis up to 40th harmonic order of VSI output current at rated power.

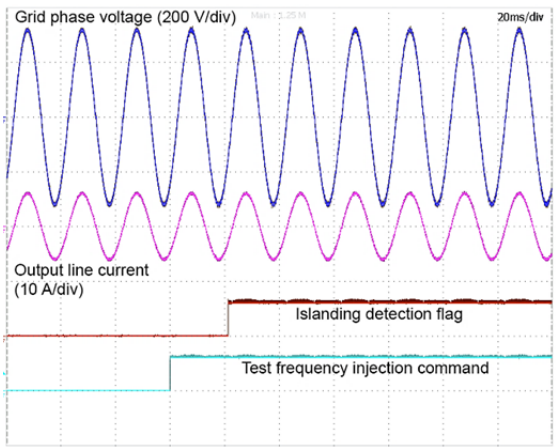


Fig. 21. Detection of islanding condition with active method.

Fig. 23. PLL - to-grid synchronization.

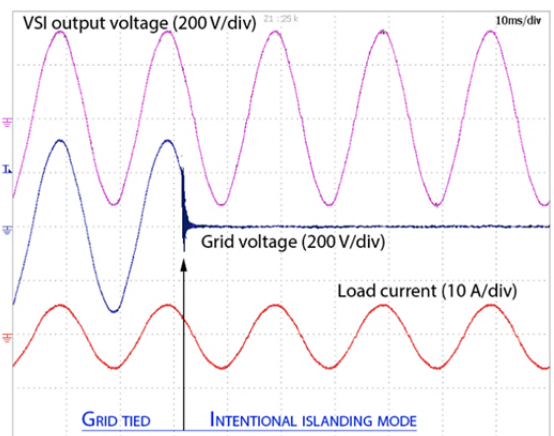


Fig. 22. Transition between Grid-tied and Intentional islanding operation.

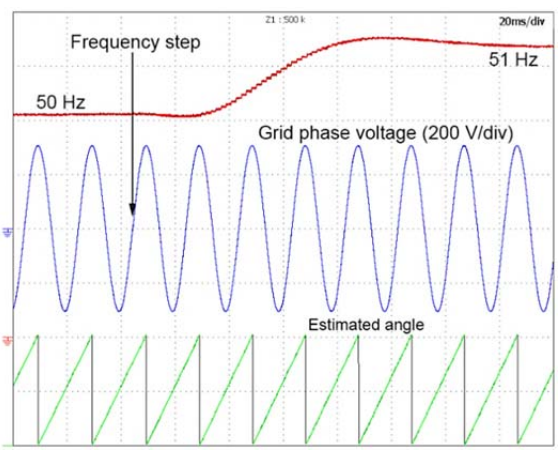


Fig. 24. PLL response to grid frequency step change.

active method. In this picture, from the top, the first and second traces are the VSI output voltage and current, while the third and the fourth traces are the sent injection command and the detected islanding flag, respectively. It can be noticed that while using the proposed technique, islanding operation can be detected roughly within one fundamental period (~20ms). The intentional islanding mode of operation has also been tested.

In this case, the 1PH-VSI prototype automatically switches from the current to voltage mode supplying the local island with a 1 kW load. Fig. 22 shows the results at transition between the grid-tied and islanding operating modes. The proposed PLL implementation is tested through the connection of the 1PH-VSI to a 50 Hz on intentionally achieved local grid. Fig. 23 shows the transition from the no-grid to grid operation.

The PLL requires less than a fundamental period to synchronize with the grid. The PLL estimated angle is plotted by means of the control board DAC output. Fig. 24 shows the PLL dynamics under a grid frequency step from 50 Hz to 51 Hz. The PLL estimated angle properly tracks this step

without a loss of synchronism. The top trace of Fig. 24 is the filtered output frequency which is used for the resonant controller online tuning.

The slow dynamic related to this estimation does not influence the functional operation of the inverter in the presence of a step-change in the grid nominal frequency. This is due to the fact that this value is not used in the PLL feedback loop. However, a temporary degradation of the current-THD, due to a mismatch between the resonant controllers tuning frequency and the actual grid frequency, is expected.

It should be noticed that the grid frequency, during normal grid operation, fluctuates around its rated value with low frequency oscillations. This means that the proposed filter approach is suitable for tracking typical grid frequency variations, which assures proper resonant controller tuning.

VIII. CONCLUSION

In this paper a single-phase three-level transformer-less inverter for residential distributed generation is proposed. The hardware configuration is described in detail. The control algorithm architecture is able to operate in both the grid-tied and islanding modes, in accordance with recent international standards. The proposed PLL feedback loop modifications allow for accurate estimation of the grid frequency and assure the proper online direct tuning of the proposed tuned resonant controllers. This is accomplished without the need for any additional hardware. The complete islanding detection procedure, based on active and passive detection algorithms, has been described and experimentally validated. Further, transitions from the grid-tied to intentional islanding operations, and vice versa, have been investigated. Experimental results are given to validate the functioning of the proposed inverter control architecture and the achieved performances.

REFERENCES

[1] P. Fairley, "The greening of GE [alternative energy]," *IEEE Spectrum*, Vol. 42, No. 7, pp. 28-33, Jul. 2005.

[2] R. C. Dugan, T. S. Key, and G. J. Ball, "Distributed resources standards," *IEEE Ind. Appl. Mag.*, Vol. 12, No. 1, pp. 27-34, Jan./Feb. 2006.

[3] P. Mattavelli, "Synchronous-frame harmonic control for high-performance AC power supplies," *IEEE Trans. Ind. Appl.*, Vol. 37, No. 3, pp. 864-872, May/Jun. 2012.

[4] A. Lidozzi, G. L. Calzo, L. Solero, and F. Crescimbini, "Integral-resonant control for stand-alone voltage source inverters," *IET Power Electronics*, Vol. 7, No. 2, pp. 271-278, Feb. 2014.

[5] G. L. Calzo, A. Lidozzi, L. Solero, and F. Crescimbini, "LC filter design for on-grid and off-grid distributed generating units," *IEEE Trans. Ind. Appl.,* Vol. 51, No. 2, pp. 1639-1650, Mar./Apr. 2015.

[6] C.-X. Dou, B. Liu, and D. J. Hill, "Hybrid control for high-penetration distribution grid based on operational mode conversion," *IET Generation, Transmission & Distribution*, Vol. 7, No. 7, pp. 700-708, Jul. 2013.

[7] R. Guillaume, T.-U. Tuan, and H. Nouredine, "Fuzzy logic supervision and control of distributed generators," in *18th International Conference and Exhibition on Electricity Distribution*, pp. 1-5, Jun. 2005.

[8] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.

[9] L. D'Errico, A. Lidozzi, and L. Solero, "Neutral point clamped converter for high fundamental frequency applications," *IET Power Electronics*, Vol. 4, No. 3, pp. 296-308, Mar. 2011.

[10] K. Jalili and S. Bernet, "Design of LCL filters of active-front-end two-level voltage-source converters," *IEEE Trans. Ind. Electron.,* Vol. 56, No. 5, pp. 1674-1689, May 2009.

[11] W. Wu, Y. He, and F. Blaabjerg, "An LLCL power filter for single-phase grid-tied inverter," *IEEE Trans. Power Electron.*, Vol. 27, No. 2, pp. 782-789, Feb. 2012.

[12] R. P. Stratford, "Rectifier harmonics in power systems," *IEEE Trans. Ind. Appl.*, Vol. IA-16, No. 2, pp. 271-276, Mar. 1980.

[13] J. M. Bloemink and T.C. Green, "Reducing passive filter sizes with tuned traps for distribution level power electronics," in *Proc. European Conference on Power Electronics and Applications(EPE 2011)*, pp. 1-9, Aug./Sep. 2011.

[14] Y. Patel, D. Pixler, and A. Nasiri, "Analysis and design of TRAP and LCL filters for active switching converters," in *IEEE International Symposium on Industrial Electronics(ISIE)*, pp. 638-643, Jul. 2010.

[15] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, Vol. 24, No. 3, pp. 654-664, Mar. 2009.

[16] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," in *IEE Proc. Electric Power Applications*, Vol. 153, No. 5, pp. 750-762, Sep. 2006.

[17] D. N. Zmood and D.G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, Vol. 18, No. 3, pp. 814-822, May 2003.

[18] S. Guo and D. Liu, "Rotating transformation and resonant control based feedback control strategy for dynamic voltage restorer system," in *2nd IEEE International Symposium on Power Electronics for Distributed Generation Systems(PEDG)*, pp. 333-338, Jun. 2010.

[19] A. Vidal, F. D. Freijedo, A. G. Yepes, P. F. Comesana, J. Malvar, O. Lopez, and J. D. Gandoy, "Assessment and optimization of the transient response of proportional-resonant current controllers for distributed power generation system," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 4, pp. 1367-1383, Apr. 2013.

[20] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Power Electronics Specialists Conference(PESC)*, pp. 1- 6, Jun. 2006.

[21] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*,

Vol. 60, No. 6, pp. 2167-2177, Jun. 2013.
[22] F. J. Rodriguez, E. Bueno, M. Aredes, L. G. B. Rolim, F. A. S. Neves, and M. C. Cavalcanti, "Discrete-time implementation of second order generalized integrators for grid converters," in *34th Annual Conference of IEEE Industrial Electronics(IECON)*, pp. 176-181, Nov. 2008.
[23] A. Nagliero, R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Monitoring and synchronization techniques for single-phase PV systems," in *International Symposium on Power Electronics Electrical Drives Automation and Motion(SPEEDAM)*, pp. 1404-1409, Jun. 2010.
[24] S. Bifaretti, A. Lidozzi, L. Solero, and F. Crescimbini, "Anti-islanding detector based on a robust PLL," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 1, pp. 398-405, Jan./Feb. 2015.
[25] R. S. Kunte and W. Gao, "Comparison and review of islanding detection techniques for distributed energy resources," in *40th North American Power Symposium*, pp. 1-8, Sep. 2008.
[26] T. Funabashi, K. Koyanagi, and R. Yokoyama, "A review of islanding detection methods for distributed resources," *in IEEE Power Tech Conference Proceedings*, Vol. 2, pp. 23-26 Jun. 2003.
[27] E. J. Estébanez, V. M. Moreno, A. Pigazo, M. Liserre, and A. Dell'Aquila, "Performance evaluation of active islanding-detection algorithms in distributed-generation photovoltaic systems: Two Inverters Case," *IEEE Trans. Ind. Electron*., Vol. 58, No. 4, pp. 1185-1193, Apr. 2011.
[28] M. Liserre, A. Pigazo, A. Dell'Aquila, and V. M. Moreno, "An anti-islanding method for single-phase inverters based on a grid voltage sensorless control," *IEEE Trans. Ind. Electron*., Vol. 53, No. 5, pp. 1418-1426, Oct. 2006.
[29] M. Ciobotaru, V. G. Agelidis, R. Teodorescu, and F. Blaabjerg, "Accurate and less-disturbing active anti-islanding method based on PLL for grid-connected converters," *IEEE Trans. Power Electron.*, Vol. 25, No. 6, pp. 1576-1584, Jun. 2010.
[30] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 5, pp. 1398-1409, Oct. 2006.
[31] S.-K. Kim, J.-H. Jeon, J.-B. Ahn, B. Lee, and S.-H. Kwon, "Frequency-shift acceleration control for anti-islanding of a distributed-generation inverter," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 2, pp. 494-504, Feb. 2010.
[32] B. Yu, Y. Jung, J. So, H. Hwang, and G. Yu, "A robust anti-islanding method for grid-connected photovoltaic inverter," in *4th World Conference on Photovoltaic Energy Conversion*, Vol. 2, pp. 2242-2245, May 2006.
[33] I. J. Balaguer, Q. Lei, S. Yang, U. Supatti, and F. Z. Peng, "Control for grid-connected and intentional islanding operations of distributed power generation," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 1, pp. 147-157, Jan. 2011.

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