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A Single-Phase Cell-Based Asymmetrical Cascaded Multilevel Inverter

Varsha Singh[†], Swapnajit Pattnaik[*], Shubhrata Gupta[*], and Bokam Santosh[*]

[†,*]Department of Electrical Engineering, National Institute of Technology, Raipur, India

Abstract

A single-phase asymmetrical cascaded multilevel inverter is introduced with the goal of increasing power quality with the reduction of power in insulated-gate bipolar transistor (IGBT) switches. In the present work, the proposed inverter topology is analyzed and generalized with respect to different proposed algorithms for choosing different voltage source values. To prove the advantages of the proposed inverter, a case study involving a 17-level inverter is conducted. The simulation and experimental results with reduced THD are also presented and compared with the MATLAB/SIMULINK simulation results. Finally, the proposed topology is compared with different multilevel inverter topologies available in the literature in terms of the number of IGBT switches required with respect to the number of levels generated in the output of inverter topologies.

Key words: Multilevel inverter, Power losses, Total harmonic distortion (THD)

I. INTRODUCTION

The demand for electrical power continues to increase today. Consequently, the amount of resources needed to address this demand also increases. The proper utilization of power is necessary whenever surplus power is available. Such state can be achieved by storing surplus power through batteries in the form of DC. This stored energy can then be re-utilized by conversion devices known as inverters by converting DC power into AC power. Existing multilevel inverters (MLIs) are updated according to their high power capabilities. Hence, MLIs are capable of achieving good voltage spectrum and low voltage stress.

In an MLI, the output levels that occur in a proper way achieve the approximated sinusoidal wave. If these levels are large in number, then the staircase waveform is relatively close to the sinusoidal waveform. However, conventional MLIs require several clamping diodes or flying capacitors to achieve a large number of output levels. Hence, the number of levels achieved is limited to circuit complexity and equipment cost [1]. Certain clamping diodes are required for some topologies; hence, researchers are still focused on simplifying circuitry and avoiding clamping devices as much possible [2]. The advantages of MLIs include low switching losses, low voltage stress, and good electromagnetic interference [3], [4].

Conventional MLIs come in three types [5]: neutral point clamped multilevel inverters (NPCMLIs), flying capacitor multilevel inverter (FCMLIs), and cascaded H-bridge multilevel inverter (CHBMLIs). NPC MLIs represent the first generation of MLI topologies according to [6]. In the FCMLI topology, numerous bulk capacitors are required to block the voltage and achieve clamping. CHB MLIs are formed from single-phase H-bridge (H-B) inverters connected in series with individual DC voltage sources. Each H-B produces three levels, namely, positive, negative, and zero, and the total voltage in the output is the sum of all individual H-B voltages [7]. The conventional MLIs all require numerous switches, insulated-gate bipolar transistor (IGBT) drivers, and separate DC voltage sources. Thus, different innovative MLI topologies are introduced to address the drawbacks of existing ones. Switching losses, control algorithms, numbers of levels, total harmonic distortions (THDs) in the output voltage waveform, stresses across switches, and the dynamics of voltage across switches are issues optimized with recent topologies. In the literature, many topological approaches were developed to deal with issues and applications, such as the introduction of low switching frequency and high power switches in MLIs [6], [9]. Moreover, MLIs are widely used in industrial applications,

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[†]Corresponding Author: vsingh.ele@nitrr.ac.in
Tel: +94-2-552-4731,Fax: +91-771-2254600, N. I. T. Raipur
[*]Department of Electrical Engineering, National Institute of Technology, India

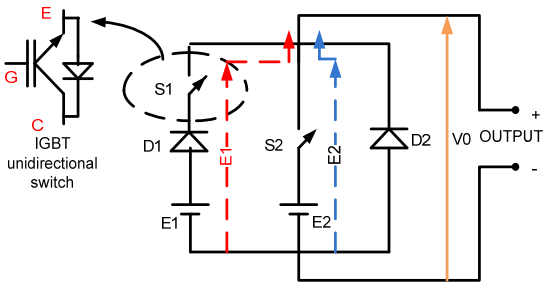

Fig. 1. Basic proposed cell.

TABLE I
SWITCHING SEQUENCE OF A CELL

State	S1	S2	Output Voltage (V0)
1	ON	OFF	E1
2	OFF	ON	E2

including flexible AC transmission of electrical power systems (FACTS) [8], electric vehicle [9] applications, as well as non-conventional sources, such as the recent technology of photovoltaic systems. Generally, inverters represent cascade connections of different basic modules, in which switches, diode combination, and DC voltage sources are necessary

II. PROPOSED TOPOLOGY

In this section, the proposed topology is introduced to overcome the disadvantages of the conventional and existing topologies cited in the literature. The proposed topology consists of a basic cell, which is shown in Fig.1. This cell consists of two unidirectional IGBT switches, two diodes, and two DC sources E1 and E2 (E2 > E1). The proposed basic cell can produce two output voltage levels across the connected load. When switch S1 is turned ON, the output voltage across the load is E1 volts. When switch S2 is triggered by the gate signal, the output voltage V_0 across the load is E2 Volts by keeping the other switch in OFF mode. This switching sequence is given in Table I.

The following waveform represents the basic cell output waveform in the output side (Fig. 2).

A. Proposed Topology for Five-Level Output

The proposed topology is developed by using the basic H-B for generating a five-level AC stepped voltage waveform across the load. In the circuit, the switches and voltage sources require two voltage sources E1, E2=2E1; two unidirectional switches S1 and S2; an H-B comprising four unidirectional switches T1,T2,T3, and T4; and two diodes D1 and D2. In the present work, the unidirectional switch is replaced with an IGBT with an anti-parallel diode, which is mainly used for medium power applications. For the production of a five-level output for the proposed topology, a proper switching sequence is required, as shown in Table II. Specifically, this table shows

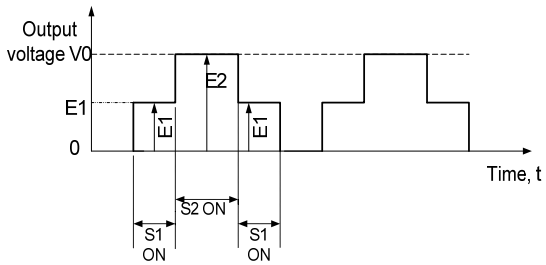

Fig. 2. Output Voltage (V_0) waveform for Cell 1.

TABLE II
SWITCHING SEQUENCE FOR BASIC FIVE-LEVEL OUTPUT

V0	Step	S1	S2	D1	D2	T1	T2	T3	T4
0	1	0	0	0	0	1	1	0	0
						0	0	1	1
E1	2	1	0	1	0	1	0	0	1
2E1	3	0	1	0	0				
−E1	4	1	0	1	0	0	1	1	0
−2E1	5	0	1	0	0				

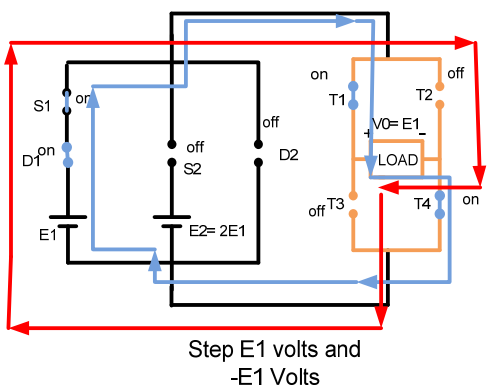

Fig. 3. Current flowing path for different modes of levels, with the blue line representing level "E1" and the red line representing level "–E1."

the switching sequence for five different states with output voltage values 0, E1, 2E1, −E1, and −2E1, with "1"representing the ON state and "0" representing the OFF state.

Fig. 3 shows the switching states for different levels, which can be produced from the proposed five-level topology. The current flowing path for different levels, which are generated across the output, is based on the switching sequence from Table II.

III. PROPOSED PARAMETER-GENERALIZED TOPOLOGY

Fig. 4 shows the cascaded connection of basic cell topologies for producing a definite number of output levels. In this extended proposed topology, "n", which denotes the number of basic cells, is connected in series to produce a multilevel output. This output is the sum of individual cell

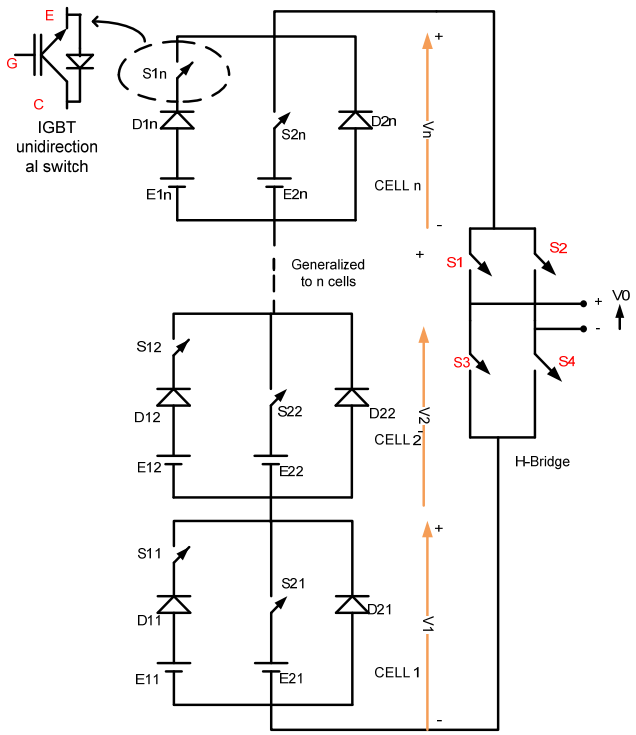

Fig. 4. Generalized format of proposed topology.

output voltages.

In expression form,

$$V_0 = \text{sum } (V1, V2, V3 \ldots Vn)$$

$$\text{i. e., } v_0 = \sum_{i=1,2\ldots n} Vi \,. \quad (1)$$

In the abovementioned equation, V1, V2…Vn refer to the individual voltages across cell1, cell2… cell n. With the proper ON and OFF switching of the switches, the required output can be obtained.

As mentioned in the preceding paragraphs, the asymmetrical voltage sources can differ in value but produce a different number of levels. In fact, such feature improves inverter performance. Here, the asymmetrical value of voltage sources is obtained by changing the transformer turns ratio for various source values. In this case, the selection of the values of DC voltage sources is an important factor. A considerable number of choices are available for selecting the source values. Four different algorithms are presented to choose the voltage values for the proposed generalized topology. For all the algorithms the components used, the number of DC sources and the topology configurations are the same.

Number of IGBT switches, N switches = $2n + 4$

Number of voltage sources, N sources = $2n$

Number of diodes, N diodes = $2n$

A. Algorithm 1: M(I)

In this algorithm, "n" basic cells are connected in a cascaded format. The first algorithm features a symmetrical cell configuration as described below. A symmetrical cell configuration means that an "n" number of cells have the same number of voltage values, i.e. Vdc, 2Vdc…, the same number of switch count, and the same characteristics of individual cell structure.

Number of voltage levels, N step = $4n + 1$

Variety of voltage sources, N asymmetry = $2n$

B. Algorithm 2: M(II)

In this algorithm, the voltage source values follow a powered format. The following equations represent the format of the voltage sources and its usefulness in increasing the levels in the output voltage waveform.

Number of voltage levels, N step = $4.2^n - 3$

Variety of voltage sources, N asymmetry = $2n$

C. Algorithm 3: M(III)

If asymmetry increases, then the complexity and cost of the inverter also increase. However, the steps in the output waveform increase for the same number of switches used in the second method. In this method, the voltage source values are not equal. Hence, this topology is suitable for PV cell arrays.

Number of voltage levels, N levels = $2.3^n - 1$

Variety of voltage sources, N asymmetry = $2n$

D. Algorithm 4: M(IV)

The voltage values are calculated by the new voltage combination analysis, which is called the "even and odd voltage" analysis.

Number of voltage levels, N levels= $2.n^2 + 2n + 1$

Variety of voltage sources, N asymmetry = $2n$

where "n" is the basic number of cells.

Table III presents the comparison between the derived algorithms of the proposed topology. Specifically, this table shows the values of sources, variety, switches, and levels generated in terms of the "n" number of cascaded cells.

We can conclude that Algorithm M (III) gives the maximum number of levels for the same number of switches.

IV. Comparison of Proposed Topology with Conventional Topologies

The comparison of the proposed topology with conventional topologies in the literature is necessary to identify the advantages and disadvantages of the proposed topology. This comparison is made by using the parameters such as N sources, N switches, N diodes, and N levels between proposed topology and conventional topologies.

A. Comparison of the Required Number of IGBTs with Respect to the Number of Levels

The topologies in [11], [12], and [14] generate specific

TABLE III
DIFFERENT PARAMETERS OF THE PROPOSED CASCADED MULTILEVEL INVERTER

Parameters to be compared	Asymmetrical configuration algorithms			
	Algorithm M(I)	Algorithm M(II)	Algorithm M(III)	Algorithm M(IV)
Voltage magnitude	E1n= $n.Vdc$ E2n= $2n.V_{dc}$	E1n= $n.Vdc$ E2n= $2^n.Vdc$	E1n= $3^{n-1}.V_{dc}$ E2n= $2.3^{n-1}.V_{dc}$	E1n= $(2n-1)V_{dc}$ E2n= $2n.V_{dc}$
Nlevels	$4n+1$	4.2^n-3	2.3^n-1	$2.n^2+2n+1$
Nswitches	$2n+4$	$2n+4$	$2n+4$	$2n+4$
Nvariety	2	$2n$	$2n$	$2n$
Ndiodes	$2n$	$2n$	$2n$	$2n$
Nsources	$2n$	$2n$	$2n$	$2n$

where “n” is the basic number of cells.

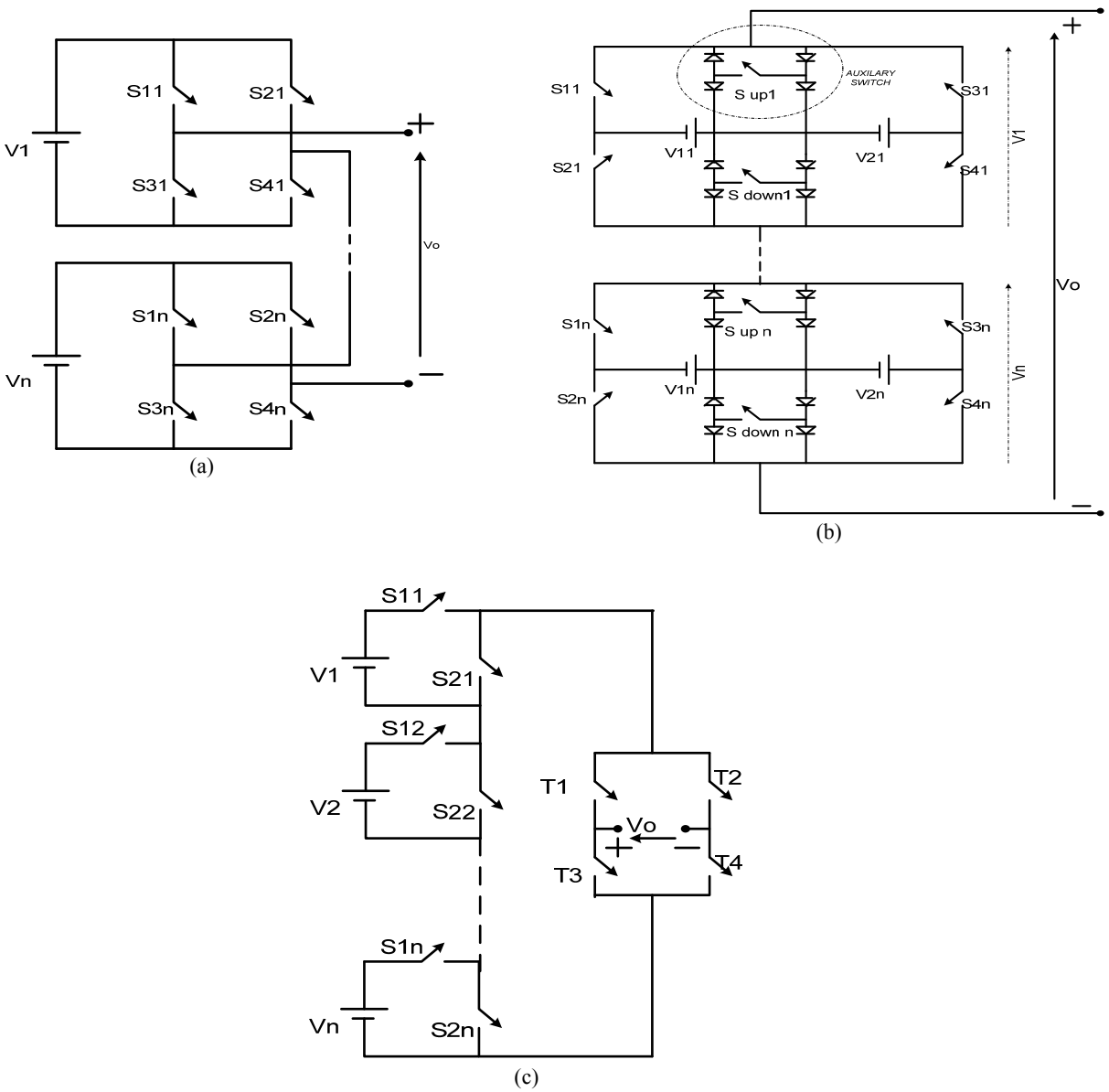

Fig. 5. Cascaded multilevel inverters. (a) Conventional cascaded multilevel inverter V1= Vdc,V2=V3=….Vn= 2vdc[11]. (b) Presented Topology in[12]with binary progression. (c) Presented Topology in [14] with binary V1=Vdc,V2=2vdc,V3=4vdc, … .

TABLE IV
COMPARISON OF PROPOSED TOPOLOGY WITH EXISTING TOPOLOGIES

Topology	Levels (L)	Switches (IGBT)	DC sources	Diodes
Proposed M(I)	$4n+1$	$2n+4$	$2n$	$2n$
Proposed M(II)	4.2^n-3	$2n+4$	$2n$	$2n$
Proposed M(III)	2.3^n-1	$2n+4$	$2n$	$2n$
Proposed M(IV)	$2.n^2+2n+1$	$2n+4$	$2n$	$2n$
Topology T(a)	$4n-1$	$4n$	n	----
Topology T(b)	$2^{2n+1}-1$	$6n$	$2n$	$8n$
Topology T(c)	$4n-1$	$2n+4$	n	----

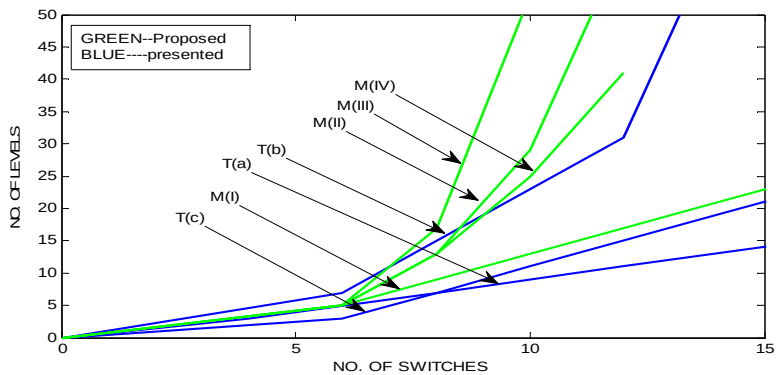

Fig. 6. Comparison graph for Number of switches Vs. Number of levels.

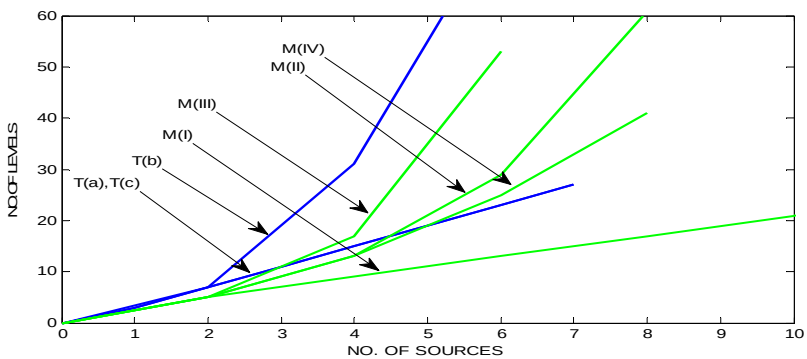

Fig. 7. Comparison graph for voltage sources and levels.

numbers of levels by using the required numbers of IGBTs and more number of diodes. However, the required number of IGBTs varies for each topology, as shown in TABLE IV and in the comparison graph of Fig. 6. In [12], unidirectional and bidirectional switches were combined for switching purposes; these bidirectional switches require four power diodes and an additional switch, thus increasing the power electronic components and reducing system modularity. Fig. 8 shows that all compared topologies suffer from an increase in the number of diodes. Power dissipation notably rises whenever current flows through the diodes. If more number of diodes are used, then the total power dissipation also increases, thereby decreasing the system efficiency. Thus, the proposed topology is able to reduce the required number of diodes and switches for a particular level.

The proposed topology with four algorithms is compared with existing topologies to show that the proposed one is useful (Fig. 6). According to the above comparison graphs, the output voltage is the highest for the asymmetrical type of inverter topologies. Fig. 6 shows that Algorithm M (III) (top green line in Fig. 6) gives a large number of levels with reduced switches and sources such that the performance of the inverter is improved.

B. Comparison of Number of Voltage Sources with respect to Number of Levels

In medium voltage applications, high voltage blocking capacity switches (T1, T2, T3, and T4) are required in H-B.

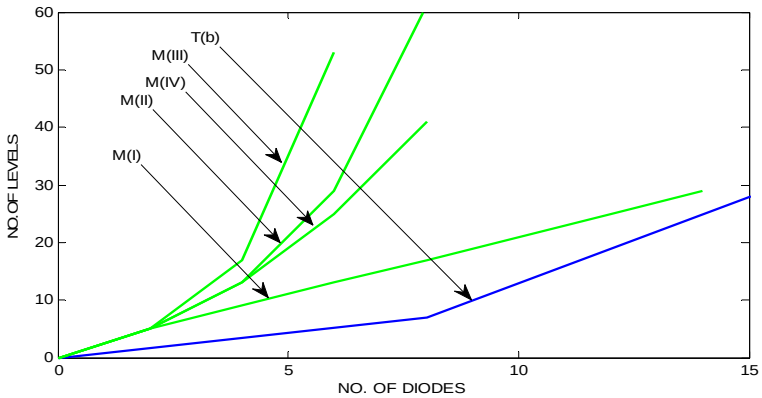

Fig. 8. Comparison between number of diodes required and number of levels.

This feature may significantly increase the blocking voltage for the proposed topology but reduce the number of switches required. In the literature, topologies of different configurations are available for different applications. The proposed topology is perfectly suitable for applications involving non-conventional voltage sources because it requires more voltage sources for the corresponding levels generated. Fig. 7 shows that the proposed topology requires more voltage sources in comparison with the remaining topologies, thus suitable for solar powered applications.

C. Overall Cost Comparison

The overall cost of the proposed topology is lower than that of the conventional topologies presented in literature. In the present paper, the formula for the overall cost of the proposed generalized topology is given below.

Overall Cost= $N_{IGBT}+N_{driver}+N_{sources}+N_{variety}+N_{diode}+MC$

where N_{IGBT}, N_{driver}, $N_{sources}$, $N_{variety}$, N_{diode}, and MC denote the cost of the IGBT switches used in the topology, the cost of the driver circuit for each IGBT, the cost of DC voltage sources, the cost of different voltage varieties as in the case of the asymmetrical type, the cost of the power diodes used, and other miscellaneous costs, respectively. The cost of the proposed MLI is lower than that of the topologies in [11], [12], and [14] but is higher than that of the cascaded H-B because of the cost polarity generator added to the proposed topology. Even though the proposed topology can be cascaded to significantly reduce the cost of the inverter and increase the number of voltage levels with a low number of power switches and diodes, it is the most suitable topology for high power applications.

V. Simulation and Experimental Results

To determine the performance of the proposed inverter, the case study of a 17-level inverter is also analyzed. The proposed 17-level MLI structure is simulated in MATLAB/SIMULINK. Although the literature cites many inverters that produce the same number of levels as the 17-level inverter, this case inverter produces the same number of levels but with few

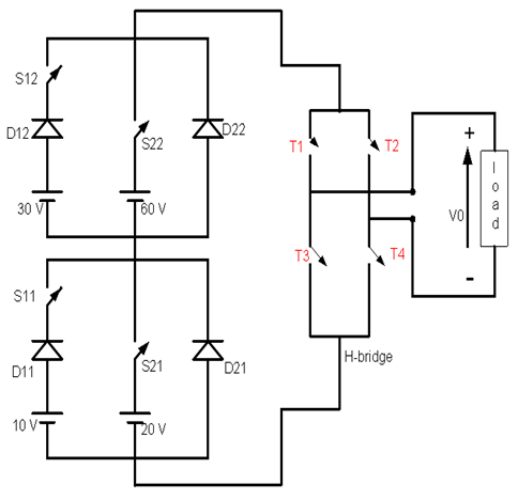

Fig. 9. 17-level inverter configuration with two basic cells.

switches and low %THD values in the output. Fig. 9 shows that the configuration of the 17-level inverter is based on the asymmetrical cell voltage method (third proposed voltage value calculation algorithm). The requirements for the generation of 17 levels in the output are as follows: voltage source values V11=1Vdc, V21=2Vdc (Cell 1), V12=3Vdc, V22=6Vdc (Cell 2); four unidirectional IGBT switches, namely, S11,S21,S12, and S22;an H-B consisting of four switches T1,T2,T3, and T4 to reverse the polarity of the voltage levels; and a load consisting of RL load with values of R=60 ohm, L= 5mH,as well as four diodes. The maximum voltage across the load is 8Vdc. The modulation method used to generate the switching instants is the APOD (alternate phase opposition disposition [10]. In this case study, the 1.2 kHz switching frequency is used.

Table V presents how the individual levels are produced by the switches employed in a sequence. The RL load can be used as a low pass filter so that the output waveform of the current is nearly equal to the smooth sinusoidal waveform.

As shown in Table VI, the %THD of the output voltage at 1,200 Hz is lower than that of the remaining frequency variation for the R-load and RL-loads. The %THD of the

TABLE V
SWITCHING SEQUENCE FOR 17-LEVEL INVERTER (THIRD ALGORITHM).

Level	S11	S21	S12	S22	D11	D21	D12	D22	T1	T2	T3	T4
8	0	1	0	1	0	0	0	0				
7	1	0	0	1	1	0	0	0				
6	0	0	0	1	0	1	0	0	1	0	0	1
.												
.												
1	1	0	0	0	1	0	0	1				
0	0	0	0	0	0	0	0	0	1 0	1 0	0 1	0 1
-1	1	0	0	0	1	0	0	1				
.												
.												
-6	0	0	0	1	0	1	0	0	0	1	1	0
-7	1	0	0	1	1	0	0	0				
-8	0	1	0	1	0	0	0	0				

TABLE VI
VARIATION OF 17-LEVEL INVERTER WITH FREQUENCY FOR R- AND RL-LOAD

Frequency(Hz)	%THD(V)	%THD(I)	%THD(V)
	R-LOAD	RL-LOAD	
200	6.54	5.124	6.541
400	5.948	4.515	5.949
600	7.077	5.524	7.078
1,000	6.466	4.765	6.469
1,200	**5.92**	**3.847**	**5.91**
1,500	6.482	4.575	6.496
1,800	6.966	4.448	6.989
2,000	7.042	4.223	7.074

voltage and current is 5.92% (Fig. 10) for R = 60 ohm at 1,200 Hz frequency. For the RL-load, the %THD of the current waveform at 1,200 Hz frequency is 3.847%.The following are the formulas for calculating %THD and %WTHD. %WTHD is another factor for measuring the weight of the individual harmonic content. 0.333% and 0.338% are the %WTHD values for the R-load and RL-load of the 17-level inverter, respectively.

$$\%THD = \sqrt{\frac{V_{rms}^{\ 2} - V_1^{\ 2}}{V_1^{\ 2}}} \times 100 \quad (2)$$

$$\%WTHD = \sqrt{\frac{V_2^{\ 2}/2^2 + V_3^{\ 2}/3^2 + ... V_n^{\ 2}/n^2}{V_1^{\ 2}}} \times 100 \quad (3)$$

Figs. 12 and 13 provide the waveforms of the blocking voltages and currents of each switch in the two available cells of the proposed topology, respectively. From these waveforms, the voltage stress of each element can be calculated. The experimental results verify the simulation results. Figs. 14 and 15 show the output voltage waveform and Fast Fourier Transform (FFT) results of the proposed 17-level MLI. Figs.16 and 17 are added to support the experimental validation for the output voltage and current.

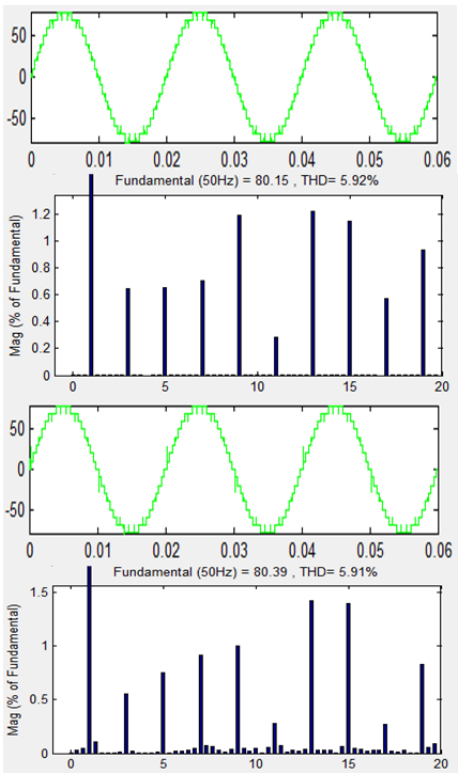

Fig. 10. Output voltage waveform and FFT analysis for R-Load and RL-load.

A. Power Loss Calculation for 17-Level Inverter by Using PSIM

The proposed MLI bridge network comprises eight IGBTs and four diodes. The power losses of the proposed MLI are calculated with the PSIM software. The power loss considered here is a combination of switching and conduction losses. Switching losses can be calculated by the operating switching frequency of IGBTs. Thus, switching losses are a combination of turn-ON and turn-OFF energies that are wasted in the ON and OFF of IGBTs.

Table VII presents the switching losses for each switch at a

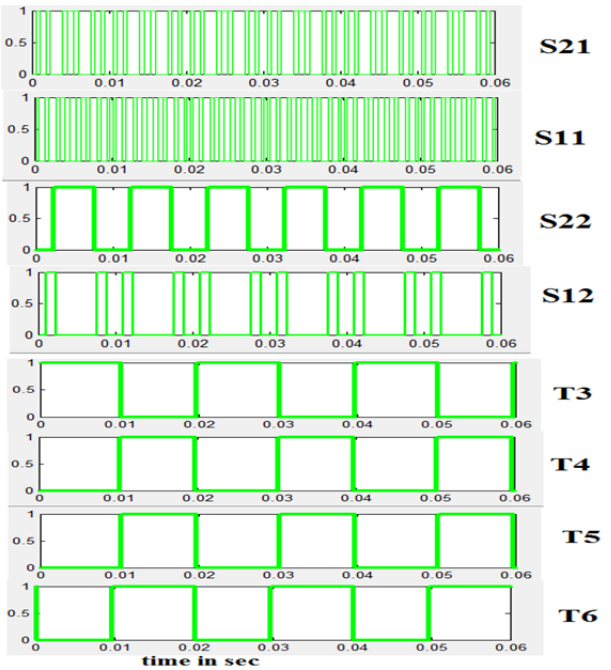

Fig. 11. Gate pulses to the IGBT switches for proposed topology.

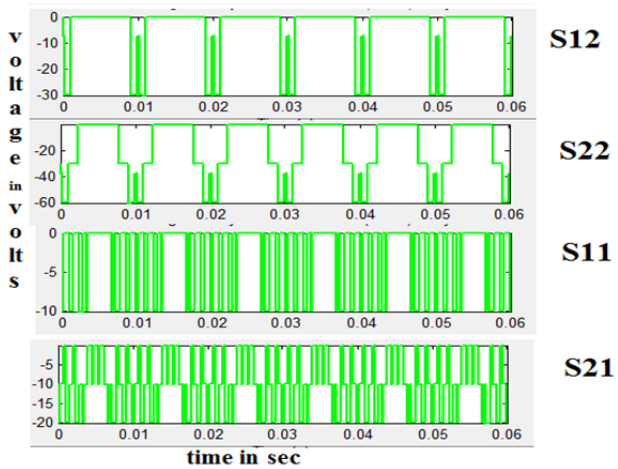

Fig. 12. Voltage across each switch in two available cells.

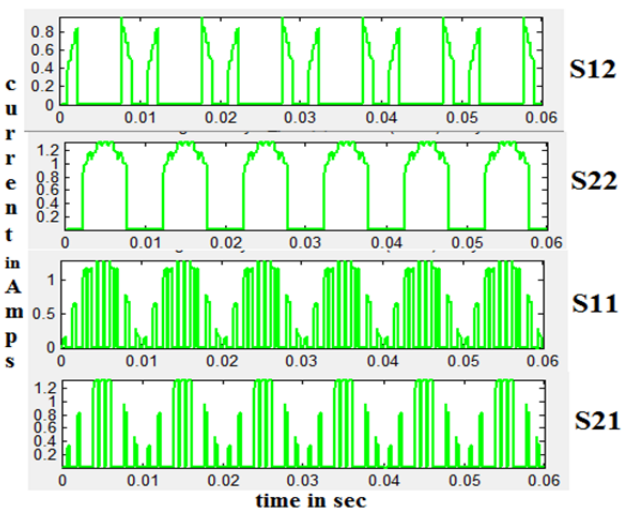

Fig.13. Current passing through the switches inside two cells.

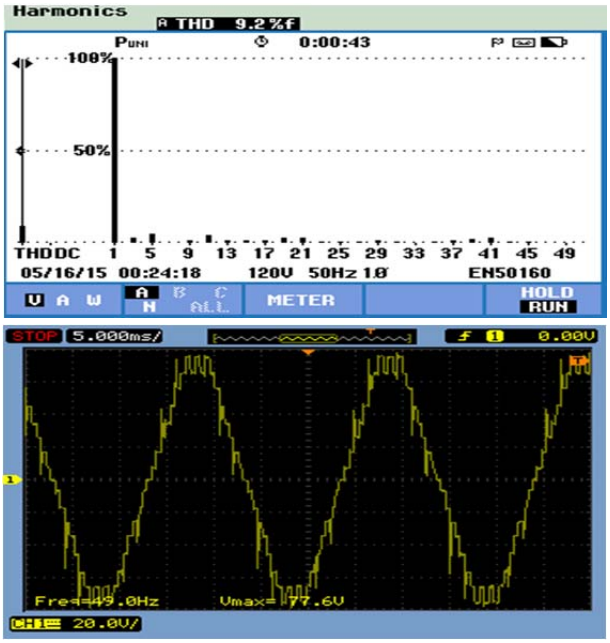

Fig. 14. Experimental output voltage waveform and FFT analysis for 17-level inverter for R-Load.

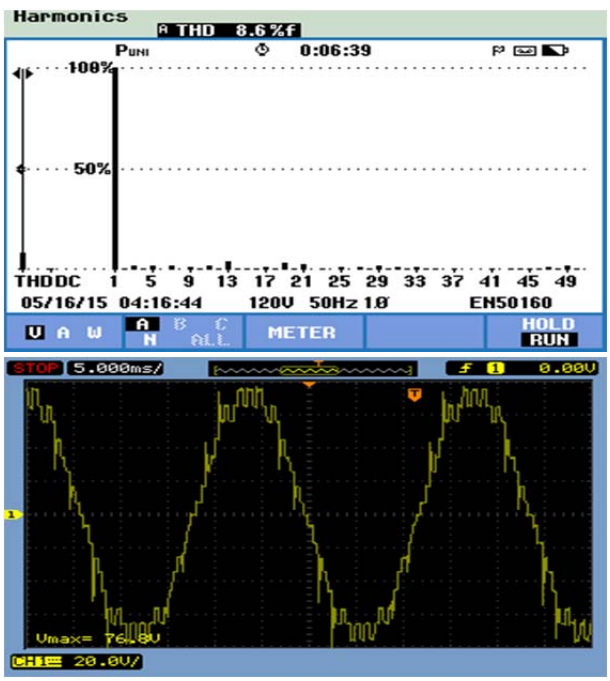

Fig. 15. Experimental output voltage waveform and FFT analysis for RL-load.

Fig. 16. Experimental output voltage waveform for 100 W load.

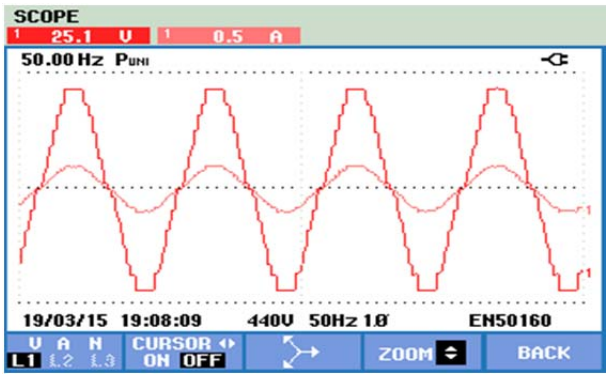

Fig.17. Experimental output voltage and output current waveforms for 17-levelinverter.

TABLE VII
17-LEVEL INVERTER SWITCHING LOSSES FOR R-AND RL LOAD

S.No	Switch No.	Max. Voltage (V)	Max. Current (A) R-LOAD	Power Loss (W)	Max. Current (A) RL-LOAD	Power Loss (W)
1	IGBT S22	90	1.7	0.4	2	0.50
2	IGBT S12	60	1.9	0.2	1.66	0.25
3	IGBT T1,T2	90	1.3	$5.8e^{-3}$	1.5	$0.4e^{-3}$
4	IGBT T4,T3	90	1.3	$1.8e^{-2}$	1.5	$3.0e^{-2}$
5	IGBT S11	20	2.5	0.6	2.3	0.7
6	IGBT S21	40	2.5	1.2	2.6	1.2
7	DIODE D11	10	2.5	0.7	2.3	0.7
8	DIODE D12	30	1.9	0.4	1.6	0.4
9	DIODE D21	20	2.2	1.0	2	1.0
10	DIODE D22	30	0.9	0.23	0.6	0.2

1.2 kHz frequency for the R- and RL-load. As shown in the TABLE VII total switching losses for the17-level inverter topology with R-load and RL-load are approximately 5.0118W and 4.7786 W, respectively.

B. Efficiency Calculation for 17-Level Inverter

For any inverter, the efficiency calculation is necessary because it is the performance factor when different fractions of loads are considered [17]. The following is the formula for the efficiency calculation when the output and input power are known.

$$\% \ \eta \ = \left(\frac{P_{out}}{P_{in}} \right) \times 100 \tag{4}$$

According to the efficiency curve analysis, the efficiency of the17-level inverter at R = 90 ohm and L = 50 mH is 98.24%. Hence, the proposed inverter circuit with several levels operates satisfactorily under good efficiency conditions (Fig. 18).

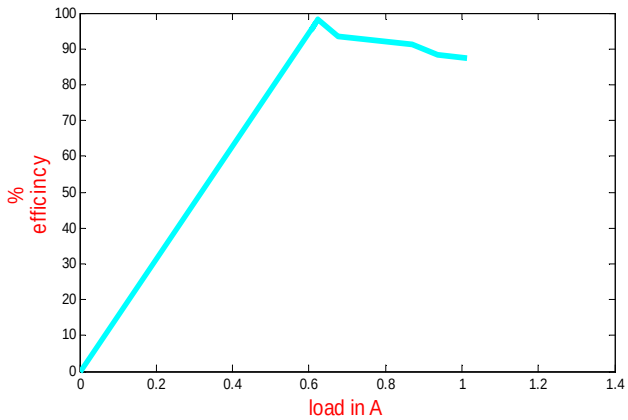

Fig. 18. Efficiency curve for 17-level inverter.

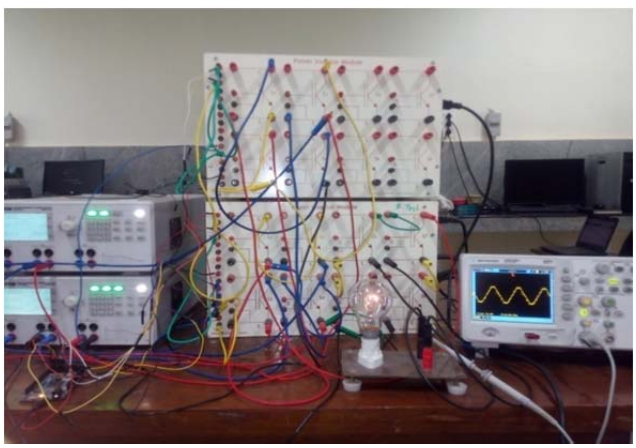

Fig.19. Experimental prototype model.

VI. CONCLUSION

An asymmetrical MLI with 17 levels is proposed and analyzed. According to the aforementioned analysis, the proposed topology is more advantageous than conventional topologies because of its low number of switches, diodes, and sources to achieve the required number of levels generated. When the number of switches is reduced, switching losses could also be reduced. Hence, the proposed topology is suitable for different applications in ac drives. A 17-level MLI for R-load and RL-load is studied and is found to yield good results in terms of %THDs, which are5.91% for the RL-load and 5.92%for the R-load in the simulation case and 8.6% for the RL-load and 9.2% for the R-load in the experimental case.The efficiency of the 17-level inverter is good at 98.24%. Hence, as validated via the experiment, the proposed inverter is able to produce more levels with a reduced number of switches and %THD which is validated by experiment.

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Varsha Singh was born in Madhya Pradesh, India. Sheis an Assistant Professor in the Department of Electrical Engineering, National Institute of Technology, Raipur. She received her B.E. degree in Electrical Engineering from the Government Engineering College, Bilaspur, and her M.Tech degree in Electrical Engineering from the Government Engineering College Raipur, India, in 1991 and 2002, respectively. Her teaching experience spans over 15 years. She is currently working toward her Ph.D. degree in Electrical Engineering in N.I.T. Raipur. She has published more than 15 papers in international conferences and international journals. Her current research interests include PWM inverter systems and their applications and the usage of soft computing techniques in the field of power electronics.

Swapnajit Pattnaik was born in Odisha, India. He received his B.E. degree in Electrical Engineeringfrom Utkal University, in 1998, and his M.Tech. and Ph.D. degrees in Electrical Engineeringfrom the National Institute of Technology, Rourkela, India, in 2003 and 2011, respectively. He was with CSIT, Durg as Faculty from 2003 to 2006 and as a Research Scholar from 2006 to 2008.From 2008 to 2009, he was with ITER, Bhubaneswar as Faculty. In 2009, he became an Assistant Professor in the Electrical Engineering Department ofthe National Institute of Technology, Raipur. His current research interests include AC electric vehicles, DC-DC converters, and PWM converter/inverter systems.

Shubhrata Gupta was born in March 1966. She is a Professor in the Department of Electrical Engineering, National Institute of Technology, Raipur. She completed her B.E. degree in Electrical Engineering in 1988, her master's degree in Integrated Power System in 1998, and her Ph.D. degree in Power Quality in 2009. She has over 25 years of teaching experience. Her research interests include power electronics, electric machines, and power quality. She has published articles/papers in various referred national and international conferences and journals. She is currently serving as a reviewer for several journals. One of her papers has beenselected as a recipient of the Best Paper Award/Certificate (International Journal of Electrical and Electronics Engineering Research (IJEEER) Tran stellar Journal Publications, Impact Factor - 5.6397). She was awarded the "Shiksha Ratan Puraskar" by the International Friendship Societyand nominated for the "Indira Gandhi Shiromani Award," "Rajiv Gandhi Excellence Award,"and the "Bharat Gaurav Award" by the Inter. Friendship Society. She also earned the Outstanding Engineering Teacher award by IE (I)-2014.

Bokam Santosh was born in Visakhapatnam, Andhra Pradesh, India, in 1991. He received his B.Tech. degree in Electrical and Electronics Engineering from the VITS College of Engineering, Visakhapatnam, Andhra Pradesh, India, in 2012.He is currently pursuing hismaster's degree in Computer Technology from the National Institute of Technology (NIT), Raipur, India. His current research interests include powerelectronic converters,application ofpower electronics in renewable energy systems, and soft computing techniques in applications of power electronics.