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A New Scheme for Nearest Level Control with Average Switching Frequency Reduction for Modular Multilevel Converters

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Abstract

This paper proposes a new NLC (Nearest Level Control) scheme for MMCs (Modular Multilevel Converters), which offers voltage ripple reductions in the DC capacitor of the SM (Sub-Module), the output voltage harmonics, and the switching losses. The feasibility of the proposed NLC was verified through computer simulations. Based on these simulation results, a hardware prototype of a 10kVA, DC-1000V MMC was manufactured in the lab. Experiments were conducted to verify the feasibility of the proposed NLC in an actual hardware environment. The experimental results were consistent with the results obtained from the computer simulations.

Key words: DC voltage balancing, HVDC (High-Voltage DC transmission), IGBT (Insulated Gate Bipolar Transistor), MMC (Modular Multi-level Converter), NLC (Nearest Level Control), Redundancy sub-modules, SM (Sub-Module)

I. INTRODUCTION

The MMC (Modular Multilevel Converter) for HVDC (High-Voltage DC transmission) applications is composed of series-connected SMs (Sub-Modules) in which IGBT (Insulated Gate Bipolar Transistor) switches and DC capacitors constitute a half-bridge circuit [1], [2]. The MMC is advantageous in that switching losses are low due to the low frequency switching, and the harmonics of the generated output voltage are low due to the large number of steps [5]-[7].

The operational reliability of the MMC is greatly affected if any of the individual SMs connected in series malfunction. Therefore, several redundancy SMs are connected in series with the normally operating SMs to replace any malfunctioning SMs among them [8], [9]. The redundancy SMs are always charged in advance and put on standby so that they can be quickly inserted and begin to operate when some normally operating SMs malfunction. Physically, the redundancy SMs cannot be distinguishable from the normally operating SMs.

Assuming that all of the SMs in each arm participate to form the output voltage, when one of the SMs malfunctions, the MMC continues operation through bypassing the faulty SM. When another SM malfunctions, this SM will also be bypassed. As a result, the MMC will operate continuously [10], [11]. Therefore, under normal status, the MMC can operate at a lower DC capacitor voltage because the DC capacitor voltage is determined by dividing the DC terminal voltage by the number of SMs per arm. In addition, the THD of the output voltage can be reduced due to an increased number of steps. However, when a SM malfunctions, the DC capacitor voltage increases because the available number of SMs per arm is reduced.

A continuous-switching avoidance NLC was applied to a MMC to reduce the average switching frequency. However, in this scheme a certain DC capacitor has a longer turn-on state and the capacitor voltage exceeds the maximum limit. A switching frequency adjustment NLC was proposed to solve this problem, in which all of the DC capacitor voltages stay within a limited value by conducting additional switching if the maximum difference of the DC capacitor voltage is larger than the limited value. One disadvantage of this scheme is that it increases the average switching frequency, which causes higher switching losses [12]. Therefore, this paper proposes an integrated modulation scheme for the NLC to reduce the average switching frequency and to limit the maximum voltage ripple of the DC capacitor [13].

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II. MMC Operation Algorithms

A. MMC Power Circuit

As shown in Fig. 1, each pole of an MMC consists of two arms, one on the top and the other on the bottom. Each arm consists of many SMs connected in series through a reactor [14], [15]. Each SM is a half-bridge circuit consisting of two IGBT switches and one DC capacitor. According to the ON/OFF operations of the top and bottom IGBT switches, the SM forms the output voltage by choosing the DC capacitor voltage V_c or zero voltage. If a current flows into the DC capacitor through the anode of the capacitor, the DC capacitor voltage increases, and if the current flows out, the DC capacitor voltage decreases. Therefore, the DC capacitor voltage varies according to the IGBT's switching state and the current direction. If the switching operations are not properly performed, the DC capacitor voltage will greatly increase or decrease so that the MMC cannot properly form the output voltage.

If the number of SMs in the upper or lower arm is N, the maximum output voltage is $N \times V_c$ and the minimum voltage is zero. Normally, some of the SMs among the number N of SMs are assigned as redundancy SMs. When any number of SMs malfunction in normal operation, the same number of redundancy SMs should be activated to replace them so that the MMC can operate continuously. Therefore, a certain voltage should always be maintained in the DC capacitors of the redundancy SMs

B. NLC (Nearest Level Control) Modulation

In general, a high-voltage large-capacity MMC consists of a large number of SMs to form AC voltage using the staircase modulation scheme and to reduce switching losses. The staircase modulation used in the MMC includes SHE (selective harmonic elimination) that determines the switching times to selectively remove certain order harmonics, EAM (equal area modulation) that determines the switching times at the points where the areas of both ends of the reference voltage are the same, and NLC that periodically samples the reference voltage to determine the switching time at a location similar to the reference values [16], [17].

The SHE and EAM greatly improve the harmonics in the output voltage. However, it is not easy to implement these controllers in real-time when the number of SMs is large, because the number of computations will be too large in such cases. On the other hand, the NLC generates a relatively higher level of output voltage harmonics. However, it is easy to implement this controller in real-time, because it does not involve too large a number of computations [18], [19].

As shown in Fig. 2, the NLC selects output levels that are closer to the reference voltage, in which the output levels are formed at every sampling moment to determine the switching time. For instance, if the size of the reference signal is 5 and the voltage is formed at level 11, the output voltage is at level

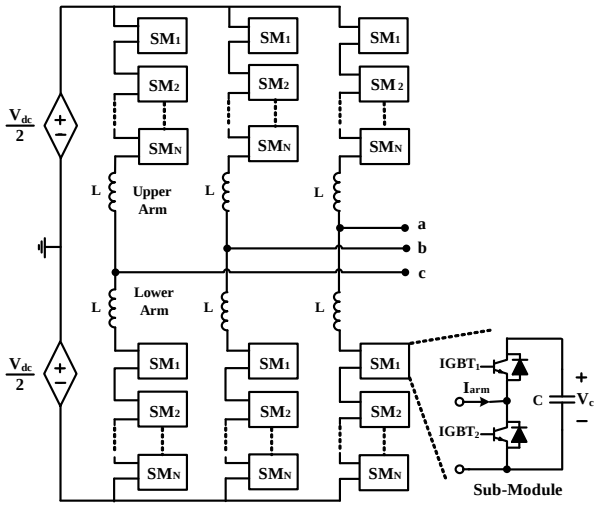


Fig. 1. Configuration of MMC with N SMs.

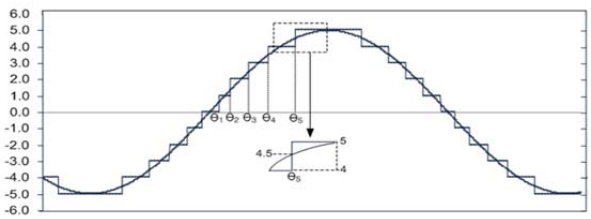


Fig. 2. Modulation scheme of NLC.

11 in the range of –5~+5 with differences of 1. Therefore, if the reference voltage is in the range of 3.5~4.5 at the moment of sampling, the output voltage will be formed at 4. Meanwhile, if the reference voltage is over 4.5, the output voltage will be formed at 5.

Since the AC voltage of the MMC is systematically formed by accumulating the DC capacitor voltages distributed in the individual SMs, the harmonic level of the AC voltage can be reduced only when the individual capacitor voltages are maintained uniformly. Therefore, the DC capacitor voltages have to be balanced [20], [21].

A common method to balance individual DC capacitor voltages is applying a bubble sorting algorithm. In this algorithm, the DC capacitor voltages are measured for each arm at every control period. Then the values are sorted and arranged in descending or ascending order for charging or discharging the DC capacitor. If the arm current flows in the direction to charge the DC capacitors, the SMs with the lowest voltage will be selected in advance. On the other hand, if the arm current flows in the direction to discharge the DC capacitors, the SMs with the highest voltage will be selected in advance.

C. Utilization of Redundancy SMs

The MMC generates a $N+1$ level output voltage with N SMs in the upper or lower arms. However, it has several redundancy SMs in preparation for the possible failure of SMs. If M redundancy SMs are added to the upper and lower

arms, *N+M* SMs participate in the operation. *N* SMs out of *N+M* SMs always operates to generate the *N+1* level output voltage, while the remaining *M* SMs are in the stand-by state.

If an SM failure occurs, the redundancy SMs must start to work immediately. The MMC must smoothly change the operation without any transient. The DC capacitor voltages of the *N+M* SMs must be maintained at V_{dc}/N at all times. Therefore, the *N+M* SMs must engage in the switching operation and keep the DC capacitor voltage of the SMs balanced.

If the MMC forms an output voltage with *N+M* SMs instead of *N* SMs, it can generate the *N+M+1* level output voltage. Therefore, the output voltage level increases by M so that the THD of the output voltage can be reduced and the DC capacitor voltage of the SMs V_c can be reduced by equation (1).

$$V_c = \frac{V_{dc}}{N+M} \tag{1}$$

III. Switching Frequency Adjustment NLC

If an SM malfunctions while the redundancy SMs participate in output voltage formation, the average DC capacitor voltages increase. If this value exceeds the allowable limit, operation becomes impossible. Therefore, a switching frequency adjustment NLC was proposed to make all of the DC capacitor voltages stay within a limited value by additional switching [11], [22].

Fig. 3 shows a flow chart for balancing the DC capacitor voltage and forming the output voltage through a switching frequency adjustment NLC. The number of SMs to be turned on is determined by applying the ROUND function to the upper arm reference voltage. If the polarity of the arm current is positive, the capacitor voltages should be arranged in ascending order for charging. However, if the polarity of the arm current is negative, the capacitor voltages should be arranged in descending order for discharging.

In the case of charging, if the capacitor voltage difference is larger than the limited voltage difference, the new sampled N_{ON_SM} number of SMs in ascending order is turned on. However, if the capacitor voltage difference is smaller than the limited voltage difference, the new sampled N_{ON_SM} is checked to see whether it is the same as the previous sampled $N_{ON\_SM\_old}$. If it is the same, the previous sampled capacitor voltages are arranged in ascending order and a switching transition occurs at the SM with the lowest capacitor voltage. If it is not the same, the new sampled capacitor voltages are arranged in ascending order and a switching transition occurs at the SM with the lowest capacitor voltage.

In the case of discharging, if the capacitor voltage difference is larger than the limited voltage difference, the new sampled N_{ON_SM} number of SMs in descending order is turned on. However, if the capacitor voltage difference is smaller than the limited voltage difference, the new sampled

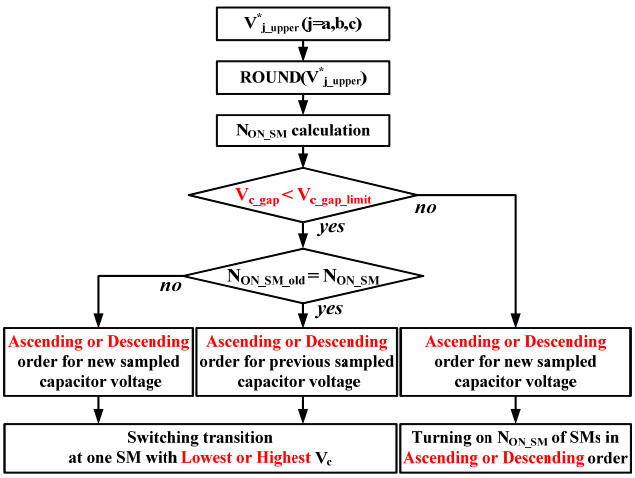


Fig. 3. Flow chart for balancing SM capacitor voltage and forming output voltage by switching frequency adjustment NLC.

TABLE I
MMC Simulation Model Parameter

Parameter	Value
DC link voltage	±500 [V]
rated power	10 [kVA]
rated current	13.0 [A]
number of SM	12 (N=10, M=2)
DC capacitor voltage	100 [V]
DC capacitor	3280 [μF]
arm reactor	10 [mH]

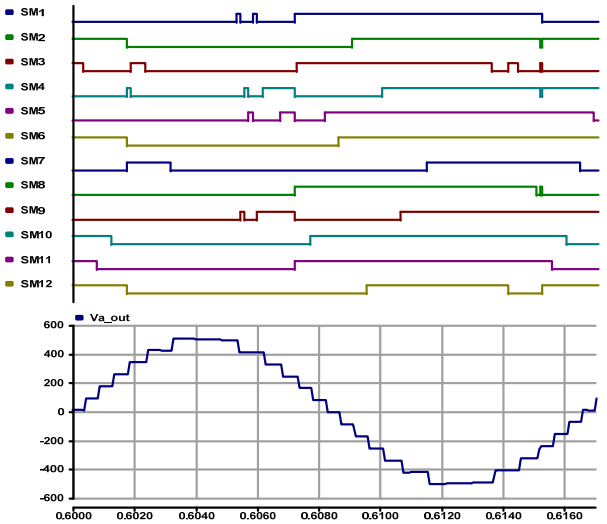
N_{ON_SM} is checked to see whether it is same as the previous sampled $N_{ON\_SM\_old}$. If, the previous sampled capacitor voltages are arranged in descending order and switching transition occurs at SM with highest capacitor voltage. If it is not the same, the new sampled capacitor voltages are arranged in descending order and a switching transition occurs at the SM with the highest capacitor voltage. The maximum limited voltage difference was set to 2.5% of the maximum voltage appearing when the MMC operates at the *N+1* level.

In order to verify the feasibility of the proposed switching scheme, computer simulations with PSCAD/EMTDC were carried out. Table I shows the circuit parameters for a MMC which has 12 SMs in the upper or lower arm (10 SMs for normal operation and 2 SMs for redundancy purposes).

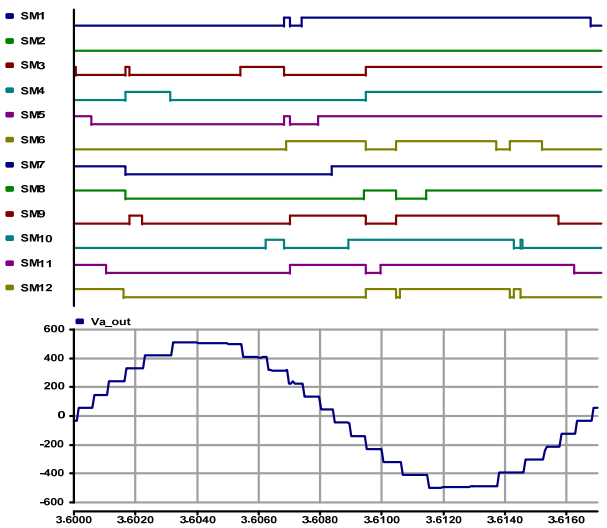
The average capacitor voltage in the proposed NLC scheme is approximately 83.33V, because 12 SMs participated in the output voltage formation. The number of switchings for each SM was checked using the average switching frequency in each level of operation, which is expressed by the following equation:

$$f_{s\_avg} = \frac{N_{ON\_T}}{N_{arm} \times T} \tag{2}$$

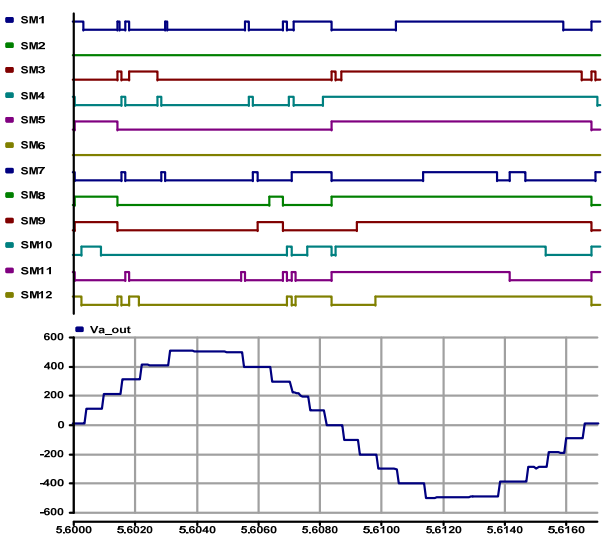
Where, f_{s_avg} is the average switching frequency, N_{arm} is the number of SMs per arm, *T* is the operation time of each level, and N_{ON_T} is the number of turned-on SMs per arm during *T*.



(a) 13-level output voltage with average switching of 167Hz.

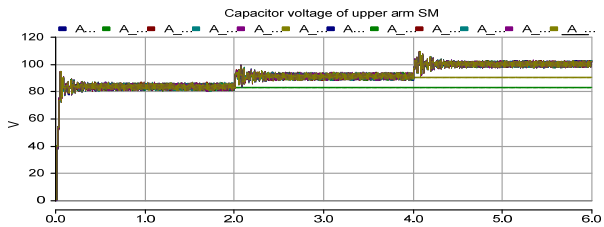


(b) 12-level output voltage with average switching of 171Hz.

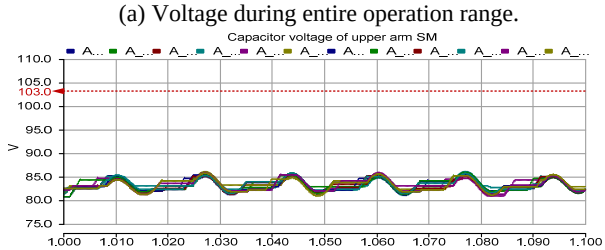


(c) 11-level output voltage with average switching of 222Hz.

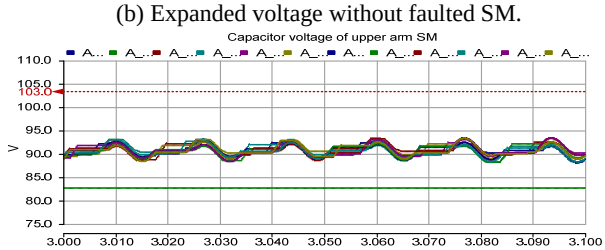
Fig. 4. Gating pulses and Output voltage by switching frequency adjustment NLC.



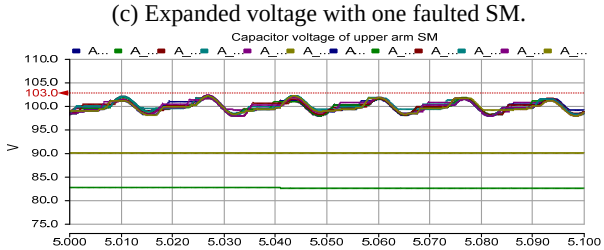
(a) Voltage during entire operation range.



(b) Expanded voltage without faulted SM.



(c) Expanded voltage with one faulted SM.



(d) Expanded voltage with two faulted SMs.

Fig. 5. DC capacitor voltages for each level of operation by switching frequency adjustment NLC.

Fig. 4(a), (b), and (c) show the gate pulses for each SM and the output voltage formed by switching frequency adjustment NLC when the MMC operates in 13-level, 12-level, and 11-level, respectively. The average switching frequencies for each operation level were calculated at 167Hz, 171Hz, and 222Hz, respectively.

Fig. 5(a) shows the variation of the DC capacitor voltages and the limited value of the DC capacitor voltage for the entire operation range. Fig. 5(b), (c), and (d) are the expanded waveforms of the DC capacitor voltages for each level of operation. Each level of operation was simulated where no SM would malfunction between 0 and 2 sec, one SM would malfunction between 2 and 4 sec, and two SMs would malfunction between 4 and 6 sec. The ripple limit of the eDC capacitor voltage was set to 103V. The DC capacitor voltages increase but they are located within the limit value of 103V as the number of faulted SMs increases. The voltage ripple decreases as the average switching frequency increases. Therefore, the MMC can operate stably during the entire range of operation even when some SMs have malfunctioned.

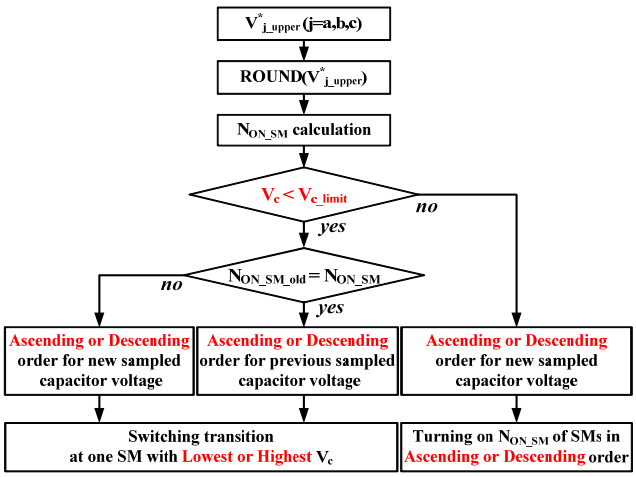


Fig. 6. Flow chart for balancing SM capacitor voltage and forming output voltage by proposed NLC.

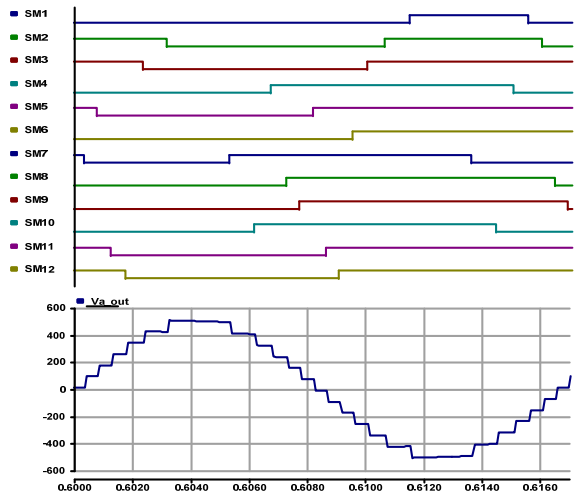
IV. Proposed Switching Scheme

In order to reduce the switching losses in a MMC, the number of switching operations should be reduced. A continuous switching avoidance NLC can provide an average switching frequency to be reduced to the power frequency. However, the DC capacitor voltage of a number of SMs with a long conduction time exceed the limited DC capacitor voltage. Therefore, the MMC cannot stably operate using only the continuous switching avoidance NLC.

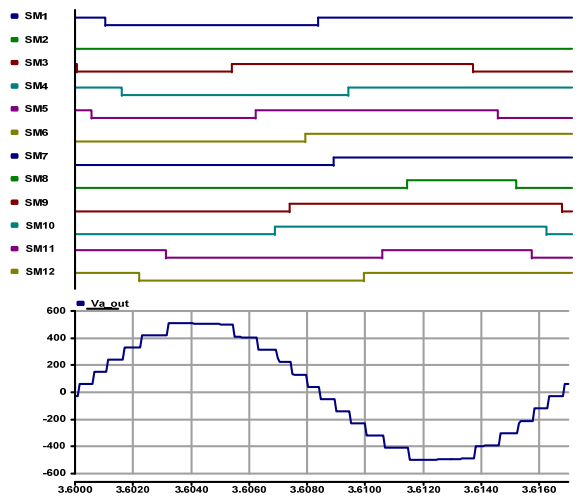
A continuous switching avoidance NLC with a maximum limited capacitor voltage was proposed so that the DC capacitor voltage does not exceed the limited voltage. It offers the lowest average switching frequency through bypassing SMs in which the capacitor voltage exceeds the limit value. The maximum limited capacitor voltage was set to the maximum capacitor voltage appearing when the MMC operates at the *N+1* level.

Fig. 6 shows a flow chart of the output voltage formation by the proposed NLC, which includes the continuous switching avoidance NLC with a maximum limited capacitor voltage. As explained in the previous scheme, the number of SMs to be turned on is determined by applying the ROUND function to the arm reference voltage. If the polarity of the arm current is positive, the capacitor voltages should be arranged in ascending order for charging. However, if the polarity of the arm current is negative, the capacitor voltages should be arranged in descending order for discharging.

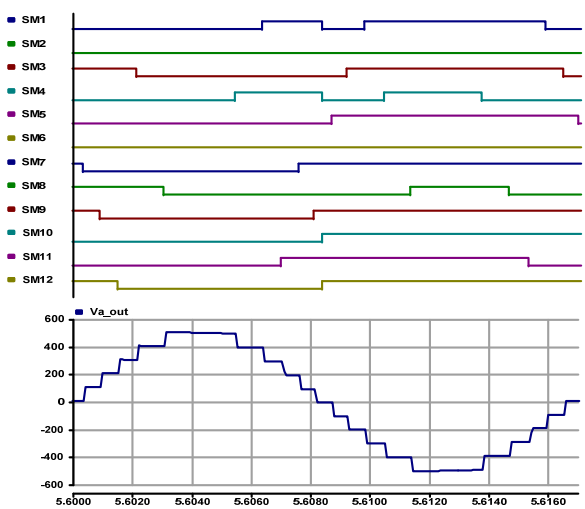
In the case of charging, if the capacitor voltage is higher than the limited voltage, the new sampled N_{ON_SM} number of SMs in ascending order are turned on. However, if the capacitor voltage is lower than the limited voltage, the new sampled N_{ON_SM} is checked to see whether it is the same as the previous sampled $N_{ON\_SM\_old}$. If it is the same, the previous sampled capacitor voltages are arranged in ascending order and a switching transition occurs at the SM with the lowest capacitor voltage. If it is not the same, the new sampled capacitor voltages are arranged in ascending order and a switching transition occurs at the SM with the lowest capacitor voltage.



(a) 13-level output voltage with average switching of 60Hz.

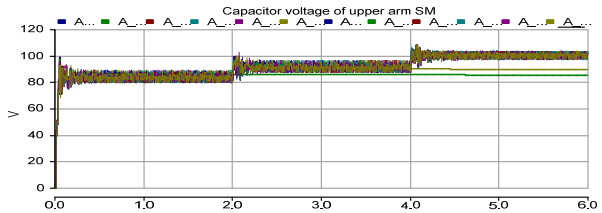


(b) 12-level output voltage with average switching of 60Hz.

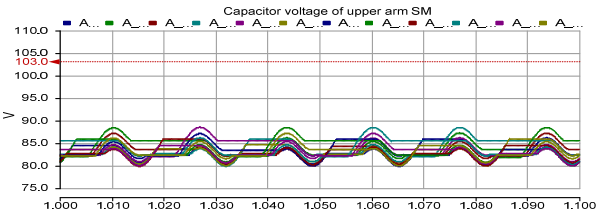


(c) 11-level output voltage with average switching of 110Hz.

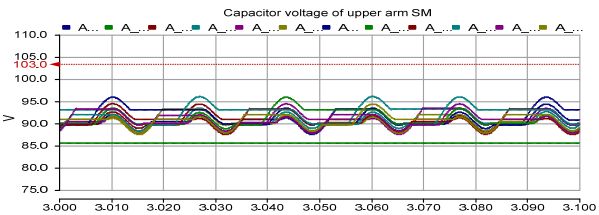
Fig. 7. Gating pulses and Output voltage by Proposed NLC.



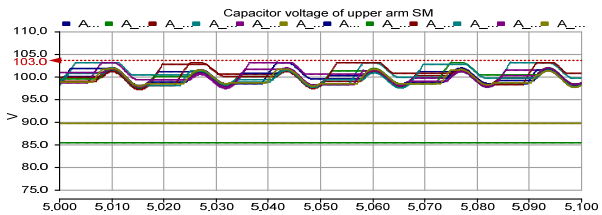
(a) Voltage during entire operation range.



(b) Expanded voltage without faulted SM.



(c) Expanded voltage with one faulted SM.



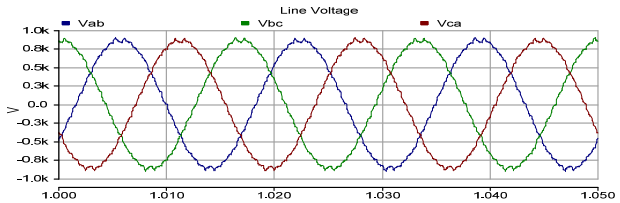
(d) Expanded voltage with two faulted SMs.

Fig. 8. DC capacitor voltages for each level of operation by proposed NLC.

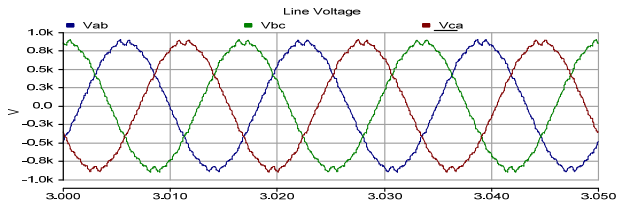
In the case of discharging, if the capacitor voltage is higher than the limited voltage, the new sampled N_{ON_SM} number of SMs in descending order are turned on. However, if the capacitor voltage is lower than the limited voltage, the new sampled N_{ON_SM} is checked to see whether it is the same as the previous sampled $N_{ON\_SM\_old}$. If it is the same, the previous sampled capacitor voltages are arranged in descending order and a switching transition occurs at the SM with the highest capacitor voltage. If it is not the same, the new sampled capacitor voltages are arranged in descending order and a switching transition occurs at the SM with the highest capacitor voltage.

Fig. 7(a), (b), and (c) show the gate pulses of each of the SMs and the output voltage formed by the proposed NLC when the MMC operates in 13-level, 12-level, and 11-level, respectively. The average switching frequencies for each operation level were calculated at 60Hz, 60Hz, and 110Hz, respectively.

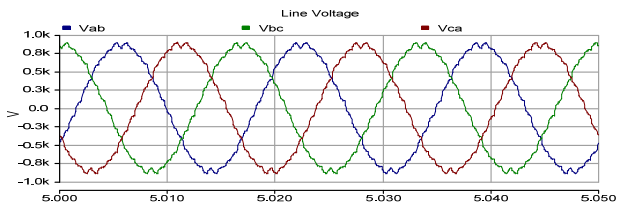
Fig. 8(a) shows the voltage variation of the DC capacitor voltages in the entire range by applying the proposed NLC for the MMC. As the number of malfunctioning SMs increases, the ripples of the DC capacitor voltage decrease. There are some transients at the transition instants. However, they are not very high. Fig. 8(b), (c), and (d) show the expanded waveforms of the DC capacitor voltages under no faulted SMs, one faulted SM, and two faulted SMs, respectively. As the number of faulted SMs increases, the average capacitor voltages increases. However, all of the capacitor voltages remain within the limit value of 103V. If any capacitor voltage exceeds the limited value, additional switching occurs based on the limited value. Through this process, all of the SM capacitor voltages stay under the limited voltage during the entire operation range.



(a) 13-level operation.



(b) 12-level operation.



(c) 11-level operation.

Fig. 9. Line-to-line AC output voltage by proposed NLC.

TABLE II
COMPARISON OF AVERAGE SWITCHING FREQUENCY

Operation Level	13-level	12-level	11-level
Switching Frequency Adjustment NLC	161	162	210
Proposed NLC	60	60	110

Fig. 9 shows the 3-phase line-to-line AC voltages formed by the proposed NLC according to changes of the operation level due to a faulted SM. Through simulation analyses, the THD of the output voltage was 2.1% when the MMC operates at the 13-level including two redundancy SMs in normal operation. However, the THD of output voltage was 3.1% when the MMC operates at the 11-level.

Table II shows a comparison of the results of the average switching frequency when the switching frequency adjustment NLC and the proposed NLC were applied in cases where the SMs operate normally and in cases where the SMs had malfunctioned. When the proposed NLC was applied, although the average switching frequency increased as the SMs malfunctioned, the average switching frequency was much lower for the entire operation range than the cases where the switching frequency adjustment NLC was applied. This fact can be confirmed by comparing the gate pulses shown in Fig. 4 and Fig. 7.

V. Experimental Verification

A. MMC Hardware Configuration

Fig. 10 shows a scaled prototype of a 10kVA 11-level MMC built in the laboratory. This system comprises three racks, one for each phase, where each rack is composed of six floors with four SMs installed on each floor. A total of 24 SMs in each rack constitute the top and bottom arms, and arm reactors are installed at the bottom of the individual racks depending on their weight.

Each SM consists of four optic terminals, two gate drives, two IGBTs, one DC capacitor, one relay, one capacitor voltage sensor, and one output voltage terminal. Each SM has RX optic terminals that receive two gate signals for driving the IGBTs, one relay driving signal to protect the SM from the controller, and one TX optic terminal that sends a fault signal to the controller when a fault occurs in an SM.

B. MMC Controller Structure

The controllers for the scaled prototype consist of one master controller and six arm controllers. Two of the arm controllers supply gate signals to the SMs located on the top and bottom of each bed and receive fault signals generated by each SM.

Fig. 11 shows a connection diagram between the master controller and the arm controllers. The master controller transmits information on the reference voltage and current polarity for the voltage balancing algorithm to the arm controllers, and issues operation commands to the arm controllers. The master controller takes care of the output voltage formation. Meanwhile the arm controllers implement the SM capacitor voltage balancing algorithm, the SM Gate signal generation algorithm, and the redundancy SM input algorithm.

The arm controllers are in charge of 12 SMs receiving voltage sensing information, maintaining voltage balancing, and transmitting gate signals to the SMs through optical communication via the optic board. In addition, the arm controllers operate the relays when a fault occurs and the SMs send signals to the arm controllers when a fault has been detected. These fault signals are transmitted to the master

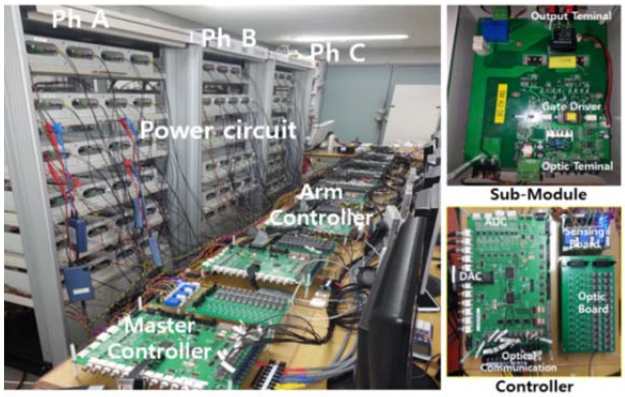


Fig. 10. Scaled prototype of 10kVA 11-level MMC.

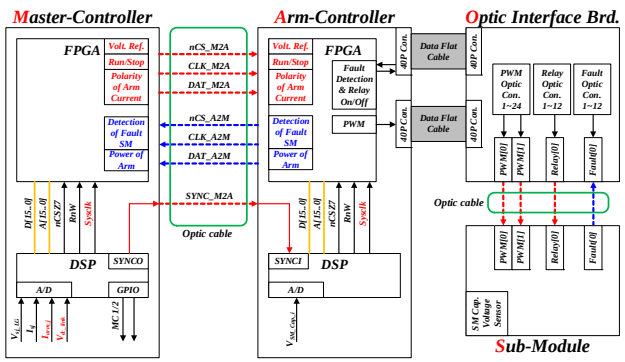


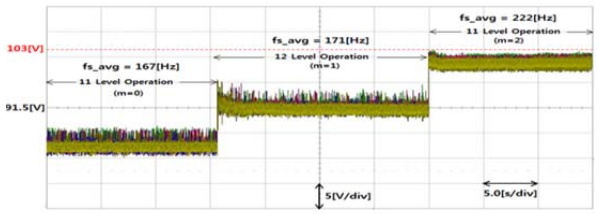
Fig. 11. Structure of MMC controller.

controller through the arm controllers, and the master controller takes appropriate action based on the signals.

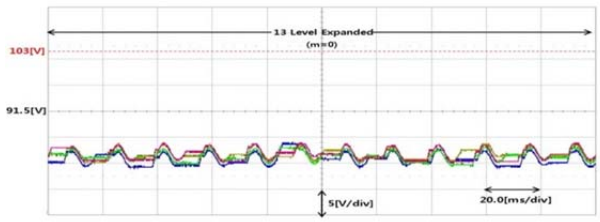
The arm controllers were made using a TMS320F28335 DSP and a XC6SLX100-3FGG484 FPGA. Each peripheral circuit consists of a DAC port, an ADC port, a CAN communication port, an SCI communication port, a gate pulse port, and a relay port. A total of 24 driving signals are sent through the gate pulse port. One is sent to each of the upper and lower IGBTs in the 12 SMs. These 24 driving signals are converted into optic signals through the optic board and transmitted to the SMs. In addition, 12 signals for driving the SM relay and fault signals sent from the SMs are exchanged through the optic board. Communications between the controllers are made through optic communications. Two TXs and two RXs are in charge of these communications. One of them is in charge of the clocks for the communication and the other is in charge of data. They can exchange up to 64 bits of information for a maximum four words.

C. Scaled-Prototype Experimental Result

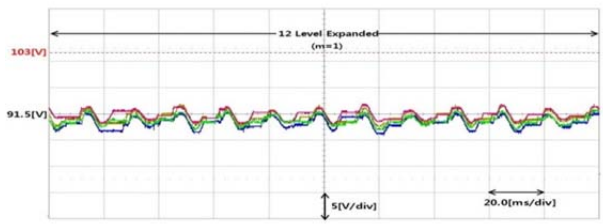
Fig. 12(a) shows the DC capacitor voltages of the switching frequency adjustment NLC to check the operation of the MMC before and after the SMs malfunctioned. The average voltage of the DC capacitor was 83.33V in the 13-level operation when no SMs malfunctioned. According to the voltage band gap setting, all of the DC capacitor voltages stayed within the limit value of 103V. At that time, the



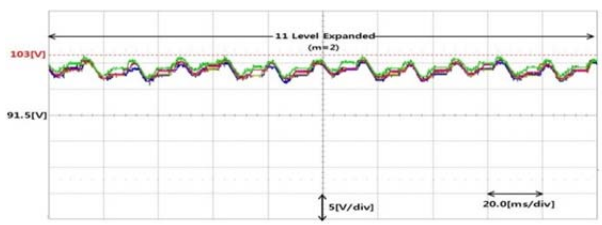
(a) Capacitor voltage for entire operation range.



(b) Expanded waveform of 13-level operation.

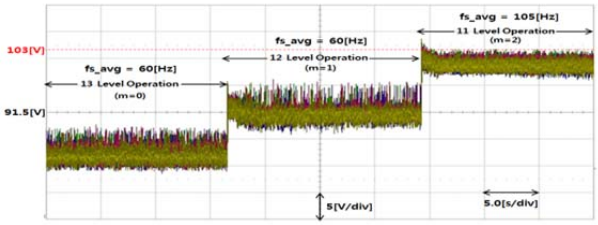


(c) Expanded waveform of 12-level operation.

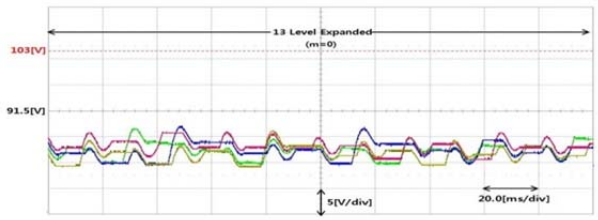


(d) Expanded waveform of 11-level operation.

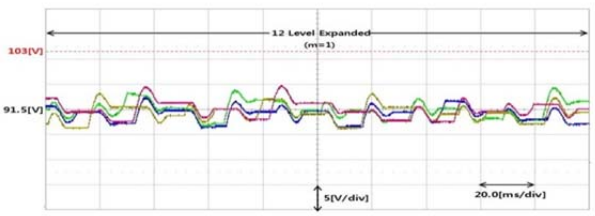
Fig. 12. DC capacitor voltages for each level of operation by switching frequency adjustment NLC.



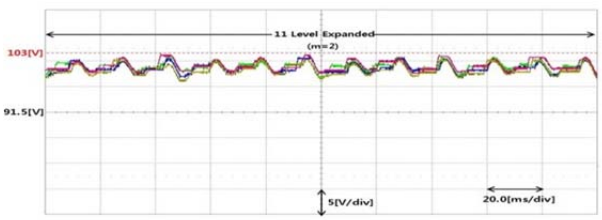
(a) Capacitor voltage for entire operation range.



(b) Expanded waveform of 13-level operation.



(c) Expanded waveform of 12-level operation.



(d) Expanded waveform of 11-level operation.

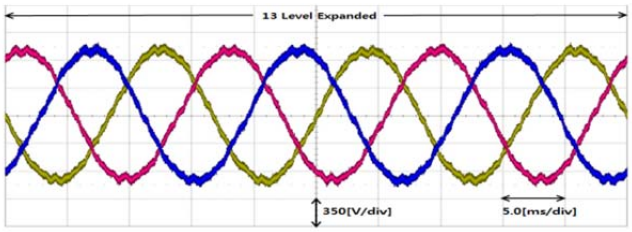
Fig. 13. DC capacitor voltages for each level of operation by proposed NLC.

average switching frequency was 167Hz. If the MMC operates at the 12-level, the average DC capacitor voltages increase from 83.33V to 90.91V. The average switching frequency was increased from 167Hz to 171Hz. By reducing the voltage band gap, all of the DC capacitor voltages are located within the limit value of 103V at the 11-level operation. The average switching frequency was increased from 171Hz to 222Hz. Fig. 12(b), (c), and (d) show the expanded waveforms of the DC capacitor voltages under no faulted SMs, one faulted SM, and two faulted SMs, respectively. As the number of faulted SMs increases, the average capacitor voltages increase. However, all of the capacitor voltages remain within the limit value of 103V for the entire operation range.

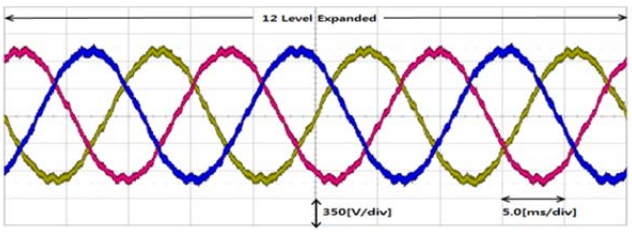
Fig. 13(a) shows the voltage variation of the DC capacitor voltages in the whole range by applying the proposed NLC scheme for the MMC. As the number of malfunctioning SMs increases, the ripples of the DC capacitor voltages decrease.

There are some transients at the transition instants. However, they are not very high. Fig. 13(b), (c), and (d) show the expanded waveforms of the DC capacitor voltages under no faulted SMs, one faulted SM, and two faulted SMs, respectively. As the number of faulted SMs increases, the average capacitor voltages increase. However, all of the capacitor voltages remain within the limit value. If any capacitor voltage exceeds the limited value of 103V, additional switching occurs based on the limited value. Through this process, all of the SM capacitor voltages stay under the limited value of 103V during the whole operation.

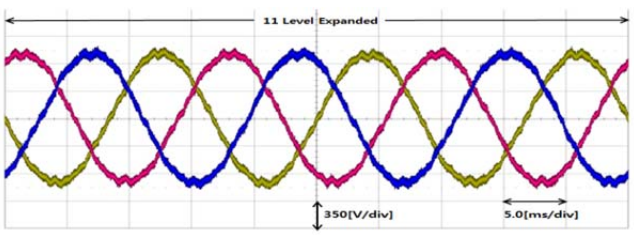
Fig. 14 shows the 3-phase line-to-line AC voltages formed by the proposed NLC according to changes of the operation level due to faulted SMs. According to the simulation analysis, the THD of the output voltage was 2.3% when the MMC operates in the 13-level including two redundancy SMs. However, the THD of the output voltage was 3.5% when the MMC operates in the 11-level. It is confirmed that the



(a) 13-level operation.



(b) 12-level operation.



(c) 11-level operation.

Fig. 14. Line-to-line AC output voltage by proposed NLC.

experimental results are very close to the simulation results shown in Fig. 9.

VI. CONCLUSION

This paper proposes a new NLC scheme for MMCs with redundancy SMs so that the output voltage harmonics and the average switching frequencies can be reduced and the voltage across the individual DC capacitors of the SMs can be limited to within a certain level even under some SMs malfunctions.

When some SMs malfunction, they are bypassed and the remaining SMs operate with a switching frequency adjustment NLC so that the individual DC capacitor voltage can stay within the maximum limit. However, the switching losses increase due to the increased average switching frequencies. To solve this problem, a new switching scheme called a continuous switching avoidance NLC with maximum voltage-ripple limiting was proposed.

To verify the feasibility of the proposed scheme, the operation of an MMC consisting of 10 normal operating SMs and 2 redundancy SMs was examined. In order to verify the proposed scheme, a large number of computer simulation were carried out. In addition, a scaled hardware prototype consisting of 10 normal operating SMs and 2 redundancy SMs was manufactured and large numbers of experiments were conducted. The experimental results were quite consistent with the computer simulation results.

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REFERENCES

[1] P. Breseti, W. L. Kling, R. L. Hendriks, and R. Vailati, "HVDC connection of off-shore wind farms to the transmission system," *IEEE Trans. Energy Convers*., Vol. 22, No. 1, pp. 37-43, Mar. 2007.

[2] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-Based HVDC power transmission systems: an overview," *IEEE Trans. Power Electron*., Vol. 24, No. 3, pp. 592-602, Mar. 2009.

[3] R. Marquardt, "Modular multilevel converter: a universal concept for HVDC networks and extended DC-bus-applications," in *International Power Electronics Conference(IPEC)*, pp. 502-507, Jun. 2008.

[4] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *IEEE Power Electronics Specialists Conference(PESC)*, pp. 174-179, Jun. 2008.

[5] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converter on electromagnetic transient simulation programs," *IEEE Trans. Power Del.*, Vol. 26, No. 1, pp. 316-324, Jan. 2011.

[6] J. Xu, C. Zhao, W. Liu, and C. Guo, "Accelerated model of modular multilevel converters in PSCAD/EMTDC," *IEEE Trans. Power Del.*, Vol. 28, No. 1, pp. 129-136, Jan. 2013.

[7] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.*, Vol. 28, No. 8, pp. 3702-3713, Aug. 2013.

[8] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2633-2642, Aug. 2010.

[9] Q. Tu, Z. Xu, Y. Chang, and L. Guan, "Suppression DC voltage ripples of MMC-HVDC under unbalanced grid conditions," *IEEE Trans. Power Del*., Vol. 27, No. 3, pp. 1332-1338, Jul. 2012.

[10] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electron*., Vol. 27, No. 1, pp. 57-68, Jan. 2012.

[11] Q. Tu, Z. Xu, and L. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del*., Vol. 26, No. 1, pp. 298-306, Jan. 2011.

[12] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del*., Vol. 26, No. 3, pp. 2009-2017, Jul. 2011.

[13] K. Ilves, A. Antonopoulos, S. Norrga, and H-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron*., Vol. 27, No. 8, pp. 3482-3494, Aug. 2012.

[14] E. Solas, G. Abed, J. A. Barrena, A. Carcar, and S. Aurtenetxea, "Modulation of modular multilevel converter for HVDC application," in 14th International Power Electronics and Motion Control Conference(EPE/PEMC), pp. T2-84-T2-89, Sep. 2010.
[15] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for modular multilevel converters," *IEEE Trans. Power Electron*., Vol. 28, No. 11, pp. 4873-4879, Nov. 2013.
[16] Y. Liu, H. Hong, and A. Huang, "Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation," *IEEE Trans. Ind. Electron*., Vol. 56, No. 6, pp. 2249-2258, Jun. 2009.
[17] Q. Song, W. Liu, X. Li, and H. Rao, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron*., Vol. 28, No. 8, pp. 3702-3713, Aug. 2013.
[18] M. Hagiwara and H. AKagi, "PWM control and experiment of modular multilevel converters," in *IEEE Power Electronics Specialist Conference(PESC)*, pp. 154-161, Jun. 2008.
[19] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converter," *IEEE Trans. Power Electron*., Vol. 27, No. 8, pp. 3472-3481, Aug. 2012.
[20] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts-part I: capacitor voltage balancing method," *IEEE Trans. Ind. Electron*., Vol. 60, No. 10, pp. 4525-4535, Oct. 2013.
[21] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts-part II: experimental validation and comparison for HVDC application," *IEEE Trans. Ind. Electron*., Vol. 60, No. 10, pp. 4536-4545, Oct. 2013.
[22] G. S. Konstantinou, M. Ciobotaru, and V. G. Agelidis, "Effect of redundant sub-module utilization on modular multilevel converters," in *IEEE International Conference on Industrial Technology(ICIT)*, pp. 815-820, Mar. 2012.

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