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An Improved Phase-Shifted Carrier Pulse Width Modulation Based on the Artificial Bee Colony Algorithm for Cascaded H-Bridge Multilevel Inverters

Xinjian Cai[†,*], Zhenxing Wu[**], Quanfeng Li[***], and Shuxiu Wang[**]

[†]State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China
[*]College of Information Science and Engineering, Fujian University of Technology, Fuzhou, China
[**]National Key Laboratory for Vessel Integrated Power System Technology, Wuhan, China
[***]School of Electrical Engineering, Zhejiang University, Hangzhou, China

Abstract

Cascaded H-bridge multilevel (CHBML) inverters usually include a large number of isolated dc-voltage sources. Some faults in the dc-voltage sources result in unequal cell dc voltages. Unfortunately, the conventional phase-shifted carrier (PSC) PWM method that is widely used for CHBML inverters cannot eliminate low frequency sideband harmonics when the cell dc voltages are not equal. This paper analyzes the principle of sideband harmonic elimination, and proposes an improved PSCPWM that can eliminate low frequency sideband harmonics under the condition of unequal dc voltages. In order to calculate the carrier phases, it is necessary to solve transcendental equations for low frequency sideband harmonic elimination. Therefore, an approach based on the artificial bee colony (ABC) algorithm is presented in this paper. The proposed PSCPWM method enhances the reliability of CHBML inverters. The proposed PSCPWM is not limited to CHBML inverters. It can also be applied to other types of multilevel inverters. Simulation and experimental result obtained from a prototype CHBML inverter verify the theoretical analysis and the achievements made in this paper.

Key words: Artificial bee colony algorithm, Cascaded H-bridge multilevel (CHBML) inverter, Phase-shifted carrier pulse width modulation (PSCPWM), Unequal dc voltages

I. INTRODUCTION

Cascaded H-bridge multilevel (CHBML) inverters are widely used for motor drives and photovoltaic power conversion, because of advantages such as high-voltage output, improved electromagnetic compatibility, extreme modularity and a reduced number of components for synthesizing the same number of voltage levels [1]-[8]. The phase-shifted carrier (PSC) PWM is a commonly used modulation technique for CHBML inverters because it is easy to use and convenient for controlling the output power of individual H-bridge cells [9]-[12]. Unfortunately, the low frequency sideband harmonics elimination of the conventional PSCPWM only operates under the condition of equal cell dc voltages.

CHBML inverters need a large number of isolated dc voltage sources. This reduces the reliability of CHBML inverters, so the ability to ride through cell dc source faults is required [13]-[18]. Some cell dc source faults lead to a drop in the dc voltage. Therefore, the cell dc voltages are unequal. Some differences in the cell dc source parameters lead to unequal cell dc voltages too. Therefore, the capability of

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[†]Corresponding Author: cxj2001@fjut.edu.cn
Tel: +86-27-88390145, Huazhong Univ. of Science and Technology
[*]College of Information Science and Engineering, Fujian University of Technology, China
[**]National Key Laboratory for Vessel Integrated Power System Technology, China
[***]School of Electrical Engineering, Zhejiang University, China

operating under the condition of unequal cell dc voltages is necessary for improving the reliability. However, the conventional PSCPWM cannot cancel low frequency sideband harmonics under the condition of unequal cell dc voltages. As a result, the output voltage waveform quality is reduced. On the other hand, high power CHBML inverters usually operate with a low carrier frequency to improve efficiency. In most applications, such as induction motor drives, reductions of the carrier frequency increase the current ripples, which are produced by the sideband harmonics around the carrier and double carrier frequency. Therefore, designing a PSCPWM that can cancel low frequency sideband harmonics under the condition of unequal dc voltages will improve the performance of CHBML inverters.

Recently, many researchers have been paying attention to CHBML inverters with unequal cell dc voltages and have proposed many modulation methods [19]-[26]. Some researchers are interested in selective harmonic elimination (SHE) PWM under the condition of unequal dc voltages [19], [20]. This modulation method regulates the switching angles according to the different cell dc voltages to eliminate selective harmonics. In [21] and [22], selective harmonic mitigation (SHM) PWM techniques were developed for CHBML inverters with unequal dc voltages. However, the complexity of calculating the switching angles increases greatly when the number of voltage levels rises. As a result, the use of SHEPWM and SHMPWM is limited. In [24], a fast space vector modulation (SVM) technique for inverters with non-constant dc sources is presented. Considering the large number of space vectors, SVM is difficult to apply to multilevel inverters when the number of voltage levels is great. A commonly used modulation technique for CHBML inverters is the PSCPWM because of the modularity of this topology. Unfortunately, the PSCPWM technique of CHBML inverters with unequal dc voltages has not yet been published. This paper proposes a new PSCPWM, in which the carrier phases are calculated and regulated according to different dc voltages, to eliminate low frequency sideband harmonics.

The calculation of the carrier phases needs to solve nonlinear transcendental equations for the sideband harmonics elimination. Many methods have been presented to solve nonlinear transcendental equations. A systematic approach involves converting the transcendental equations into an equivalent set of polynomial equations [27]. Then they can be solved by use of the mathematical theory of resultants. However, considering the large degrees of the equivalent polynomial equations describing the problem of the proposed PSCPWM, this is not an effective approach. Many heuristic algorithms, such as particle swarm optimization (PSO), have been employed for solving transcendental equations [28, 29]. Furthermore, some heuristic algorithms have been applied to the modulation methods for multilevel inverters. In [28], a method based on PSO is used to solve the transcendental equation of SHEPWM. Until now, a method to solve the problem of PSCPWM under the condition of unequal dc voltages has not been found in the literature. This paper presents an approach based on the artificial bee colony algorithm to calculate the cell carrier phases.

This paper is organized as follow. Section II introduces the principle of sideband harmonics elimination. Then it determines the reason why the conventional PSCPWM cannot cancel low frequency sideband harmonics under the condition of unequal dc voltages. Section III proposes a PSCPWM that can eliminate the sideband harmonics under the condition of unequal dc voltages. Section IV presents an approach, based on the artificial bee colony (ABC) algorithm, to calculate the carrier phases. Section V offers simulation and experimental results. Section VI provides a conclusion to this paper and discusses a potential research area.

II. The Topology of CHBML Inverters and the Low Frequency Sideband Harmonics Problem

All of the single-phase legs of three-phase CHBML inverters include several cascaded H-bridge cells consisting of a single-phase full-bridge (H-bridge) dc-to-ac converter and an isolated dc source. The topology of the single-phase leg of CHBML inverters is shown in Fig. 1.

In this paper, asymmetrical regular sampled PWM is adopted for the H-bridge cell. The inverter output voltage is analyzed by use of the double Fourier integral analysis [30], [31]. The output phase voltage can be expressed as:

$$\begin{aligned} u_{CH}(t) = {} & \frac{4k_f}{\pi}\sin\left(\frac{\pi}{2k_f}+\frac{\pi}{2}\right)\sin\left(\omega_m t-\frac{\pi}{k_f}\right)J_1\left(\frac{m\pi}{2k_f}\right) \\ & \cdot\sum_{h=1}^{N}U_{dch}+\sum_{b=2}^{\infty}\frac{4k_f}{b\pi}\sin\left(\frac{b\pi}{2k_f}+b\frac{\pi}{2}\right)\sin(b\omega_m t \\ & -\frac{b\pi}{k_f})J_b\left(\frac{bm\pi}{2k_f}\right)\sum_{h=1}^{N}U_{dch}+\sum_{a=2,4}^{\infty}\sum_{b=\pm1,3}^{\pm\infty}\frac{4}{d\pi} \\ & \cdot\sin\left(d\frac{\pi}{2}+b\frac{\pi}{2}\right)J_b\left(\frac{dm\pi}{2}\right)\sum_{h=1}^{N}U_{dch}\sin\left[a(\omega_s t \right. \\ & \left. -\frac{d}{a}\pi-\theta_{psh})+b(\omega_m t-\pi/k_f)\right] \end{aligned} \quad (1)$$

In Equ. (1), ω_s is the frequency of the carrier waveform; ω_m is the modulating frequency; m is the amplitude modulation index; N represents the number of cascaded cells; U_{dch} and θ_{psh} are the dc voltage and the carrier phase of cell h, respectively; $J_1(m\pi/2)$, $J_b[bm\pi/(2k_f)]$ and $J_b(dm\pi/2)$ are all Bessel functions of the first kind; "a" and "b" are both integers; and "$a\omega_s t+b\omega_m t$" denotes the frequency of the "b" order sideband harmonics around the "a" times carrier frequency. The ω_s-to-ω_m ratio k_f and the variable "d" are

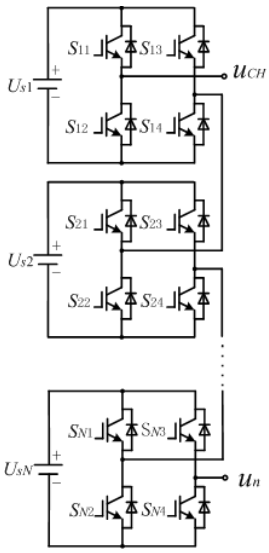


Fig. 1. Topology of a single-phase leg of CHBML inverters.

defined as:

$$k_f = \omega_s / \omega_m \tag{2}$$

$$d = a + b / k_f \tag{3}$$

It can be observed that the cell output voltage shown in Equ. (1) can be divided into three parts: 1) the first term in (1) denotes the fundamental wave; 2) the second term defines the baseband harmonics; 3) the third term defines the sideband harmonics around the carrier frequency. Since this paper does not include the elimination of baseband harmonics, the expression of the sideband harmonics is separated from Equ. (1) and converted into a summation of the phasors, as shown in Equ. (4).

$$M_{ab} \sum_{h=1}^{N} U_{dch} e^{-ja\theta_{psh}} \tag{4}$$

$$M_{ab} = \frac{4}{d\pi} \sin\left(d\frac{\pi}{2} + b\frac{\pi}{2} \right) J_b\left(\frac{dm\pi}{2} \right) \tag{5}$$

If the dc voltages are equal, they can be expressed as:

$$U_{dc1} = U_{dc2} = \cdots = U_{dcN} = U_{dce} \tag{6}$$

The conventional PSCPWM can completely eliminate the low frequency sideband harmonics only by setting the carrier phases $\theta_{psh}=\pi(h\text{-}1)/N$. The principle of the sideband harmonic cancellation can be expressed as:

$$M_{ab} U_{dce} \sum_{h=1}^{N} e^{-j[a\pi(h-1)/N]} = 0 \quad (a = 2,4,\ldots 2N-2) \tag{7}$$

Under the condition of unequal cell dc voltages, the low frequency sideband harmonics around $2f_s$, $4f_s$, … , $2(N\text{-}1)f_s$ ($f_s=\omega_s/2\pi$) cannot be removed by the conventional PSCPWM, because the summation of the low frequency sideband harmonics of the cascaded H-bridge cells are not zero, as shown in Equ. (8). As a result, the output power quality is significantly reduced.

$$M_{ab} \sum_{h=1}^{N} U_{dch} e^{-j[a\pi(h-1)/N]} \neq 0 \quad (a = 2,4,\ldots,2N-2) \tag{8}$$

III. THE PROPOSED PSCPWM

As can be seen from the analysis in Section II, the low frequency sideband harmonics cannot be cancelled by means of the conventional PSCPWM when the dc voltages are not equal. It can be found from Equ. (4) that the sideband harmonics around af_s can be eliminated by regulating the carrier phases (θ_{psh}) according to the different dc voltages. This principle can be expressed as:

$$M_{ab} \sum_{h=1}^{N} U_{dch} e^{-ja\theta_{psh}} = 0 \tag{9}$$

The low frequency sideband harmonics are more difficult to filter and they usually produce greater current ripples on the load. Therefore, eliminating the low frequency sideband harmonics is a priority. Since one of the cell carrier phases is usually set to zero, only N-1 carrier phases can be regulated. On the other hand, the output voltage sideband harmonics of the H-bridge cell handled by the asymmetrical regular sampled PWM only exist around even times the carrier frequency harmonic. As a result, the low frequency sideband harmonics around $2f_s$, $4f_s$, … , kf_s can be cancelled only by regulating the N-1 carrier phases. This principle is expressed as:

$$\begin{aligned} M_{ab} \sum_{h=1}^{N} U_{dch} \cos(a\theta_{psh}) = 0 \quad (a = 2,4,\ldots,k) \\ M_{ab} \sum_{h=1}^{N} U_{dch} \sin(a\theta_{psh}) = 0 \quad (a = 2,4,\ldots,k) \end{aligned} \tag{10}$$

In Equ. (10), k is an even number. If N is an even number, k=N-2. If N is an odd number, k=N-1. The exact carrier phases for the low frequency sideband harmonics elimination are defined as the solution of Equ. (10).

IV. APPROACH BASED ON THE ARTIFICIAL BEE COLONY ALGORITHM

Karaboga proposed the artificial bee colony (ABC) algorithm in 2005 [32]. This heuristic method is developed based on imitating the foraging behavior of a bee swarm. In ABC algorithms, a colony of artificial bees includes employed bees, onlooker bees and scout bees. In general, the number of employed bees and onlooker bees are both N_b, which is equal to the number of food sources. Employed bees search for available food sources and gather necessary information, which will be passed on to the onlooker bees. The onlooker bees select good food sources from the found food sources and further investigate them. When the quality of a food source is not improved through a predetermined number of iterations, the food source is abandoned and the employed bee becomes a scout bee that searches a new food source in the entire available space. Each position of food sources denotes a possible solution to the optimization problem.

When the ABC algorithm is applied to calculating carrier

phases, only N-1 carrier phases need be calculated because the first cell carrier phase θ_{ps1} is usually set to zero. Each food source is an N-1 dimension vector. Food source i can be expressed as $\theta_i=[\theta_{ps2\_i}, \theta_{ps3\_i},\ldots, \theta_{psN\_i}]$, and the hth element is the carrier phase of cascaded H-bridge cell h. New food source i is also an N-1 dimension vector, and it can be expressed as $V_i=[V_{ps2\_i}, V_{ps3\_i},\ldots, V_{psN\_i}]$.

Since Equ. (10) refers to a multi-goal optimization, the direct use of the ABC algorithm to solve it is difficult. Therefore, (10) need to be reduced to a single equation. Since the magnitude of the high-order (|b|≥7) sideband harmonics around af_s is usually negligible, (10) is reduced to Equ. (11), which denotes the normalized value of the weighted average of the low-order (b= ± 1,3,5) low frequency sideband harmonics magnitude.

$$\frac{1}{3km\sum_{h=1}^{N}U_{dch}}\sum_{a=2,4}^{k}\sum_{b=\pm1,3}^{\pm5}|M_{ab}|\left\{\left[\sum_{h=1}^{N}U_{dch}\cos(a\theta_{psh})\right]^2+\left[\sum_{h=1}^{N}U_{dch}\sin(a\theta_{psh})\right]^2\right\}^{\frac{1}{2}}=0 \tag{11}$$

The objective function of the ABC algorithm can be obtained from Equ. (11), and it can be expressed as:

$$f(\theta_i)=\frac{1}{3km\sum_{h=1}^{N}U_{dch}}\sum_{a=2,4}^{k}\sum_{b=\pm1,3}^{\pm5}\left\{\left[\sum_{h=1}^{N}U_{dch}\cos(a\theta_{psh})\right]^2+\left[\sum_{h=1}^{N}U_{dch}\sin(a\theta_{psh})\right]^2\right\}^{\frac{1}{2}}|M_{ab}| \tag{12}$$

It can be observed for Equ. (12) that the value of the objective function cannot be less than zero. On the other hand, the smaller the objective function value is, the better the solution quality is. Then the fitness value of the food source i can be expressed as:

$$fit_i=\frac{1}{0.001+f(\theta_i)} \tag{13}$$

The major procedure for calculating the carrier phases is as follows:

1) The basic data for the algorithm is determined. The data includes the number of food sources, the maximum iteration number *iter_max*, the maximum value of the carrier phase θ_{ps_max}, the minimum value of the carrier phase θ_{ps_min}, the maximum cycle number that is called the *limit* for abandonment, etc.
2) The initial position of the food sources θ_i is generated. Each element of the initial θ_i is determined according to Equ. (14).

$$\theta_{psh\_i}=\theta_{ps\_\min}+rand(0,1)\left(\theta_{ps\_\max}-\theta_{ps\_\min}\right) \tag{14}$$

In Equ. (14), *rand*(0,1) represents a random value between 0 and 1. Then all of the initial food sources are evaluated by use of Equ. (12) and (13).

3) Each employed bee is sent to search the neighboring space of the food source according to Equ. (15).

$$V_i=\theta_i+rand(-1,1)\left(\theta_i-\theta_g\right) \tag{15}$$

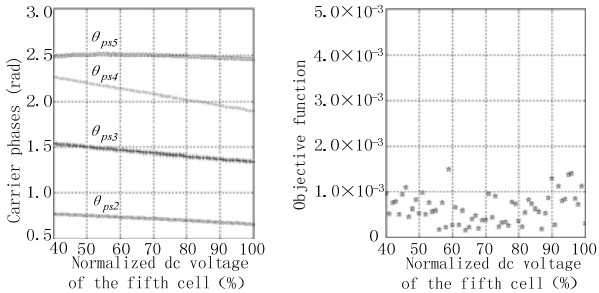
In Equ. (15), *rand*(-1,1) represents a random value between -1 and 1; $g\in\{1, 2, \ldots, N_b\}$. It is a randomly chosen index and has to be different from i. Then the fitness of the new food source is calculated by use of Equ. (12) and (13). If the fitness of the new food source is better than that of the old food source, the employed bee saves the new food source. If the fitness of the new food source is not better than that of the old food source, the employed bee remembers the old food source.
4) The employed bees go back to the hive and shares the information of the food sources with the onlooker bees. Each onlooker bee chooses a food source depending on the probability value, which is expressed as:

$$p_i=fit_i\Big/\sum_{l=1}^{N_b}fit_l \tag{16}$$

5) Each onlooker bee searches the neighboring space of the food source according to Equ. (15). The working bees then calculate the fitness of the new food source and save the position of the food source that has better fitness.
6) A food source that is not improved for a number of iterations (*limit*) is abandoned. Then the employed bee is sent to find a new food source as a scout bee.
7) If the iteration counter does not reach *iter_max*, the algorithm returns to step 3) for the next iteration. When the counter reaches *iter_max*, the algorithm stops.

Take for example a CHBML inverter in which each phase leg is composed of five cascaded H-bridge cells. The dc voltages of the 1st to 4th cells are 0.996, 1.001, 1.002 and 0.7 times the nominal dc voltage, respectively. In addition, the dc voltage of the fifth cell changes between 0.4 and 1.0 times the nominal dc voltage. As mentioned previously, the first cell carrier phase θ_{ps1} is zero. The four calculated carrier phases θ_{ps2}, θ_{ps3}, θ_{ps4} and θ_{ps5} are shown in Fig. 2(a), and the corresponding objective function values are shown in Fig. 2(b). The convergence speed for calculating the four cell carrier phases is show in Fig. 3, when the dc voltage of the fifth cell is 0.4 times the nominal dc voltage.

The other example is an inverter in which each phase leg includes nine cascaded H-bridge cells. The dc voltages of the 1st to 8th cells are 0.996, 1.0, 1.002, 1.001, 0.999, 0.997, 1.003 and 0.7 times the nominal dc voltage, respectively. In addition, the dc voltage of the ninth cell changes between 0.4 and 1.0 times the nominal dc voltage. The eight calculated carrier phases θ_{ps2}, θ_{ps3}, θ_{ps4}, θ_{ps5}, θ_{ps6}, θ_{ps7}, θ_{ps8}, and θ_{ps9} are



(a) Carrier phases. (b) Objective function values.

Fig. 2. Four calculated carrier phases and the corresponding objective function values.

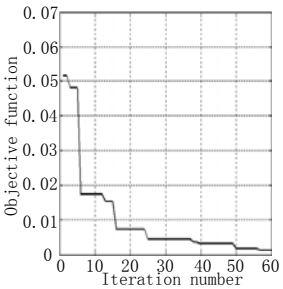
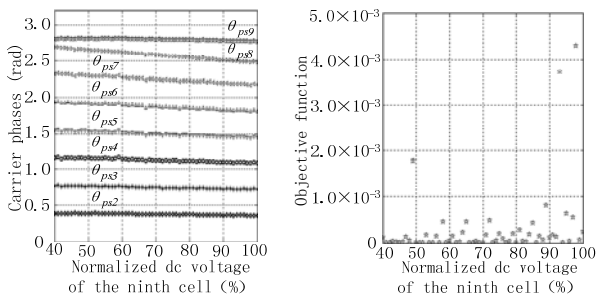


Fig. 3. Convergence speed of the calculation.



(a) Carrier phases. (b) Objective function values.

Fig. 4. Eight calculated carrier phases and the corresponding objective function values.

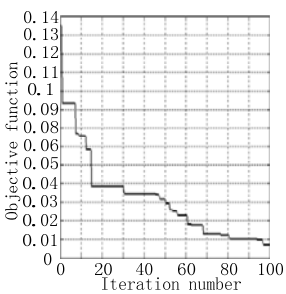
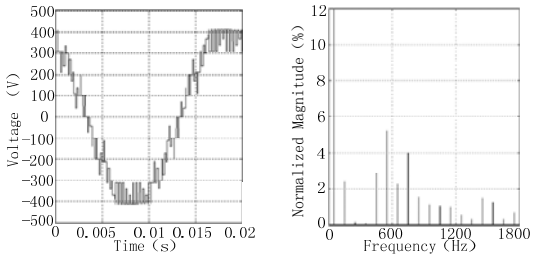


Fig. 5. Convergence speed of the calculation.

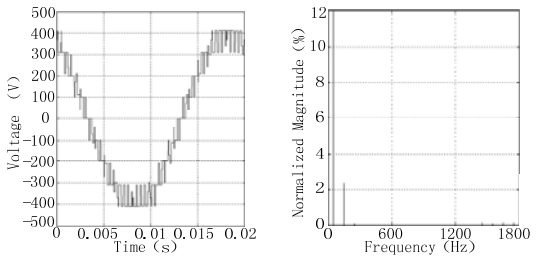
shown in Fig. 4(a), and the corresponding objective function values are shown in Fig. 4(b). The convergence speed of calculating the eight cell carrier phases is show in Fig. 5, when the dc voltage of the ninth cell is 0.4 times the nominal dc voltage.

Fig. 2 and Fig. 4 show that the carrier phases can be calculated by the use of the presented approach based on the ABC algorithm according to different dc voltages. They also show that the weighted average of the magnitude of the



(a) Voltage waveform. (b) Harmonic components.

Fig. 6. Output voltage waveform and harmonics of the conventional PSCPWM when the fifth cell dc voltage is 42V.



(a) Voltage waveform. (b) Harmonic components.

Fig. 7. Output voltage waveform and harmonics of the proposed PSCPWM when the fifth cell dc voltage is 42V.

low-order low frequency sideband harmonics can be reduced to an acceptable level. Fig. 3 and Fig. 5 show that the objective function values can be reduced to an acceptable level (lower than 0.01) within several tens of iterations. Therefore, when the calculation is applied in a digital controller such as a DSP, the calculation of the carrier phases can be achieved within several tens of mini-seconds.

V. SIMULATION AND EXPERIMENT

A mathematical model of the CHBML inverter was established by means of MATLAB/SIMULINK to verify the proposed PSCPWM method. Each single-phase leg of the three-phase CHBML inverter includes five cascaded H-bridge cells. The fundamental wave frequency is 50Hz, and the cell carrier wave frequency is 300Hz. The amplitude modulation index of each cell is 0.99. The phase voltage output is connected to a load that consists of a 1.383Ω resister and a 0.89mH inductance in series. The iteration of calculating the carrier phases is completed 3000 times per second. The cell dc voltages, the carrier phases of the conventional PSCPWM and the carrier phases calculated by use of the presented approach based on the ABC algorithm are shown in Table I.

Fig. 6 shows the phase voltage waveform and the corresponding harmonic components obtained from the conventional PSCPWM when the dc voltage of the fifth cell is 42V. The phase voltage waveform and the corresponding harmonic components of the proposed PSCPWM are shown in Fig. 7. Fig. 8 shows the current waveform obtained with the conventional PSCPWM, and when the proposed

TABLE I
DC VOLTAGES AND CARRIER PHASES OF THE CELLS

	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5
U_{dch}	99V	101V	102V	71V	42V
θ_{psh} of the conventional PSCPWM	0	$\pi/5$	$2\pi/5$	$3\pi/5$	$4\pi/5$
θ_{psh} of the proposed PSCPWM	0	0.766	1.534	2.255	2.491
U_{dch}	99V	101V	102V	71V	51V
θ_{psh} of the conventional PSCPWM	0	$\pi/5$	$2\pi/5$	$3\pi/5$	$4\pi/5$
θ_{psh} of the proposed PSCPWM	0	0.751	1.500	2.194	2.504

TABLE II
DIFFERENT COMBINATIONS OF UNEQUAL CELL DC VOLTAGES AND THE CARRIER PHASES

No	Content	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5
1	U_{dch}	99V	101V	102V	71V	62V
	θ_{psh}	0	0.734	1.465	2.133	2.507
2	U_{dch}	99V	101V	102V	71V	73V
	θ_{psh}	0	0.714	1.432	2.076	2.500
3	U_{dch}	99V	101V	102V	71V	81V
	θ_{psh}	0	0.697	1.399	2.016	2.486
4	U_{dch}	99V	101V	102V	71V	90V
	θ_{psh}	0	0.677	1.372	1.958	2.472

PSCPWM is applied after 0.05 second (t_1). Fig. 9 shows the phase voltage waveform and the corresponding harmonic components obtained from the conventional PSCPWM when the dc voltage of the fifth cell is 51V. The phase voltage waveform and the harmonic components of the proposed PSCPWM are shown in Fig. 10. Fig. 11 shows the current waveform of the load with the conventional PSCPWM, and when the proposed PSCPWM is applied after 0.05 second (t_1).

As seen from the harmonic components in Fig. 6 and Fig. 9, the conventional PSCPWM cannot eliminate the sideband harmonics around 600Hz ($2f_s$) and 1200Hz ($4f_s$). Fig. 7 and Fig. 10 show that the sideband harmonics around 600Hz and 1200Hz can be eliminated when the proposed PSCPWM is utilized. It can be observed from Fig. 8 and Fig. 11 that the current waveform contains some distortions when the conventional PSCPWM is applied (from 0 second to 0.05 second). The distortions of the current are reduced within 33 mini-second (from t_1 to t_2) when the proposed PSCPWM is applied after t_1 (0.05 second). This means that the calculation and regulation of the cell carrier phases can be achieved quickly.

In order to further verify the proposed PSCPWM, more simulations are carried out under the condition that the fifth cell dc voltage changed between 62 V and 90 V. Table II contains four combinations of unequal dc voltages and the carrier phases of the proposed PSCPWM. The carrier phases of the conventional PSCPWM are $\theta_{psh} = (h - 1)\pi/5$. Table III shows the corresponding magnitude of the significant sideband harmonics around 600 Hz (2fs) and 1200 Hz (4fs).

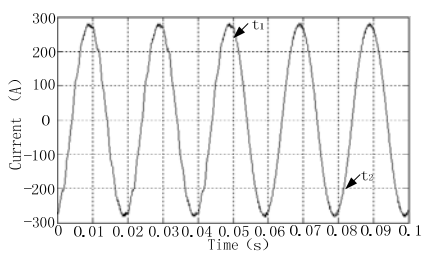
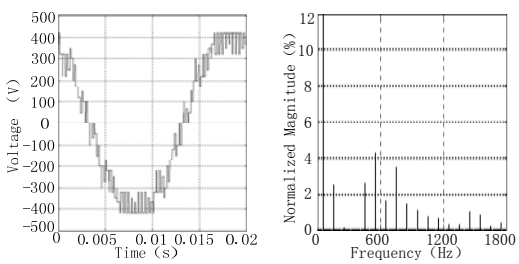


Fig. 8. Current waveform when the fifth cell dc voltage is 42V, the conventional PSCPWM is applied at first and the proposed PSCPWM is applied after 0.05 second.



(a) Voltage waveform. (b) Harmonic components.

Fig. 9. Output voltage waveform and harmonics of the conventional PSCPWM when the fifth cell dc voltage is 51V.

According to Table III, the conventional PSCPWM cannot eliminate low frequency sideband harmonics when the cell dc voltages are not equal. All of the significant sideband harmonics around 600 Hz and 1200 Hz can be almost completely eliminated when the proposed PSCPWM is applied.

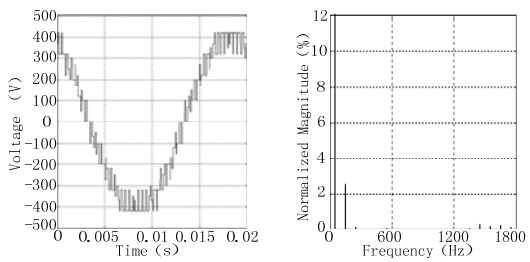
Experiments have been carried out on a CHBML inverter to verify the proposed PSCPWM technique. The topology and parameters of the inverter are identical to those of the

TABLE III
SIDEBAND HARMONICS AROUND 600 HZ AND 1200 HZ OBTAINED FROM THE SIMULATION

No	Modulation technique	Normalized magnitude of the major sideband harmonics around $2f_s$ (600Hz) and $4f_s$ (1200Hz) (%)							
		450 Hz	550 Hz	650 Hz	750 Hz	1050 Hz	1150 Hz	1250 Hz	1350 Hz
1	Conventional PSCPWM	2.15	3.55	1.39	2.91	0.55	0.49	0.24	0.25
	Proposed PSCPWM	0.01	0.02	0.01	0.03	0.02	0.03	0.01	0.02
2	Conventional PSCPWM	1.79	2.96	1.16	2.43	0.41	0.38	0.19	0.25
	Proposed PSCPWM	0.02	0.03	0.02	0.01	0.02	0.02	0.01	0.01
3	Conventional PSCPWM	1.48	2.44	0.96	2.00	0.38	0.37	0.18	0.28
	Proposed PSCPWM	0.02	0.02	0.01	0.02	0.02	0.02	0.02	0.02
4	Conventional PSCPWM	1.22	2.01	0.79	1.65	0.46	0.45	0.22	0.32
	Proposed PSCPWM	0.01	0.01	0.01	0.01	0.02	0.02	0.02	0.02

TABLE IV
SIDEBAND HARMONICS AROUND 600 HZ AND 1200 HZ OBTAINED FROM THE PROTOTYPE EXPERIMENTS

No	Modulation technique	Normalized magnitude of the major sideband harmonics around $2f_s$ (600Hz) and $4f_s$ (1200Hz) (%)							
		450 Hz	550 Hz	650 Hz	750 Hz	1050 Hz	1150 Hz	1250 Hz	1350 Hz
1	Conventional PSCPWM	1.97	3.48	1.38	2.92	0.71	0.55	0.39	0.23
	Proposed PSCPWM	0.52	0.40	0.24	0.52	0.12	0.16	0.08	0.20
2	Conventional PSCPWM	1.78	3.01	1.16	2.40	0.46	0.42	0.19	0.23
	Proposed PSCPWM	0.35	0.23	0.19	0.70	0.23	0.19	0.03	0.23
3	Conventional PSCPWM	1.47	2.53	1.09	2.15	0.26	0.45	0.11	0.26
	Proposed PSCPWM	0.34	0.30	0.15	0.61	0.11	0.12	0.11	0.10
4	Conventional PSCPWM	1.25	2.14	0.92	1.73	0.40	0.44	0.29	0.18
	Proposed PSCPWM	0.29	0.15	0.19	0.41	0.11	0.15	0.14	0.10



(a) Voltage waveform. (b) Harmonic components.

Fig. 10. Output voltage waveform and harmonics of the proposed PSCPWM when the fifth cell dc voltage is 51V.

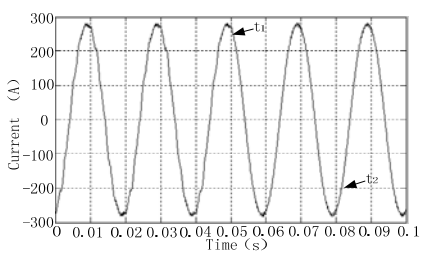
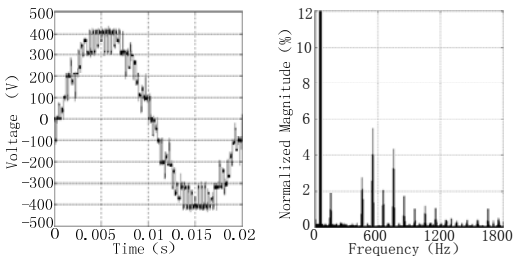


Fig. 11. Current waveform when the fifth cell dc voltage is 51V, the conventional PSCPWM is applied at first and the proposed PSCPWM is applied after 0.05 second.

simulation model. The inverter is shown in Fig. 12. Its control system consists of a main controller, cell controllers and communication devices. Each controller is composed of a low-cost DSP (TMS320F28335) and its auxiliary circuit. The main controller generates voltage (current) command values and calculates the cell carrier phases. It also handles the functions of monitoring, observation, protection, human-machine interface and the other auxiliary functions of a system. The cell controller that is installed in the H-bridge cell regulates the cell carrier phase and generates PWM signals. In addition, it can perform the functions of monitoring and protection.

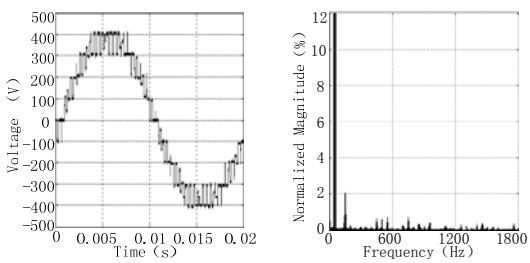
Fig. 13 shows the phase voltage waveform obtained with a digital oscilloscope and the harmonic components obtained with the fast Fourier transformation function of the digital oscilloscope when the conventional PSCPWM is applied. Fig. 14 shows the phase voltage waveform and the harmonic components when the proposed PSCPWM is used. Fig. 13 and 14 are both obtained under these conditions: 1) the first to fourth cell dc voltages are 99V, 101V, 102V and 71V, respectively; 2) the fifth cell dc voltage is 42V. Under the condition that the fifth cell dc voltage changes to 51V, Fig. 15 and Fig. 16 show the phase voltage waveform and the harmonic components of the conventional PSCPWM and the proposed PSCPWM, respectively.

Fig. 12. CHBML inverter.



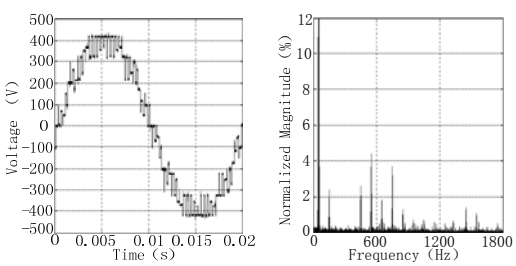
(a) Voltage waveform. (b) Harmonic components.

Fig. 13. Output voltage waveform and harmonics of the conventional PSCPWM when the fifth cell dc voltage is 42V.



(a) Voltage waveform. (b) Harmonic components.

Fig. 14. Output voltage waveform and harmonics of the proposed PSCPWM when the fifth cell dc voltage is 42V.

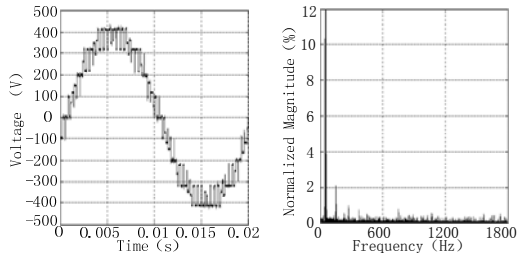


(a) Voltage waveform. (b) Harmonic components.

Fig. 15. Output voltage waveform and harmonics of the conventional PSCPWM when the fifth cell dc voltage is 51V.

Other experiments have been carried out on the prototype inverter to further verify the proposed PSCPWM, when the fifth cell dc voltage changed between 62V and 90V. The cell dc voltages and carrier phases of the proposed PSCPWM are listed in Table II. Table IV contains the corresponding magnitudes of the significant sideband harmonics around 600 Hz ($2f_s$) and 1200 Hz ($4f_s$).

It can be found from Fig. 13, Fig. 15 and Table IV that the conventional PSCPWM cannot cancel the sideband harmonics around 600Hz and 1200Hz. Fig. 14, Fig. 16 and



(a) Voltage waveform. (b) Harmonic components.

Fig. 16. Output voltage waveform and harmonics of the proposed PSCPWM when the fifth cell dc voltage is 51V.

Table IV show that the proposed PSCPWM can almost completely eliminate the low frequency sideband harmonics when the cell dc voltages are unequal and changing. Therefore, the load current distortions caused by the harmonics are reduced, and the load operates more smoothly. The prototype experimental results are slightly different than the simulation results because of the inevitable measuring error of the dc voltages and the synchronization error of the cell carrier phases.

VI. CONCLUSION AND DISCUSSION

A large number of isolated dc voltage source reduces the reliability of CHBML inverters. Therefore, the capability of riding through cell dc voltage source faults is required. Some faults of cell dc voltage sources result in unequal dc voltages. The conventional PSCPWM is unable to cancel low frequency sideband harmonics under the condition of unequal cell dc voltages, and the output power quality of CHBML inverters is reduced. Based on the principle of sideband harmonics elimination, this paper proposes a PSCPWM to remove low frequency sideband harmonics by calculating and regulating the carrier phases according to different cell dc voltages. Then an approach based on the ABC algorithm is proposed to calculate the carrier phases. The proposed PSCPWM technique preserves the merits of the conventional PSCPWM and reduces the negative consequence of unequal dc voltages, thereby enhancing the fault tolerant capability of CHBML inverters. This method can also be applied to other types of multilevel inverters, such as modular multilevel converters (MMC).

As seen from the analysis in Section II, the cell amplitude modulation indexes and the phases of the cell modulation waveform also effect the elimination of low frequency sideband harmonics. At present, many researchers are interested in balancing cell dc voltages, when the cell input voltages or loads are not equal [33-36]. Usually, a cell dc voltage balancing controller results in unequal cell amplitude modulation indexes or (and) different cell modulation waveform phases [36]. When cell dc voltage balancing is applied, low frequency sideband harmonic elimination may be an interesting research area.

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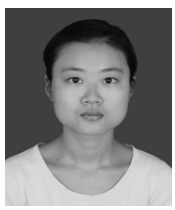
Xinjian Cai was born in Fuzhou City, Fujian Province, China, in 1979. He received his B.S. degree in Mechanical and Electrical Engineering from Fuzhou University, Fuzhou, China, in 2001; and his M.S. degree in Control Theory and Engineering from Central South University, Changsha, China, in 2008. He is presently working towards his Ph.D. degree in Power Electronics and Drives at the Huazhong University of Science and Technology, Wuhan, China. Since 2009, he has been a Research Assistant and Lecturer in the College of Information Science and Engineering, Fujian University of Technology, Fuzhou, China. His current research interests include modulation techniques of multilevel inverters, improvements in the output voltage quality of inverters, and motor control.

Zhenxing Wu was born in Hunan, China, in 1982. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2004, 2006, and 2010, respectively. He then joined the National Key Laboratory for Vessel Integrated Power System Technology, Naval University of Engineering, Wuhan, China, as a Lecturer, in 2010. His current research interests include renewable energy generation, the modeling and control of power electronic systems, and high-voltage high-power power electronic equipment.

Quanfeng Li was born in Fujian, China, in 1987. He received his B.S. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2008. He is presently working towards his Ph.D. degree in the School of Electrical Engineering, Zhejiang University. His current research interests include wind-power converters, modulation and control methods, and the modeling of power electronic circuits.



Shuxiu Wang was born in Xuzhou, China, in 1990. She received her B.S. degree in Electrical Engineering from the China University of Mining and Technology (CUMT), Xuzhou, China, in 2013. She is presently working towards her M.S. degree in the National Key Laboratory for Vessel Integrated Power System Technology, Naval University of Engineering, Wuhan, China. Her current research interests include multilevel inverters, induction motor drives, and the applications of power electronics in power systems.