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A Method to Compensate the Distorted Space Vectors in the Unbalanced Neutral Point Voltage of 3-level NPC PWM Inverters

Seung-Wook Hyun*, Seok-Jin Hong*, Jung-Hyo Lee**, Chun-Bok Lee*, and Chung-Yuen Won†

*,†Department of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea
**Automotive Component R&D Team, LG Innotek Co., Ltd., Korea

Abstract

This paper proposes a compensation method to improve the distorted space vectors when a 3-level Neutral Point Clamped (NPC) inverter has an unbalanced neutral point voltage. Since both the neutral point voltage of the DC link and the space vector of a 3-level NPC inverter are closely related depending on the output load connecting state, a distorted space vector can occur when the neutral point voltage of a 3-level NPC inverter is unbalanced. The proposed method can improve the distorted space vectors by adjusting the injection time of the small and medium vectors and by modulating the amplitude of the carrier waveforms. In this paper, the proposed method is verified by both simulation and experimental results based on a 3-level NPC inverter.

Key words: Neutral point voltage, NPC inverter, Space vector, Unbalance

I. INTRODUCTION

Recently, significant achievements have been made in terms of the topologies for renewable energy due to the advancements in switching devices and micro controller units [1]-[7]. Among them, the current wind power systems demands heavy power in the megawatt range. Therefore, the related wind power systems needs heavy power system conversion and adaptation technology. For this reason, more research on multi-level inverters is being actively conducted since they can be designed to reduce the voltage rate of switching devices when compared to 2-level inverters. Among these multi-level inverters, the topology of the 3-level neutral point clamped(NPC)type is the most popular and commonly used in this type of high power system.

Fig. 1 shows a schematic of a 3-phase 3-level NPC PWM inverter. In the NPC inverter, the neutral point of the DC link capacitors is connected to the neutral points of each phase. The 3-level NPC inverter has four IGBTs and they are connected in series with each phase. Due to this structuure, the 3-level NPCinverter can generate zero voltage depending on the switching states of the NPC inverter [8]. Therefore, it can achieve a lower voltage rate and a lower THD of the phase currents than a 2-level inverter. However, the 3-level NPC inverter has a problem with unbalancing neutral point voltage, and itcauses the distortions at output voltage and phase current.

Different compensation control methods in order to improve unbalanced neutral point voltage have been presented in [9]-[16]. General approaches for balancing neutral point voltage are calculating the injection time of small vectors based on the SVPWM of a 3-level inverter. Other methods for improving this problemareinjecting the DC offset voltage. [9], [14] In the case of predictive control, it improves this problem is alleviated by both calculating the injection vectors based on neutral point current modeling and the weighting function of the neutral point voltage [15], [16].

However, because these methods calculate the injection time of small vectors for improving the unbalanced neutral point voltage, they cannot improve distorted output voltage and or current in the transient state. Solutions for improving the distorted voltage vectors in unbalanced neutral point voltage are presented in [17]-[20]. These solutions varify the distorted

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†Corresponding Author: woncy550@gmail.com
Tel:+82-31-290-7169,Fax: +82-31-299-2623, Sungkyunkwan University
*Department of Information and Communication Engineering, Sungkyunkwan University, Korea
**Automotive Component R&D Team, LG Innotek Co., Ltd., Korea

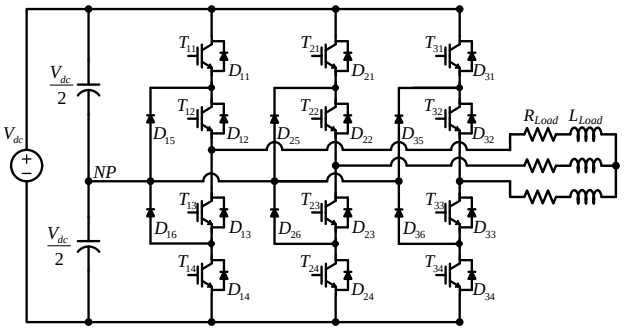

Fig. 1. Schematic of 3-level NPC PWM inverter.

space vectors when the neutral point voltage is unbalanced, and they compensate the injection time of small and medium vectors for improving this problem. However, it is difficult to improve distorted vectors with methods based on the time domain, because they calculate the injection time for 27 vectors with 24 sectors. Moreover, the general operating method of a 3-level inverter is the offset injection which is the subtraction of the minimum and maximum values of the 3-phase reference voltages. Therefore, the time domain methods cannot use offset injection PWM methods that compare carrier waveforms.

This paper presents a compensation method for improving distorted voltage vectors. It also proposesan additional method that utilizes the injection of DC offset, which makes equal usage of each DC link capacitor. The proposed method of compensation and the balancing control for the neutral point voltage are verified by simulation and experimental results.

II. Analysis of Unbalancing Unbalanced DC Link Voltage of a 3-Level Inverter

Fig. 2 shows the Sector I of the space vector diagram, Fig. 2 (a) shows that the neutral point voltage is balanced, and Fig. 2 (b) shows that it is unbalanced. In the case of Fig. 2 (a), the small vectors both POO and ONN have identical lengths and directions. The medium vector PON is located at the mid-point between PNN and PPN. However, in the case of Fig 2 (b), the small vectors POO and ONN have different lengths due to an unbalanced neutral point voltage. In addition, the direction of the medium vector PON moves to downward in the limit of the space vector area.

When the upper capacitor voltage is higher than the lower capacitor voltage, the length of the small vectors POO and PPO affecting upper capacitor voltage are increased because the load voltage, which is connected to the upper capacitor is higher than the balanced state. For the same reason, the length of the small vectors both ONN and OON are decreased due to the lower capacitor voltage. Because the more voltage is applied at the load of the A phase, which is affected by the upper capacitor or voltage, than at the load of the C phase, which is affected by the lower capacitor, the medium vector PNN moves more closely to the A phase. Fig. 3 shows the output load connection state based on the vectors in Sector I.

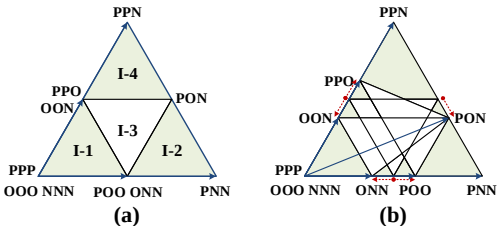

Fig. 2. Vector diagram of Sector I (a) neutral point voltage is balanced (b) neutral point voltage is unbalanced.

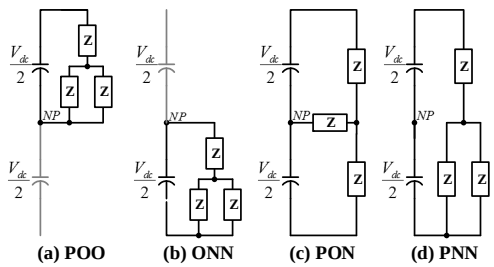

Fig. 3. The load connection state by the vectors in Sector I.

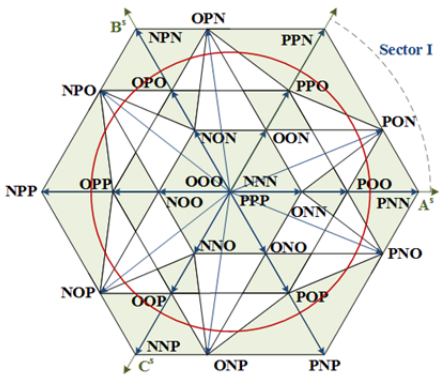

Fig. 4. Distorted space vector diagram of the 3-level NPC inverter due to unbalanced neutral point voltage.

Fig. 4 shows space vector diagram of a NPC inverter this is distorted due to the unbalanced neutral point voltage. In the case of Fig. 4, the medium vectors are concentrated at the point of each phase such as A^s, B^s and C^s. Therefore, when the NPC inverter is operated with the conventional switching method, there can be current distortion concentrated at the point of each phase.

III. Proposed Compensation Method

A. Compensation by adjusting the carrier waveforms

Fig. 5 shows the switching sequences with the conventional and proposed PWM methods in Sector I-1, assuming that the upper capacitor voltage is larger than the lower side. When the 3-level NPC inverter is operated with the conventional PWM method, the injection time of POO, which is used on the upper capacitor, is equal to the time of both ONN and OON, which is used on the lower capacitor. Therefore, the conventional PWM method cannot control the compensation of distorting voltage vectors with an unbalanced neutral point voltage.

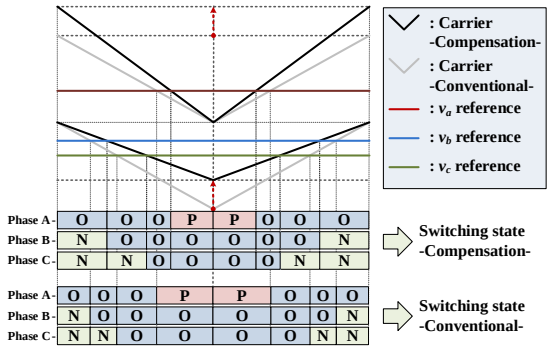

Fig. 5. Switching sequences by conventional and proposed methods based on compare with carrier waveforms in Sector I-1.

In order to compensate the distorted voltage vectors, the injection time of the vectors is inversely modulated, which is proportional to the DC link voltage of each capacitor. This paper proposed, simple compensation method, which is the modulated amplitude of the carrier waveforms by the upper and lower capacitor voltage. The amplitude of the carrier waveforms is calculated by:

$$V_{peak\_Top} = \frac{2V_{C1}}{V_{C1}+V_{C2}}, \quad V_{peak\_Bottom} = \frac{2V_{C2}}{V_{C1}+V_{C2}} \qquad (1)$$

As shown in (1), the compensation values are calculated by dividing half value of the total DC link voltage, and the voltage value of each of the upper and lower capacitors is multiplied. However, a 3-level NPC inverter is operated with this method when the upper capacitor voltage is higher than the lower side. The injection time of POO, which is used by the upper capacitor, is decreased. Thus, the injection time of both ONN and OON used on lower capacitor is increased. In addition, if this method is continuously used, the unbalancing situation of the neutral point voltage can occur because the usage rate of the upper capacitor is continuously increasing, and the usage rate of the lower capacitor is continuously decreasing.

Fig. 6 shows a compensation method to improve distorted space vectors by adjusting the amplitude of carrier waveforms in proportion to each DC link voltage. However, in the case of Fig. 6, the duty ratio of the bottom carrier is increased due to the reduced amplitude of the bottom carrier waveform. In addition, the duty ratio of the top carrier is decreased due to the increased amplitude of the top carrier waveform. As a result, the discharging rate of the lower capacitor is continuously decreased and that of the upper capacitor is continuously increased. If the NPC inverter is controlled with this method only, the neutral point voltage is still unbalanced, and the effect is more worse than the case using the conventional method. Furthermore, if the carrier waveforms are smaller than the 3-phase reference voltage, the over modulation effect can be occur because each carrier must be proportional to each capacitor voltage. Therefore, another technique for compensating the distorted space vectors of NPC inverters is needed for use on the proposed method for improving the effects of an unbalanced neutral point voltage.

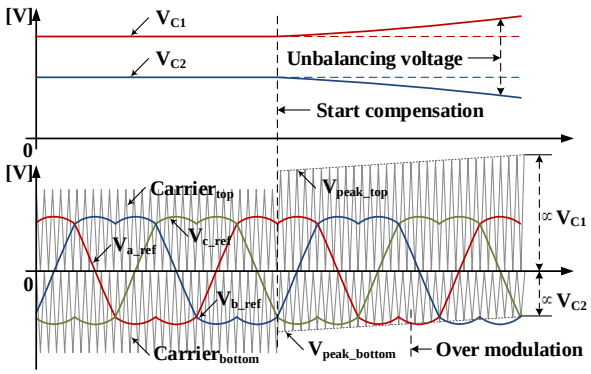

Fig. 6. Compensation method by adjusting the amplitude of both top and bottom carrier waveforms.

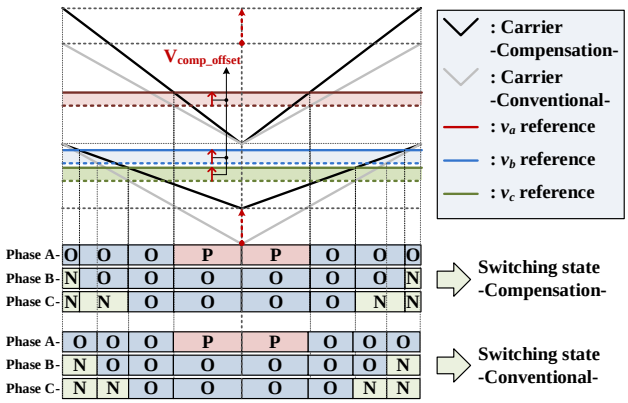

Fig. 7. Switching sequences by conventional and proposed additional methods based on compare with carrier in Sector I-1.

B. Compensation by both adjusting the carrier waveforms and injection of DC offset voltage

In order to improve the problem of the voltage usage rate, this paper proposed an additional method with DC offset. Fig. 7 shows the vector sequence by injecting the DC offset at the 3-phase reference, which has an equal utilization rate on both sides of the capacitor. The DC offset voltage injection method does not effect the AC phase voltage or current in 3-phase applications. In addition, it can compensate the effect of an increasing neutral point voltage difference through equal utilization rate on both side capacitors. The offset voltage is calculated for an equal amount of time of for maintaining the small vector, which is what each capacitors uses.

Fig. 8 shows an additional proposed method with the several periods of reference voltage that have modulated amplitudes of the carriers and an injected DC offset. The offset voltage is calculated by adding the ratio of the peak value of the reference voltage and the amplitude of the top carrier waveform. The offset is equal to the ratio of the minimum directive voltage calculated by subtracting the offset from the amplitude of the bottom carrier. The proportional expression of the offset voltage is calculated as (2).

$$\begin{aligned} V_{peak\_Top} &: V_{peak\_ref} + V_{comp\_offset} \\ = V_{peak\_Bottom} &: V_{peak\_ref} - V_{comp\_offset} \end{aligned} \qquad (2)$$

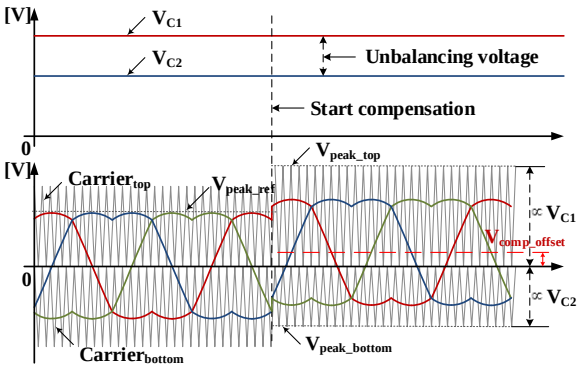

Fig. 8. Compensation method by both adjusted both the amplitude of the carrier and offset voltage.

In a proportional expression, the offset voltage for the balance voltage usage ratio can be calculated by (3).

$$V_{comp\_offset} = \frac{\sqrt{3}MI(V_{C1} - V_{C2})}{2(V_{C1} + V_{C2})} \quad (3)$$

The offset voltage is calculated by using (1) and (2). *MI* is the modulation index of the space vector pulse width modulation(SVPWM) which is the maximum value of the fundamental wave of the directive voltage.

C. Compensation by adjusting the reference and injection injecting the DC offset voltage

In the experiment, the switching frequency is varied according to the peak value of each carrier waveform, because the MCU is operated by the PWM module based on a timer counter. Thus, for purposes of this experiment, the proposed method must individually change the reference voltage to compare each carrier waveform with the method that adjusts the carrier waveform. Therefore, this paper proposes a method to compensate distorted space vectors by varying the modulation index of the reference voltage compared with varying the carrier waveforms as shown in Fig. 9. The voltage usage rate is varied by changing the modulation index of the reference voltage, and then applying the offset voltage to make the two voltage usages identical. The compensation values for each of the reference voltages by the voltage of the upper and lower capacitor are calculated with the following equation.

$$V_{comp\_Top} = \frac{V_{C1} + V_{C2}}{2V_{C1}}, \quad V_{comp\_Bottom} = \frac{V_{C1} + V_{C2}}{2V_{C2}} \quad (4)$$

Equation (4) is related to (1) where the reference voltage of the top carrier is multiplied by V_{comp_Top}, and the reference voltage of the bottom carrier is multiplied by V_{comp_Bottom}.

Thus, the reference voltages to compute the upper and lower reference voltages are calculated by (5).

$$V_{abc\_ref\_comp1} = (V_{abc\_ref} + V_{comp\_offset})V_{comp\_Top}$$
$$V_{abc\_ref\_comp2} = (V_{abc\_ref} + V_{comp\_offset})V_{comp\_Bottom} \quad (5)$$

Fig. 10 is a control block diagram of the proposed compensation method, which applies both the modulation index (MI) of the reference voltage and the offset voltage with the balance control method of the neutral point voltage. The DC offset voltage of the control block diagram is composed of the offset voltage injection to balance the voltage usage ratio and the balancing control method by applying the same voltage.

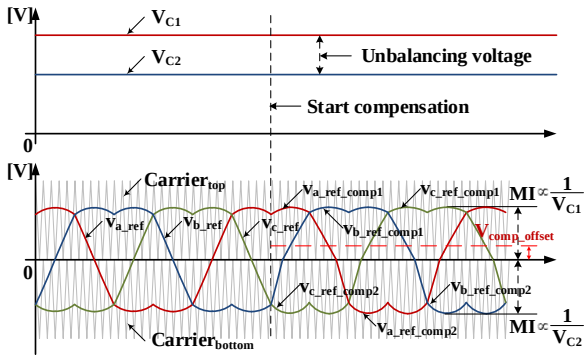

Fig. 9. Compensation method that involves adjusting the modulation index and the offset voltage of the reference voltage.

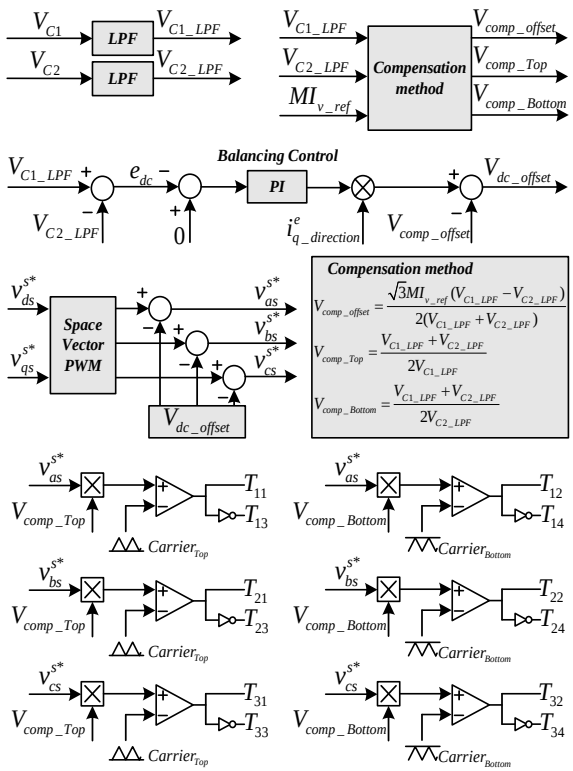

Fig. 10. Control block diagram of unbalanced voltage compensation method according to the MI compensation of the reference voltage and injecting the offset voltage.

In addition, the reference voltages are configured to multiply different compensation values with each of the related carrier waveforms of the upper and lower sides. Except for the ripple voltage of the DC link capacitors, all of the DC link voltages of V_{C1} and V_{C2} pass through a digital LPF for control unbalancing. In addition, the balancing control of the neutral point voltage generally uses the offset injection method by a PI controller as shown in Fig. 10 [9], [14].

TABLE I
SIMULATION PARAMETERS OF NPC

Parameter	Value
DC link capacitor	6[mF]
DC link voltage	500[V]
Switching frequency	5[kHz]
Load resistance	12[Ω]
Load inductance	3[mH]
Top capacitor load	17.5[Ω]
Bottom capacitor load	7.5[Ω]

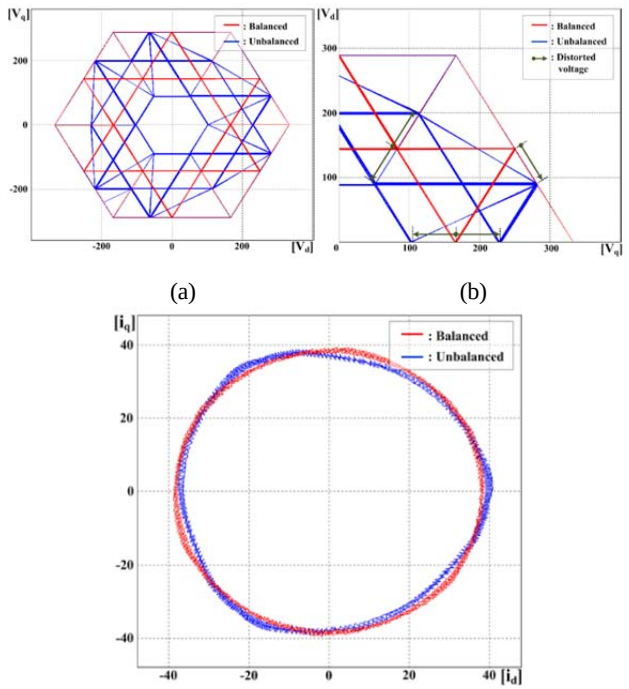

Fig. 11. Simulation results of distorted space vector and current by the unbalanced neutral point voltage.

IV. SIMULATION RESULTS

The simulation parameters are shown in Table I. An unbalanced voltage state is generated by connecting different resistances to the upper and lower capacitors in the simulation and simulation parameter shown in Table I.

Fig. 11 shows the simulation results of the output voltage vector in cases of both balanced and unbalanced DC link conditions. The x and y axis of the planar graph correspond to the output voltage vector and output phase current of the D and Q axis of the DQ Clarke transformation. Fig. 11(a) shows that the small vectors in the same direction are divided into two identical lengths, and that the medium vectors in each sector are concentrated on the A, B and C phases at the unbalanced DC link voltage. Fig. 11(b) shows a magnified Sector I of Fig. 11(a). This figure describes the distortion in the unbalanced neutral point voltage. For this reason, as shown in Fig. 11(c),

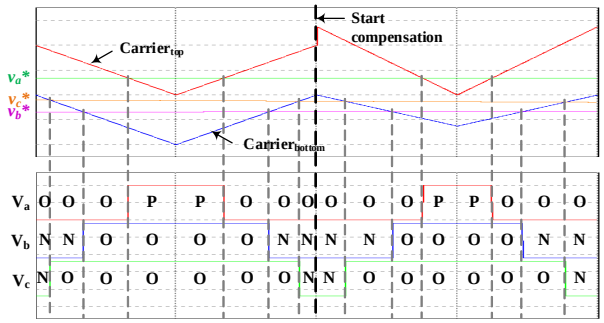

Fig. 12. Simulation results of conventional and proposed voltage vector switching sequence for modulating carrier waveforms.

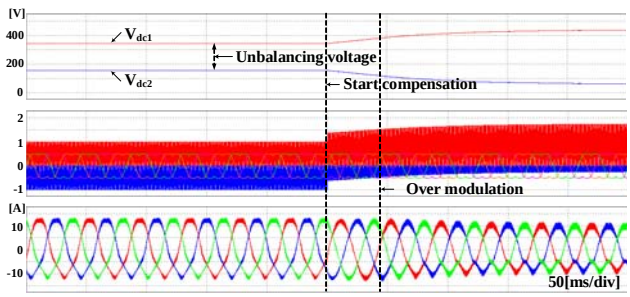

Fig. 13. Simulation results of adjusting amplitude of the carrier waveforms at the unbalanced neutral point voltage.

the maximum output current increases in the direction of the A, B and C phases, where the medium vectors are concentrated. On the other hand, the minimum current decreases in the direction where the vectors are not concentrated. In addition, when the neutral point voltage is unbalance, the interval of the current ripple is gradually narrow in the direction where the vectors are concentrated, and the current ripple is wide in the direction where the vectors are not concentrated.

Fig. 12 shows the simulation of the switching signal and vector sequence for compensating distorted voltage vectors by modulating the amplitude of the carrier waveforms. The vector injection time is inversely proportional to the distorted small vectors. Accordingly, the small vector using the upper capacitor (POO) is decreased, and the small vectors using the lower capacitor (ONN and ONO) are increased. However, if the proposed compensation method is used, the unbalance of the neutral point voltage occurs because the utilization rate of the upper capacitor is continuously increasing but the utilization rate of the lower capacitor is continuously decreasing, as shown in Fig. 12.

Fig. 13 shows the simulation of the unbalanced voltage compensation method by modulating the amplitude of each carrier waveform. If the offset voltage is not applied as shown on Fig. 13, the neutral voltage unbalance gets larger as mentioned in Fig. 6. The output current is compensated even though the neutral voltage difference is large in the initial stage of the compensation. However, the output current distortion by over modulation occurs after the bottom carrier is less than the directive voltage.

Fig. 14 shows the simulation of the switching signal and

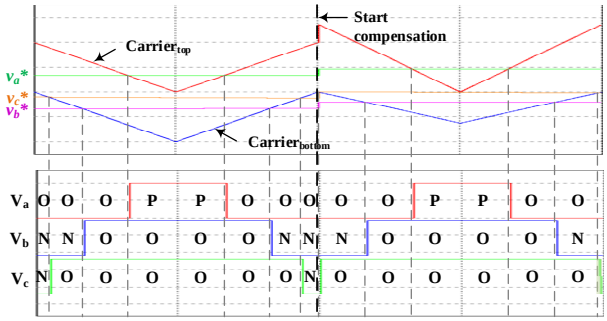

Fig. 14. Simulation results of conventional and proposed voltage vector switching sequence for modulating both amplitude of carrier and inject DC offset.

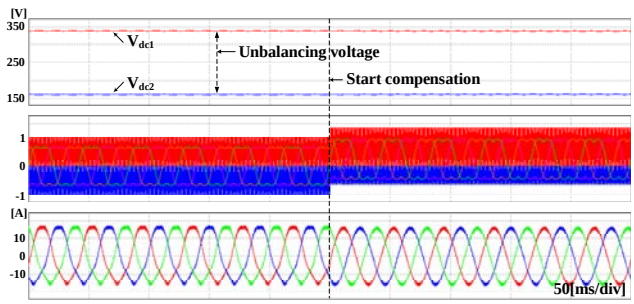

Fig. 15. Simulation results of adjusting the amplitude of the carrier waveforms and the offset of reference voltage at the unbalanced neutral point voltage.

vector sequence of the compensation method for distorted volt age vectors by modulating the amplitude of carrier waveforms and an injected DC offset. In addition, the injection time of POO is equal to the injection time of adding both ONO and ONN. The proposed method is only modulated by ONO and ONN. Therefore, the proposed method can compensate distorted voltage vector by an unbalanced DC link and the problem of a difference voltage usage range in each capacitor.

Fig. 15 shows the simulation results of the proposed compensation method according to the adjustment of the amplitude of each carrier waveform and an injected offset voltage in order to improve the voltage usage rate difference. The output currents are compensated even though the difference between voltages of the DC link is 40% of the total DC link voltage. The voltage difference is not affected after the compensation method when the amplitude of the carrier waveforms are adjusted and the offset is injected into the reference at the same time, as shown in Fig. 15.

Fig. 16 shows the simulation of the proposed compensation method by adjusting the modulation index of each reference voltage and an injected offset voltage in order to improve the voltage usage rate difference. Even though the carrier waveform has a constant value, the output currents are compensated when the modulation index of the reference voltage is adjusted and the offset is injected into the reference at the same time, as shown in Fig. 11.

Fig. 17 show the neutral point voltage balancing control

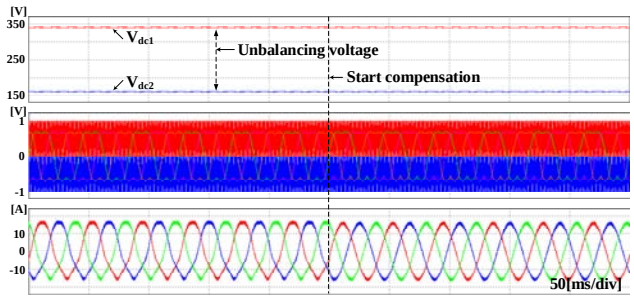

Fig. 16. Simulation results of adjusting MI and the offset of the reference voltage at the unbalanced neutral point voltage.

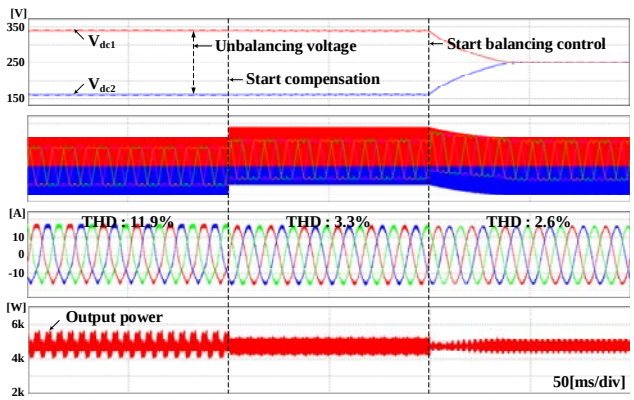

Fig. 17. Simulation results of modulating the amplitude of the carrier waveforms and offsetting the reference voltage at the balancing control of neutral point voltage.

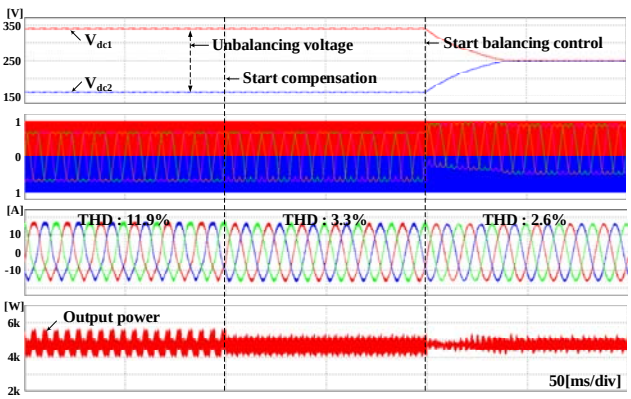

Fig. 18. Simulation results of the modulating MI and injecting the offset of the reference voltage at the balancing control of the neutral point voltage.

simulation according to the carrier magnitude modulation and applying the offset voltage. For the balancing control of the neutral point voltage, a PI controller for applying the DC offset voltage is used as shown on Fig. 10. As shown in Fig. 17, in case of the steady state of the unbalanced neutral point voltage, the THD of the phase current is 11.9% before the compensation, and 3.3% after the compensation. In addition, Fig. 17 shows the compensated power ringing according to the proposed method.

Fig. 18 shows the simulation result of the neutral point voltage balancing control according to the modulation index

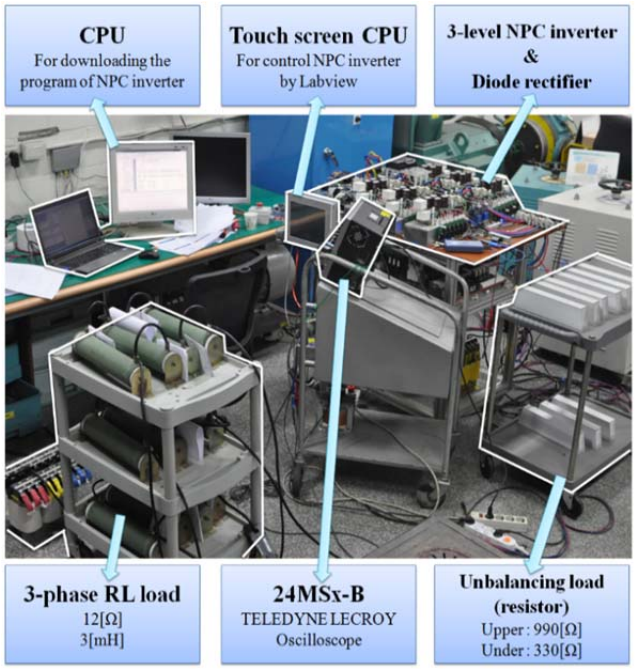

Fig. 19. Experimental setup.

TABLE II
EXPERIMENTAL PARAMETERS OF NPC

Parameter	Value
DC link capacitor	6[mF]
DC link voltage	500[V]
Switching frequency	10[kHz]
Load resistance	12[Ω]
Load inductance	3[mH]
Top capacitor load	900[Ω]
Bottom capacitor load	330[Ω]

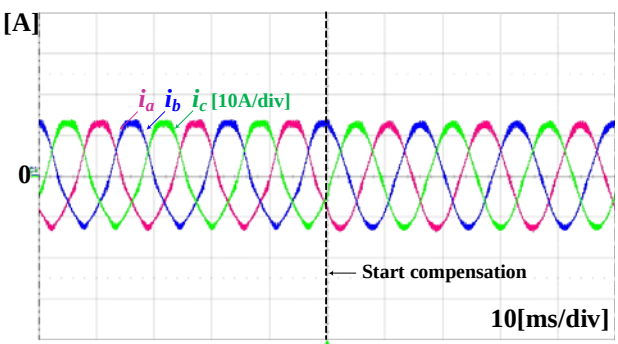

Fig. 20. The phase current waveforms by proposed method.

compensation of the reference voltage and applying the offset voltage. In case of Fig. 18, the THD of the phase current is 11.9% before the compensation, and 3.3% after the compensation in the steady state of the unbalanced neutral point voltage.

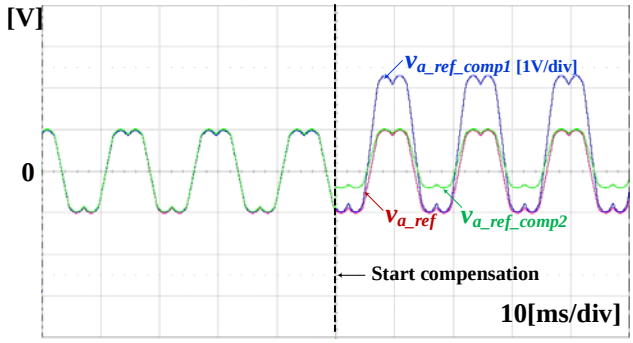

Fig. 21. Experimental results of the reference voltage waveforms.

V. EXPERIMENTAL RESULTS

Fig. 19 shows the experimental setup. An RL load is used and the metal clad resistor with a three to one ratio is connected to each DC link. Through the slidac and diode rectifier, 500[V] is rectified in a way similar to the simulation, and the three-level NPC inverter is controlled by a TMS320C28346. In the experiment, the WT3000 made by YOKOGAWA is used to measure the THD of the phase currents. An unbalanced voltage state is generated by connecting different values of the resistors to the upper and lower capacitors. The other experimental parameters are as shown in Table 2.

Fig. 20 shows the experimental results of the phase current waveforms that apply the compensation method. As shown on the figure, the distortion of the phase currents is compensated after the adaptation of the proposed compensation method. The compensation method uses adjusting the modulation index of the reference voltage and injecting the offset voltage.

Fig. 21 shows the waveforms of the reference voltage to compensate the distorted space vector by adjusting the MI and injecting the DC offset voltage. These waveforms are generated by a Digital/Analog converter module with a control board. The green and blue waveforms are the reference voltages, which are calculated by both $V_{a\_ref\_comp2}$ and $V_{a\_ref\_comp1}$ in eq. (5). The red waveform is the conventional reference voltage. As shown in the figure, the blue waveform has the maximum reference voltage at the same amplitude as the maximum reference voltage prior to the compensation. However, the modulation index is smaller in comparison to the general waveforms. The green waveform has the minimum reference voltage at the same amplitude as the minimum reference voltage prior to the compensation, while the modulation index is greater than the general waveforms. Thus, it is found that the DC link voltage does not vary even when the compensation method is applied.

Fig. 22 shows the experimental waveforms of the voltage of the upper and lower capacitor and current of the A phase when the voltage of the upper capacitor is 350[V] and the voltage of the lower capacitor is 150[V]. In the experimental results, the phase current is changed to sinusoidal waveforms by the

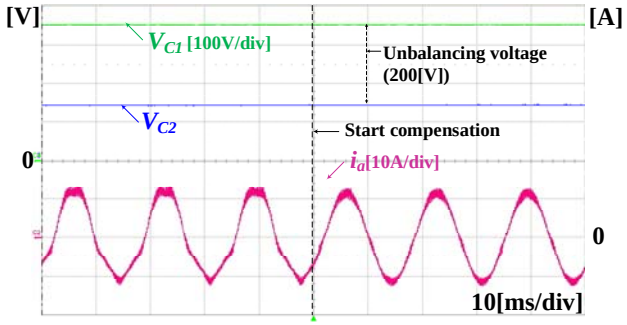

Fig. 22. Each DC link voltage and phase current by proposed method.

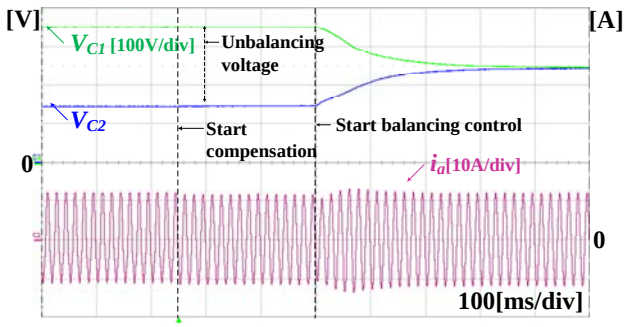

Fig. 23. The voltage of upper and lower capacitor and phase current at operating both proposed compensation method and balancing control.

proposed compensation method. This method is not effected by the neutral point voltage when the neutral point voltage has the situation of a critical unbalanced that is the same as the simulation waveforms.

Fig. 23 shows the experimental waveforms of the proposed compensation method combined with the neutral point voltage balancing control method. From Fig. 23, the phase current has a THD of 11.2% in the conventional PWM method at an unbalanced neutral point voltage. When the proposed PWM method is operated at an unbalanced neutral point voltage, the phase current THD can be reduced to 5.6%. Even though it uses the proposed method, the neutral point voltage does not have an effect on the experimental results. In addition, the phase current THD is 3.8% about the balancing control by the offset voltage injection method.

V. Conclusion

This paper proposes a compensation method to improve the distorted space vectors when a 3-level Neutral Point Clamped (NPC) inverter has an unbalanced neutral point voltage. The phase current has been improved by adjusting the amplitude of the carrier and injecting the DC offset voltage at the 3-phase reference voltage. Furthermore, the THD of the phase current is 3.3% in the simulation results when the upper capacitor voltage is 350[V] and the lower capacitor voltage is 150[V]. In the case of the experimental results, the THD of the phase current is measured 5.6% when the upper capacitor voltage is 350[V] and the lower capacitor voltage is 150[V].

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Seung-Wook Hyun received his B.S. degree in Electrical Engineering from Anyang University, Anyang, Korea, in 2012; and the his M.S. degree in Energy System Engineering from Sunkyunkwan University, Suwon, Korea, in 2014. He is presently working towardshis Ph.D. degree in the College of Electronic, Electrical and Computer Engineering, Sunky- unkwan University. His current research interests include power converters, dc-ac inverters, and 3-level PWM inverters.

Seok-Jin Hong received his B.S. degree in Automatic System Engineering from Dongyang Mirea University, Seoul, Korea, in 2012; and his M.S. degree in the Process of Mechatronics Cooperation from Sungkyun-kwan University, Suwon, Korea, in 2014. He is presently working towards his Ph.D. degree in College of Information and Communication Engineering, Sungkyunkwan University. His current research interests include power converters, dc-acinverters, motor drives, 3-level PWM inverters, and windpower systems.

Jung-Hyo Lee received his B.S. degree in Electrical Engineering from Konkuk University, Seoul, Korea, in 2006; and the his M.S. and Ph.D. degrees in Electrical Engineering from Sungkyunkwan University, Suwon, Korea, in 2008 and 2013, respectively. Since 2013, he has been a Senior Researcher in the automotive component of the R&D Team at LG Innotek. His current research interests include converters and inverters for motor drive applications.

Chun-Bok Lee received his B.S. degree in Electronic Engineering from Namseoul Univer- sity, Asan, Korea, in 2013; and his M.S. degree in Mechanical System Engineering from Sung- kyunkwan University, Suwon, Korea, in 2015. His current research interests include compensation control of power electronic devices, LVDC systems and multi level inverters.

Chung-Yuen Won was born in Korea, in 1955. He received his B.S. degrees in Electrical Engineering from Sungkyunkwan University, Suwon, Korea, in 1978; and his M.S. and Ph.D. degrees in Electrical Engineering from Seoul National University, Seoul, Korea, in 1980 and 1987, respectively. From 1990 to 1991, he was with the Department of Electrical Engineering, University of Tennessee, Knoxville, TN, USA, as a Visiting Professor. Since 1988, he has been a member of the faculty of Sungkyunkwan University, where he is a Professor in the College of Information and Communication Engineering. He is also the director of the Samsung Energy Power Research Center. He was the President of the Korean Institute of Power Electronics, in 2010. Since 2011, he has been a director of the Korean Federation of Science and Technology Societies. His current research interests include the power electronics of electric machines, electric/hybrid vehicle drives, and power converters for renewable energy systems. He is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE).