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Three-Level SEPIC with Improved Efficiency and Balanced Capacitor Voltages

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Abstract

A single-ended primary-inductor converter (SEPIC) features low input current ripple and output voltage up/down capability. However, the switching devices in a two-level SEPIC suffer from high voltage stresses and switching losses. To cope with this drawback, this study proposes a three-level SEPIC that uses a low voltage-rated switch and thus achieves better switching performance compared with the two-level SEPIC. The three-level SEPIC can reduce switch voltage stresses and switching losses. The converter operation and control method are described in this work. The experimental results for a 500 W prototype converter are also discussed. Experimental results show that unlike the two-level SEPIC, the three-level SEPIC achieves improved power efficiency with balanced capacitor voltages.

Key words: Output capacitor voltage balancing, Switching loss, Three-level single-ended primary-inductor converter (SEPIC), Voltage stress

I. INTRODUCTION

Single-ended primary-inductor converters (SEPICs) have been utilized for various industry applications because of their low input current ripples [1] and output voltage up/down capabilities [2]. Unlike the buck-boost converter [3], the SEPIC features a non-inverted output voltage [4]. It uses a series capacitor to isolate the input from the output [5]. Fig. 1 shows the circuit diagram of the conventional two-level SEPIC [1], [6]. However, the main drawback of the two-level SEPIC is that the switching devices rely on the sum of the input voltage V_i and output voltage V_o [7]. When the output voltage V_o is 400 V, the power switch and output diode should be rated at 1,200 V as V_i may increase to more than 200 V. As the output voltage increases, the switch voltage stress significantly increases. This high voltage stress increases the switching losses and eventually decreases the converter efficiency and reliability.

Three-level converters are widely adopted tools for high voltage applications [8], [9]. These converters use two series-connected capacitors to achieve total dc-link voltage. The power switches are then stressed on half of the total dc-link voltage. Three-level converters can use low voltage-rated switches and thus achieve better switching performance than two-level converters that use switches rated in terms of full blocking voltage. Moreover, the performance of three-level converters, including cost and power efficiency, can be improved in comparison with that of two-level converters. Recently, a three-level isolated SEPIC was explored in [12]. Unfortunately, the isolated-type converter requires two transformers, which increase the manufacturing cost and eventually decrease converter efficiency. However, thus far, three-level non-isolated SEPICs have not been suggested, and their performance has not been reported.

The present work proposes a three-level SEPIC whose circuit diagram is shown in Fig. 2. The three-level SEPIC can reduce switch voltage stresses by half in comparison with the two-level SEPIC. This feature allows the three-level SEPIC to have low voltage-rated switches. The three-level SEPIC improves power efficiency by reducing switching losses. The operation of the three-level SEPIC is described in Section II. The control method for regulating the output voltage and capacitor voltages is presented in Section III. The experimental results for a 500 W prototype converter are discussed in Section IV. The experimental results show that the three-level SEPIC improves power efficiency with balanced capacitor voltages in comparison with the two-level SEPIC. The concluding remarks are given in Section V.

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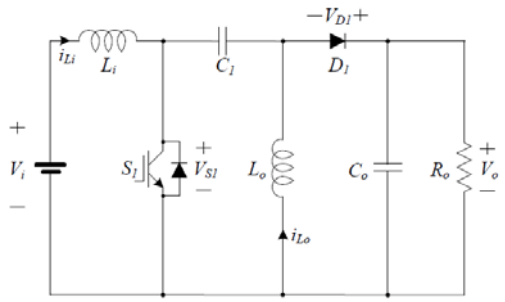


Fig. 1. Circuit diagram of the conventional two-level SEPIC.

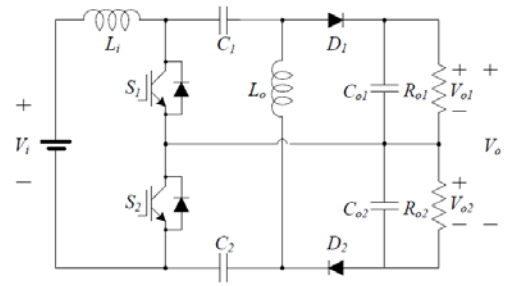


Fig. 2. Circuit diagram of the proposed three-level SEPIC.

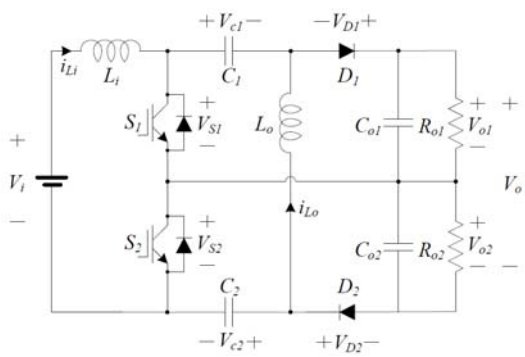
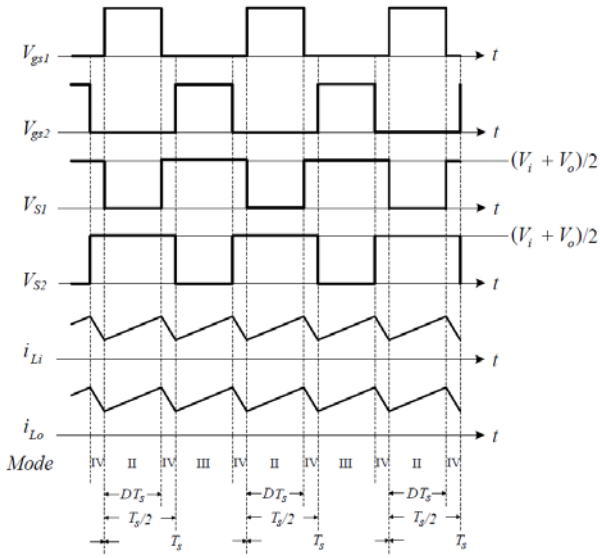


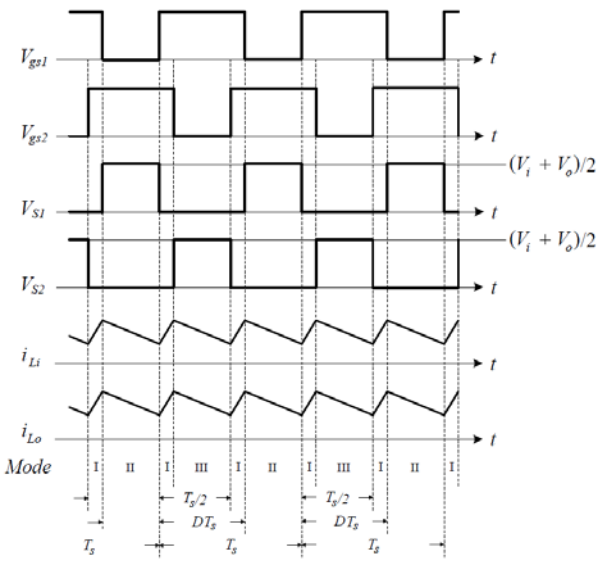
Fig. 3. Circuit diagram of the three-level SEPIC with the reference directions of currents and voltages.

II. THREE-LEVEL SEPIC

Fig. 3 shows the circuit diagram of the three-level SEPIC with the reference directions of currents and voltages. The three-level SEPIC comprises an input inductor L_i, two switches S_1 and S_2, two capacitors C_1 and C_2, an output inductor L_o, two diodes D_1 and D_2, and two output capacitors C_{o1} and C_{o2}. R_{o1} and R_{o2} are the output resistors, whereas S_1 and S_2 are the metal-oxide-semiconductor field-effect transistors (MOSFETs). V_i is an input voltage; V_{c1} and V_{c2} are the voltages of C_1 and C_2, respectively; V_{o1} and V_{o2} are the voltages of C_{o1} and C_{o2}, respectively; V_{S1} and V_{S2} are the voltages across S_1 and S_2, respectively; V_{D1} and V_{D2} are the voltages across D_1 and D_2, respectively; and i_{Li} and i_{Lo} are the currents of L_i and L_o, respectively. The midpoint of the output capacitors is connected to the midpoint of the series-connected switches. C_{o1} and C_{o2} serve as capacitive voltage dividers that split the output voltage V_o into two equal voltages, namely, V_{o1} and V_{o2} (V_{o1} = V_{o2} = V_o/2). V_{c1} and V_{c2} follow the half of the input voltage (V_{c1} = V_{c2} = V_i/2).



(a)



(b)

Fig. 4. Operation waveforms of the three-level SEPIC: (a) D < 0.5 and (b) D > 0.5.

Fig. 4 shows the operation waveforms of the three-level SEPIC. V_{gs1} and V_{gs2} are the gating signals of S_1 and S_2, respectively. D_{S1} and D_{S2} are the duty cycles of S_1 and S_2, respectively. If V_{gs1} and V_{gs2} are identical to a 180° phase difference with respect to one switching period T_s, then the duty cycle is considered as D. When the duty cycle D is less than 0.5, the three-level SEPIC steps down the input voltage, as shown in Fig. 4(a). When the duty cycle D is higher than 0.5, the three-level SEPIC steps up the input voltage, as shown in Fig. 4(b). Fig. 5 shows the circuit diagrams of the three-level SEPIC according to the switches' states. Depending on the switches' state, the three-level SEPIC has the following four operation modes.

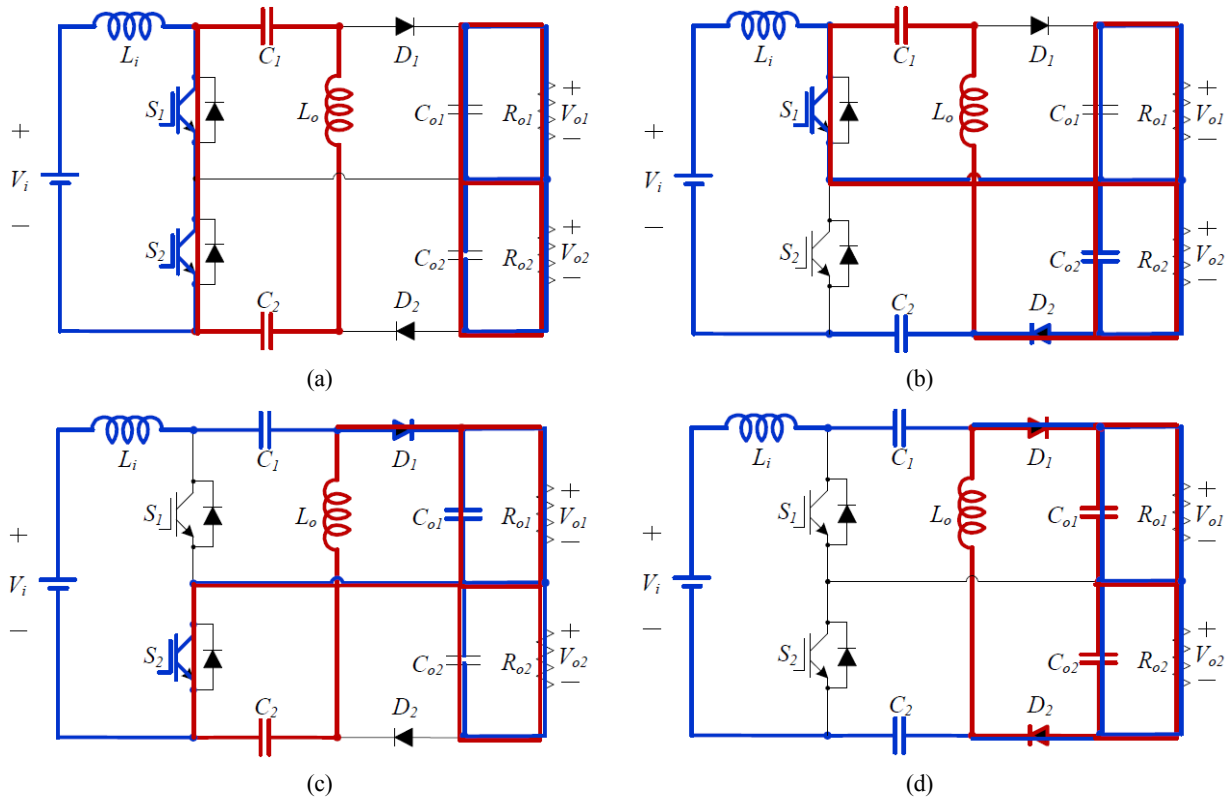


Fig. 5. Circuit diagram of the three-level SEPIC according to the switches' state: (a) *Mode I*, (b) *Mode II*, (c) *Mode III*, and (d) *Mode IV*.

Mode I: The three-level SEPIC is in *Mode I* only when $D > 0.5$. When S_1 and S_2 are turned on, D_1 and D_2 are turned off. On the one hand, the input inductor L_i stores energy from the input voltage V_i. The input inductor current i_{Li} flows through L_i, S_1, and S_2 at a rate of $di_{Li}/dt = V_i/L_i$. On the other hand, the output inductor current i_{Lo} charges the capacitors C_1 and C_2. The output inductor current i_{Lo} flows through C_1, S_1, S_2, and C_2 at the rate of $di_{Lo}/dt = V_i/L_o$.

Mode II: S_1 is turned on while S_2 is turned off. D_1 is turned off while D_2 is turned on. On the one hand, the input inductor current i_{Li} charges the capacitors C_2 and C_{o2}. The input inductor current i_{Li} flows through L_i, S_1, C_{o1}, D_2, and C_2 at the rate of $di_{Li}/dt = (V_i - V_o)/2L_i$. On the other hand, the output inductor current i_{Lo} charges the capacitors C_1 and C_{o2}. The output inductor current i_{Lo} flows through C_1, S_1, C_2, and D_2 at the rate of $di_{Lo}/dt = (V_i - V_o)/2L_o$.

Mode III: S_1 is turned off while S_2 is turned on. D_1 is turned on while D_2 is turned off. On the one hand, the input inductor current i_{Li} charges the capacitors C_1 and C_{o1}. The input inductor current i_{Li} flows through L_i, C_1, D_1, and C_{o1} at the rate of $di_{Li}/dt = (V_i - V_o)/2L_i$. On the other hand, the output inductor current i_{Lo} charges the capacitors C_2 and C_{o1}. The output inductor current i_{Lo} flows through D_1, C_{o1}, S_2, and C_2 at the rate of $di_{Lo}/dt = (V_i - V_o)/2L_o$.

Mode IV: The three-level SEPIC is in *Mode IV* only when $D < 0.5$. When S_1 and S_2 are turned off, D_1 and D_2 are turned on. On the one hand, the input inductor L_i releases its stored energy to the output capacitors C_{o1} and C_{o2}, thus discharging the capacitors C_1 and C_2. The input inductor current i_{Li} flows through L_i, C_1, D_1, C_{o1}, C_{o2}, D_2, and C_2 at the rate of $di_{Li}/dt = -V_o/L_i$. On the other hand, the output inductor current i_{Lo} flows through D_1, C_{o1}, C_{o2}, and D_2 at the rate of $di_{Lo}/dt = -V_o/L_o$.

When S_1 and D_2 are turned off, they are stressed on the sum of V_{c1} and V_{o1}. When S_2 and D_1 are turned off, they are stressed on the sum of V_{c2} and V_{o2}. With the assumption that $V_{c1} = V_{c2} = V_i/2$ and $V_{o1} = V_{o2} = V_o/2$, the switch voltage stress is $(V_i + V_o)/2$. The switch voltage stress in the three-level SEPIC is reduced by half compared with the switch voltage stress in the two-level SEPIC. This condition allows the three-level SEPIC to have low voltage-rated switches and reduce switching losses.

III. Simulation Verification

The capacitor voltages should be balanced as $V_{c1} = V_{c2} = V_i/2$ and $V_{o1} = V_{o2} = V_o/2$. In practice, capacitor voltages may be different because of mismatched capacitances and equivalent series resistance [10]. If not balanced, one capacitor voltage may be greater than the breakdown voltage of the power switch; this difference causes severe damage to the power switch [11]. Thus, capacitor voltage balance control is necessary for the three-level SEPIC.

Fig. 6 the control scheme of the three-level SEPIC. Fig. 6(a) shows the control block diagram for regulating the output

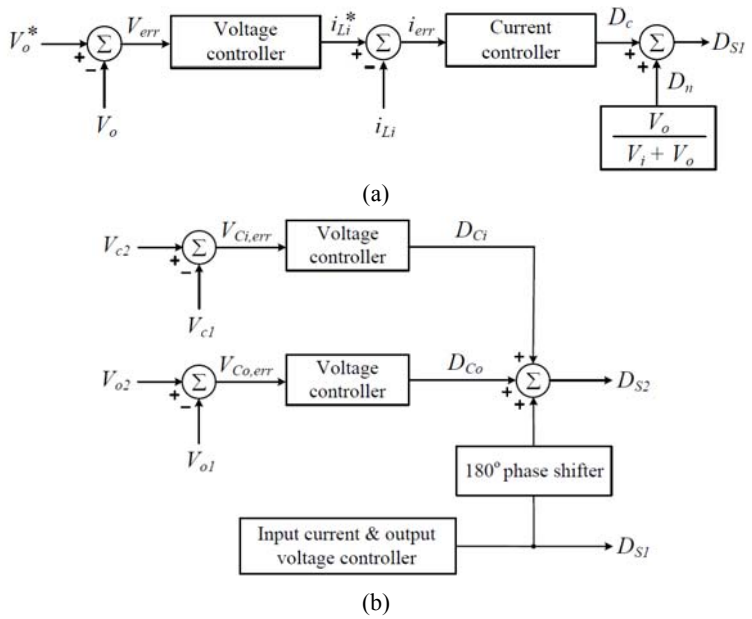


Fig. 6. Control scheme of the three-level SEPIC: (a) control block diagram for regulating the input current and output voltage and (b) control block diagram for balancing the capacitor voltages.

voltage. To obtain the relation between the control variables and duty cycle D, *Mode I* and *Mode II* are considered for a half switching period $T_s/2$. When S_1 and S_2 are turned on during *Mode I*, the input inductor current i_{Li} increases. The following voltage equation is obtained as

$$V_i - L_i \frac{di_{Li}}{dt} = 0 . \quad (1)$$

When S_1 is turned on and S_2 is turned off during *Mode II*, the input inductor current i_{Li} decreases. The following voltage equation is obtained as

$$\left(\frac{V_i - V_o}{2}\right) - L_i \frac{di_{Li}}{dt} = 0 . \quad (2)$$

Depending on the duty cycle D, the average inductor voltage for $T_s/2$ yields the input inductor current variation $\triangle i_{Li}$ as

$$V_i\left(DT_s - \frac{T_s}{2}\right) + \left(\frac{V_i - V_o}{2}\right)\left(T_s - DT_s\right) = L_i \Delta i_{Li} . \quad (3)$$

By rearranging (3),

$$\left(\frac{V_i + V_o}{2}\right) D = \frac{V_o}{2} + \frac{L_i \Delta i_{Li}}{T_s} . \quad (4)$$

Here, the duty cycle D is represented as

$$D = D_n + D_c , \quad (5)$$

where the nominal duty cycle D_n and controlled duty cycle D_c are represented as

$$D_n = \frac{V_o}{V_i + V_o} , \quad (6)$$

$$D_c = \frac{2L_i \Delta i_{Li}}{(V_i + V_o) T_s} . \quad (7)$$

To regulate the output voltage V_o to track its voltage reference V_o^*, a proportional-integral (PI)-type voltage controller is used for the controlled duty cycle D_c, which is given by

$$D_c = k_p V_{o,err} + k_i \int V_{o,err} dt , \quad (8)$$

$$V_{o,err} = V_o^* - V_o . \quad (9)$$

The voltage error $V_{o,err}$ is obtained by comparing the voltage reference V_o^* with the measured output voltage V_o. k_p and k_i are the proportional and integral control gains of the controller, respectively.

Fig. 6(b) shows the control block diagram for balancing the capacitor voltages. On the one hand, the duty cycle D_{S1} is determined by the voltage controller. On the other hand, the duty cycle D_{S2} is determined by adding the duty cycles D_{Ci} and D_{Co} to the duty cycle D_{S1}, whose phase is shifted by 180°. The duty cycle D_{Ci} is

$$D_{Ci} = k_p V_{Ci,err} + k_i \int V_{Ci,err} dt , \quad (10)$$

$$V_{Ci,err} = V_{c2} - V_{c1} , \quad (11)$$

where k_p and k_i are the proportional and integral gains of the controller, respectively. $V_{Ci,err}$ is the voltage error between V_{c2} and V_{c1}. The duty cycle D_{Co} is

$$D_{Co} = k_p V_{Co,err} + k_i \int V_{Co,err} dt , \quad (12)$$

$$V_{Co,err} = V_{o2} - V_{o1} , \quad (13)$$

where k_p and k_i are the proportional and integral gains of the controller, respectively. $V_{Co,err}$ is the voltage error between V_{o2} and V_{o1}. With the suggested capacitor voltage balancing control, the capacitor voltages can be balanced. As the duty cycle D_{S2} is different from D_{S1}, the load currents flowing through R_{o1} and R_{o2} are slightly different while the capacitor voltages are balanced.

TABLE I
ELECTRICAL SPECIFICATION OF THE PROTOTYPE CONVERTER

Electrical specification	Value
Input voltage V_i	200 V
Output voltage V_o	100 V ~ 400 V
Switching frequency f_s	50 kHz

TABLE II
MAIN COMPONENT PARAMETERS OF THE CONVERTERS

Two-level SEPIC	
Component	**Parameter**
Input inductor L_i	1 mH
Capacitor C_1	10 μF
Output inductor L_o	1 mH
Output capacitor C_o	680 μF
Switch S_1	11N80C3 (800 V / 11A)
Diode D_1	RHRP15120 (1200 V / 15 A)
Three-level SEPIC	
Component	**Parameter**
Input inductor L_i	1 mH
Capacitor C_1, C_2	10 μF
Output inductor L_o	1 mH
Output capacitor C_{o1}, C_{o2}	680 μF
Switch S_1, S_2	FQA24N50 (500 V / 24A)
Diode D_1, D_2	FES8JT (600 V / 8 A)

IV. EXPERIMENTAL RESULTS

To evaluate the performance of the three-level SEPIC, a 500 W prototype converter is built and tested. Table I shows the electrical specification of the prototype converter. A two-level SEPIC is also designed for purposes of comparison. Table II shows the main component parameters of the two converters. On the one hand, to select the inductances of L_i and L_o, the inductor ripple current is considered. The inductance is generally proportional to the voltage induced across each inductor. In addition, the duty cycle should be considered with the inductor ripple current. As the inductor ripple current increases, the minimum inductance may decrease with respect to the duty cycle for the voltage across the inductor. On the other hand, to select the capacitances of C_1, C_2, C_{o1}, and C_{o2}, the capacitors are primarily designed to reduce capacitor voltage ripples. As the capacitor voltage ripples decrease, the capacitances of the capacitor should increase. The film capacitors, as non-polarized capacitors, may be used for C_1 and C_2 because they follow half of the input voltage. By contrast, the electrolytic capacitors, as polarized capacitors, may be used for C_{o1} and C_{o2} because they supply electric power to the output load, thereby serving as a capacitive voltage divider that splits the output voltage into two equal voltages V_{o1} and V_{o1}.

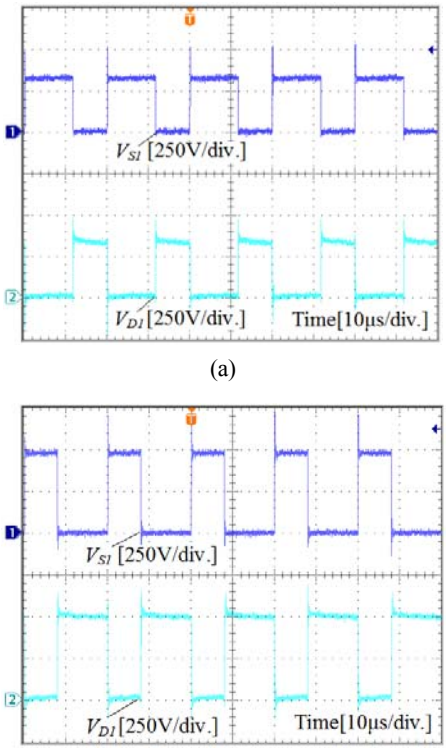
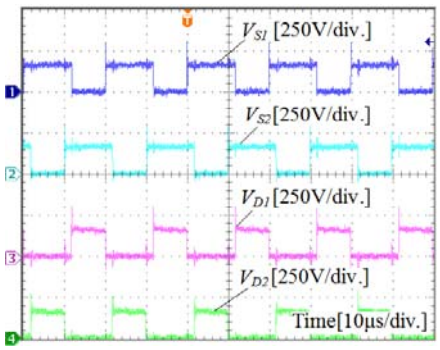
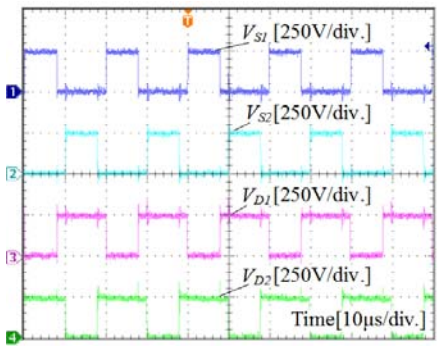


Fig. 7. Experimental waveforms of the two-level SEPIC. (a) Switch voltage V_{S1} and the diode voltages V_{D1} for D = 0.41. (b) Switch voltage V_{S1} and the diode voltages V_{D1} for D = 0.60.

Fig. 7 shows the experimental waveforms of the two-level SEPIC for a 500 W output power. The two-level SEPIC uses 11N80C3 (Infineon) for S_1, whose voltage rating is 800 V. It utilizes RHRP15120 (Fairchild) for D_1, whose voltage rating is 1200 V. Fig. 7(a) shows the switch voltage V_{S1} and the diode voltage V_{D1} when the duty cycle D is 0.41 for V_i = 200 V. The balanced resistive load is used. The output voltage V_o is 140 V for $R_{o1} = R_{o2}$ = 39 Ω. The switch voltage stress is theoretically calculated as 340 V. However, the peak switch voltage stress with the voltage spike is measured as 550 V. When the switch is turned off, the output diode cannot be turned off instantly. As a result of the reverse-recovery process of the diode, a large reverse-recovery current is produced. This reverse-recovery current, in turn, produces a voltage spike across the power switch. This type of switching operation is called the hard-switching operation [13]. Fig. 7(b) shows the switch voltage V_{S1} and diode voltage V_{D1} when the duty cycle D is 0.60 for V_i = 200 V. The output voltage V_o is 300 V for $R_{o1} = R_{o2}$ = 180 Ω. The switch voltage stress is theoretically calculated as 500 V. However, Fig. 7(b) shows that the peak



(a)



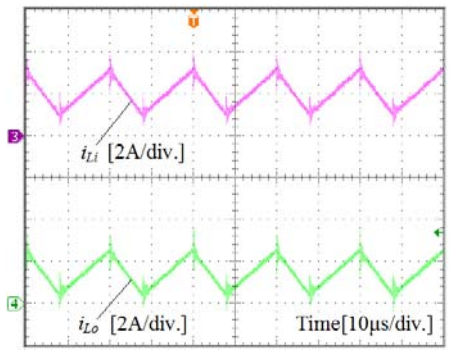
(b)

Fig. 8. Experimental waveforms of the three-level SEPIC: (a) switch voltages V_{S1} and V_{S2} and the diode voltages V_{D1} and V_{D2} for D = 0.41 and (b) switch voltages V_{S1} and V_{S2} and the diode voltages V_{D1} and V_{D2} for D = 0.60.

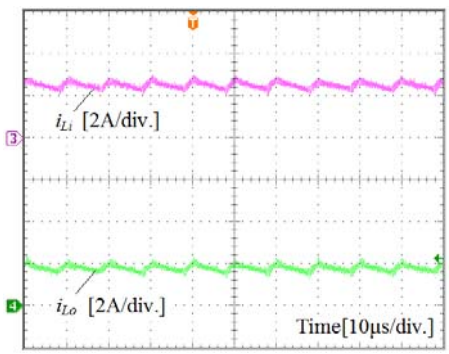
switch voltage stress with the voltage spike is measured as 700 V as a result of the hard-switching operation.

Fig. 8 shows the experimental waveforms of the three-level SEPIC for a 500 W output power. The three-level SEPIC uses FQA24N50 (Fairchild) for S_1 and S_2, whose voltage rating is 500 V. It also employs FES8JT (Vishay) for D_1 and D_2, whose voltage rating is 600 V. Fig. 8(a) the switch voltages V_{S1} and V_{S2} and diode voltages V_{D1} and V_{D2} when the duty cycle D is 0.41 for V_i = 200 V. The output voltage V_o is 140 V for R_{o1} = R_{o2} = 39 Ω. The voltage stress of the switching devices is calculated as 170 V, which is half of the voltage stress of the switching devices in the two-level SEPIC. However, the peak switch voltage stress with the voltage spike is measured as 300 V because of the hard-switching operation. Fig. 8(b) shows the switch voltages V_{S1} and V_{S2} and diode voltages V_{D1} and V_{D2} when the duty cycle D is 0.60 for V_i = 200 V. The output voltage V_o is 300 V for R_{o1} = R_{o2} = 180 Ω. The voltage stress of the switching devices is calculated as 250 V. However, Fig. 8(b) shows that the peak switch voltage stress with the voltage spike is measured as 300 V because of the hard-switching operation.

Fig. 9 shows the experimental waveforms of the two-level SEPIC and three-level SEPIC when V_i is 200 V for D = 0.60 and for a 500 W output power. Fig. 9(a) shows the inductor current waveforms of the two-level SEPIC. The current ripple is observed as 2.0 A. The current ripple frequency is the same

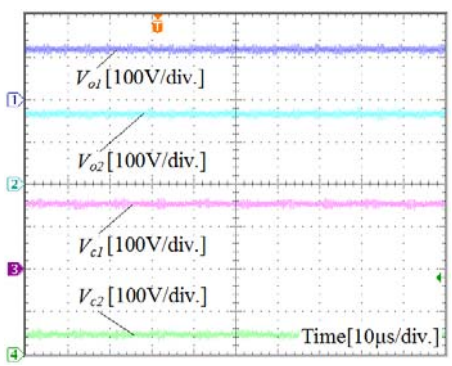


(a)

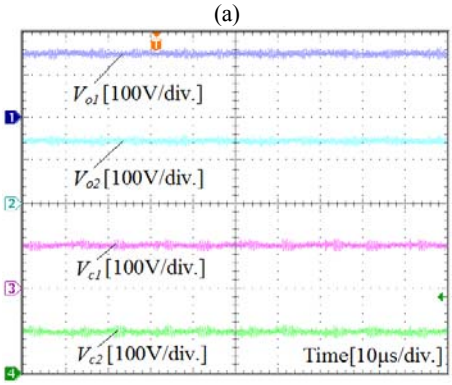


(b)

Fig. 9. Experimental waveforms of the two-level SEPIC and the three-level SEPIC: (a) inductor current waveforms of the two-level SEPIC and (b) inductor current waveforms of the three-level SEPIC.

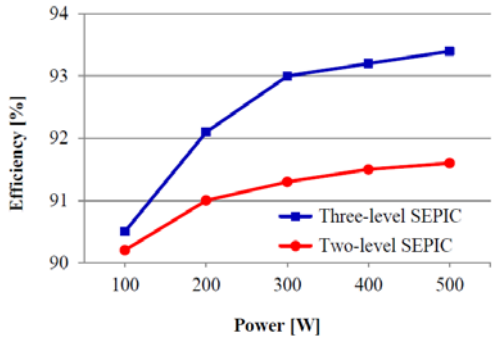


(a)

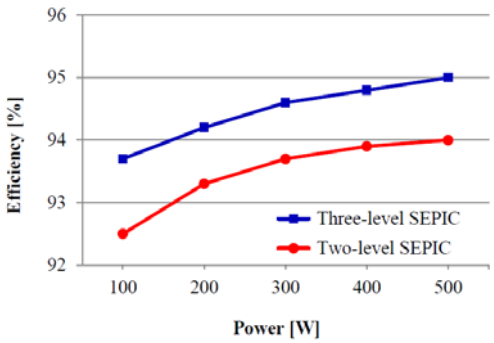


(b)

Fig. 10. Experimental waveforms of the three-level SEPIC: (a) capacitor voltages when the output voltage is regulated as V_o = 300 V without the capacitor voltage balance control and (b) capacitor voltages when the output voltage is regulated as V_o = 300 V with the capacitor voltage balance control.



(a)



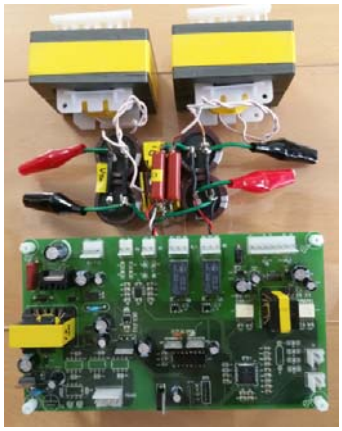
(b)

Fig. 11. Measured power efficiencies of the two-level SEPIC and three-level SEPIC: (a) power efficiencies when the output voltage is 140 V and (b) power efficiencies when the output voltage is 300 V.

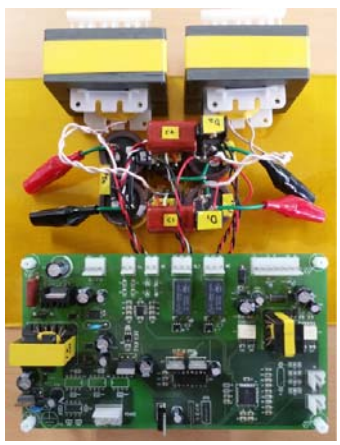
as the switching frequency of 50 kHz. Fig. 9(b) shows the inductor current waveforms of the three-level SEPIC. The current ripple is 1.0 A, which is two times lower than the current ripple of the two-level SEPIC. The current ripple frequency is 100 kHz, which is two times higher than the switching frequency of 50 kHz.

Fig. 10 shows the experimental waveforms of the three-level SEPIC. Fig. 10(a) shows the capacitor voltages when the output voltage is regulated as V_o = 300 V without the capacitor voltage balance control. The three-level SEPIC is operated for V_i = 200 V, R_{o1} = 86 Ω, and R_{o2} = 94 Ω. As the output voltage V_o is regulated as V_o = 300 V, the output capacitor voltages V_{o1} and V_{o2} are unbalanced along with the capacitor voltage V_{c1} and V_{c2} as V_{o1} = 120 V, V_{o2} = 180 V, V_{c1} = 160 V, and V_{c2} = 40 V because the mismatched series-connected output resistances. Fig. 10(b) shows the capacitor voltages when the output voltage is regulated as V_o = 300 V with the capacitor voltage balance control. The three-level SEPIC is operated for V_i = 200 V, R_{o1} = 86 Ω, and R_{o2} = 94 Ω. As the output voltage V_o is regulated as V_o = 300 V, the output capacitor voltages V_{o1} and V_{o2} are balanced as V_{o1} = 150 V and V_{o2} = 150 V. In addition, the capacitor voltages V_{c1} and V_{c2} are balanced as V_{c1} = 100 V and V_{c2} = 100 V by the suggested capacitor voltage control.

Fig. 11 shows the measured power efficiencies of the two-level SEPIC and three-level SEPIC. The power efficiencies are measured for different output power levels



(a)



(b)

Fig. 12. Photographs of the converters: (a) two-level SEPIC and (b) three-level SEPIC.

when the output voltage is controlled as V_o = 140 V and V_o = 300 V for V_i = 200 V. Fig. 11(a) demonstrates the measured power efficiencies when the output voltage is 140 V for a 500 W output power. The two-level SEPIC achieves an efficiency of 91.6%. By contrast, the three-level SEPIC achieves an efficiency of 93.4%. The three-level SEPIC improves its efficiency by 1.8% in comparison with the two-level SEPIC when the output voltage is 140 V from V_i = 200 V. Fig. 11(b) shows the measured power efficiencies when the output voltage is 300 V for a 500 W output power. The two-level SEPIC achieves an efficiency of 95.0%, whereas the three-level SEPIC achieves an efficiency of 94.0%. The three-level SEPIC improves its power efficiency by 1.0% in comparison with the two-level SEPIC when the output voltage is 300 V from V_i = 200 V for a 500 W output power. Figs. 12(a) and (b) show the photographs of the two-level and three-level SEPICs, respectively. The converters are controlled by a single-chip micro-controller, dsPIC30F2020 (Microchip). A voltage divider with an operational amplifier is designed for sensing the capacitor voltages. To generate a phase-shifted pulse width modulation (PWM) signal, a power supply PWM module in dsPIC30F2020 is utilized.

V. CONCLUSION

This study proposes a three-level SEPIC to overcome the drawback of the conventional two-level SEPIC. The three-level SEPIC features low switch voltage stresses as it reduces such stresses by half in comparison with the two-level SEPIC. This feature allows the three-level SEPIC to use low voltage-rated switches and reduce switching losses. The converter operation is described. The converter control for regulating the output voltage with the capacitor voltage balance control is also presented. The experimental results for a 500 W prototype converter are discussed. The experimental results indicate that the three-level SEPIC improves its power efficiency with balanced capacitor voltages in comparison with the two-level SEPIC. The three-level SEPIC improves its efficiency by 1.8% when it steps down the input voltage of 200 V to the output voltage of 140 V for a 500 W output power. The three-level SEPIC also improves its efficiency by 1.0% when it steps up the input voltage of 200 V to the output voltage of 300 V for a 500 W output power. The proposed three-level SEPIC is expected to be utilized in photovoltaic and fuel-cell power generations.

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