JPE 16-2-3

http://dx.doi.org/10.6113/JPE.2016.16.2.425
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

# Dead-Time for Zero-Voltage-Switching in Battery Chargers with the Phase-Shifted Full-Bridge Topology: Comprehensive Theoretical Analysis and Experimental Verification

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**Abstract**

This paper presents a comprehensive theoretical analysis and an accurate calculation method of the dead-time required to achieve zero-voltage-switching (ZVS) in a battery charger with the phase-shifted full-bridge (PSFB) topology. Compared to previous studies, this is the first time that the effects of nonlinear output filter inductance, varied Miller Plateau length, and blocking capacitors have been considered. It has been found that the output filter inductance and the Miller Plateau have a significant influence on the dead-time for ZVS when the load current varies a lot in battery charger applications. In addition, the blocking capacitor, which is widely used to prevent saturation, reduces the circulating current and consequently affects the setting of the dead-time. In consideration of these effects, accurate analytical equations of the dead-time range for ZVS are deduced. Experimental results from a 1.5kW PSFB battery charger prototype shows that, with the proposed analysis, an optimal dead-time can be selected to meet the specific requirements of a system while achieving ZVS over wide load range.

**Key words:** Battery charger, Dead-time, Phase-shifted full-bridge (PSFB), Zero-voltage-switching

## I. INTRODUCTION

The zero-voltage-switching (ZVS) phase-shifted full-bridge (PSFB) converter is the most popular topology in the power range of a few kilowatts (1-5kW) for battery chargers [1]-[3]. Its most attractive features include constant switching frequency operation, high power density, and ZVS turn-on of the primary switches [4]-[9].

Dead-time is a key parameter in the PSFB converter, for both ZVS operation and for system performance. It is well known that the ZVS of PSFB converters is achieved by utilizing the energy stored in the resonant inductance to charge the parasitic capacitors of MOSFETs during the dead-time interval [10], [11]. Meanwhile, the switches are supposed to be turned on before the commutation of the primary current. Thus, there is a minimum and a maximum limitation of the dead-time for ZVS [12]. In addition, a long dead-time may be more reliable. However, along dead-time will make the adjustment range of the duty cycle narrow and reduces the dynamic performance of the converter [13]. Therefore, ZVS cannot be achieved over a wide load range or system performance will be degraded if the dead-time is incorrectly selected.

A lot of research has focused on studying the dead-time for ZVS. In [12]-[14], an adaptive dead-time control scheme for high frequency dual active bridge converters is given. The main influencing factors of dead-time are studied. In [15] and [16], the relationship between resonant inductance and dead-time is analyzed. Equations for calculating the resonant inductance required to achieve ZVS are presented while incorporating the effect of magnetizing current and dead-time. All of these studies are conducive to setting the dead-time and can improve the performances of the PSFB converter to a certain extent.

However, research on the dead-time for ZVS in PSFB is seldom studied comprehensively, especially for battery charger

Manuscript received Apr. 16, 2015; accepted Oct. 11, 2015
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applications with a wide output power range. To be specific, the assumption that the output filter inductance remains constant is no longer valid over a wide load range. Actually, the inductance varies a lot with load changes and the primary current is affected significantly. In addition, the Miller Plateau was rarely considered in previous works, even though it occupies a part of dead-time. More importantly, the length of the Miller Plateau also varies with the output current. Furthermore, a blocking capacitor, which is introduced to prevent the transformer from becoming saturated, would considerably reduce the circulating current and consequentially affect the dead-time. In order to achieve ZVS over a wide power range, the factors mentioned above must be well considered.

Building on the aforementioned works, this paper presents a comprehensive analysis and calculation of the dead-time for ZVS over a wide load range, taking into consideration the effects of the Miller plateau, the nonlinear characteristic of the output filter inductance and the blocking capacitor. This paper is organized as follows. Section II introduces a traditional analysis of dead-time and typical experimental phenomena caused by the above mentioned effects. A comprehensive theoretical analysis and analytical equations of the dead-time are proposed in Section III. In Section IV, detailed experimental results are given to verify the theoretical analysis.

## II. Dead-Time for ZVS in the PSFB Topology

A basic circuit diagram of a PSFB converter is shown in Fig. 1(a). It is formed by four switches $Q_1$-$Q_4$, a power transformer $T_r$, a resonant inductor $L_R$(including the leakage inductor), output rectifier diodes $D_{R1}$ and $D_{R2}$, the output filter inductor $L_f$ and the capacitor $C_f$. $Q_1$ and $Q_2$ are switched on/off before $Q_3$ and $Q_4$. Thus, $Q_1$ and $Q_2$ are known as the "leading leg", while $Q_3$ and $Q_4$ are known as the "lagging leg". The two switches of each leg are driven by complementary PWM signals with a dead-time inserted between them. $V_{in}$ is the input voltage. $V_{pri}$ is the voltage across the primary winding of the transformer $T_r$, and $I_p$ is the current through it. The battery voltage is $V_o$. Since it is easy to achieve ZVS of the leading leg, the dead-time for ZVS of the lagging leg is mainly discussed here.

### *A. Traditional Analysis and Calculation of Dead-Time*

Key waveforms of a PSFB converter are shown in Fig. 1(b). Take the ZVS-on of $Q_3$as an example. $Q_4$ is switched off at $t_4$. Then the ZVS of $Q_3$is achieved by utilizing the energy stored in the resonant inductance $L_R$ to charge the parasitic capacitors of the MOSFETs ($C_{ds3}$ and $C_{ds4}$) during the time period $t_4$-$t_5$. Since $V_{pri}$ is equal to zero, an equivalent circuit during this transition interval is shown in Fig. 2. Therefore, based on Fig. 2, the following equations can be obtained

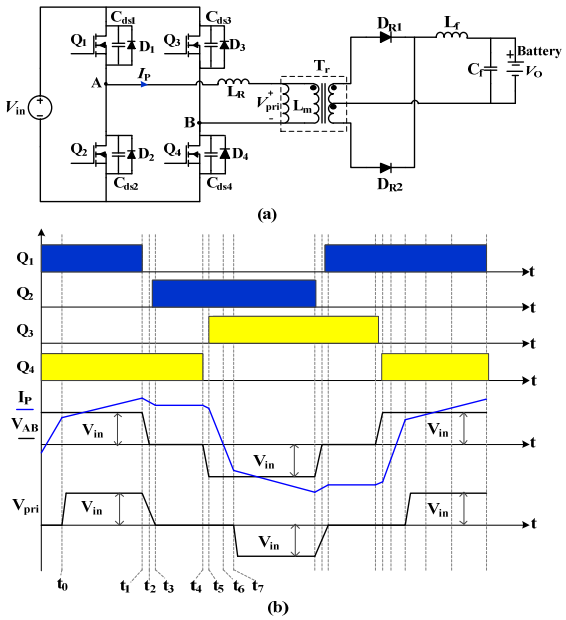



Fig. 1. (a) PSFB converter topology. (b) Key waveforms of the PSFB converter.

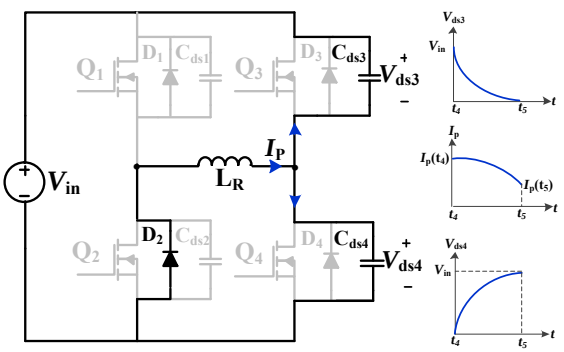



Fig. 2. Equivalent circuit during $t_4$-$t_5$.

$$2C_{ds}\frac{dV_{ds4}(t)}{dt} = I_P(t) \tag{1}$$

$$L_R\frac{dI_P(t)}{dt} + V_{ds4}(t) = 0 \tag{2}$$

Where $V_{ds4}(t)$ is the voltage across $C_{ds4}$, and $I_P(t)$ is the primary current. $C_{ds3} = C_{ds4} = C_{ds}$. Then, during $t_4$-$t_5$,$V_{ds4}(t)$ and $I_p(t)$ can be deduced as [17]:

$$V_{ds4}(t) = Z_1 I_P(t_4)\sin[\omega_1(t-t_4)] \tag{3}$$

$$I_P(t) = I_P(t_4)\cos(t-t_4) \tag{4}$$

Where $I_P(t_4)$ is the primary current at $t_4$, and:

$$\omega_1 = \frac{1}{\sqrt{2L_RC_{ds}}}\quad Z_1 = \sqrt{\frac{L_R}{2C_{ds}}}$$

$V_{ds4}(t)$ can reach $V_{in}$ at the end of the transition interval. Thus, based on (3), the minimum time $t_r$ required for this transition can be deduced as:

$$t_r = \frac{1}{\omega_1}\arcsin\frac{V_{in}}{Z_1 I_P(t_4)} \tag{5}$$

The minimum dead-time consists of the turn-off delay time of the MOSFET $t_{d\text{-off}}$ and the transition interval [12]. This can be expressed as:

$$t_{d\min} = t_{d\_off} + \frac{1}{\omega_1}\arcsin\frac{V_{in}}{Z_1 I_P(t_4)} \tag{6}$$

Meanwhile, if the dead-time is too long, the switch $Q_3$ turns on after the primary current $I_P$ commutation. The ZVS of $Q_3$fails since the voltage across the drain-to-source is increasing. After the voltage transition, $V_{in}$ is impressed across the resonant inductance. Therefore, the primary current ramps down from $t_5$.

$$I_P(t) = I_P(t_5) - \frac{V_{in}}{L_R}(t - t_5) \tag{7}$$

$I_p$ reaches zero at $t_6$. The time interval $t_{56}$ can be deduced as:

$$t_{56} = \frac{L_R I_P(t_5)}{V_{in}} \tag{8}$$

Therefore, the maximum dead-time can be given as:

$$t_{d\max} = t_{d\min} + \frac{L_R I_P(t_5)}{V_{in}} \tag{9}$$

The primary current at $t_4$ and $t_5$can be derived as follows. At $t_0$, the primary current is equal to the reflected output current [18].

$$I_P(t_0) = \frac{I_o - \frac{\Delta I_o}{2}}{N} \tag{10}$$

Where $I_o$ is the output current, $\Delta I_o/2$ is the output current ripple, and $N$ is the turn ratio of the transformer. $\Delta I_o$ can be expressed as:

$$\Delta I_o = \frac{\frac{V_{in}}{N} - V_o}{L_f}\frac{T_s}{2}D_{eff} \tag{11}$$

Where $L_f$ is the value of the output filter inductance, $V_o$ is the output voltage, $T_s$ is the switching cycle, and $D_{eff}$ is the effective duty cycle.

$$D_{eff} = \frac{V_o}{V_{in}/N} \tag{12}$$

During the time period $t_0$-$t_1$, the input voltage $V_{in}$ is mainly impressed across the magnetizing inductance. The magnetizing current increases linearly in this time period. From (10), (11) and (12), the primary current at time $t_1$ can be calculated as:

$$I_P(t_1) = I_P(t_0) + I_{Lm} + \frac{\Delta I_o}{\mathrm{N}} = \frac{I_o}{N} + \frac{(\frac{V_{in}}{N} - V_o)V_o T_s}{4L_f V_{in}} + \frac{NT_s V_o}{2L_m} \tag{13}$$

Where $I_{Lm}$ is the magnetizing current, and $L_m$ is the magnetizing inductance of the transformer.

During the time period $t_1$-$t_3$, $Q_1$ is turned off, the charging of $C_{ds1}$ and $C_{ds2}$ is practically conducted by constant current, and the energy is provided by the output inductor $L_f$ with its current reflected to the primary side. Similar to the calculation process presented in (1)-(4), the primary current at $t_3$ can be expressed as:

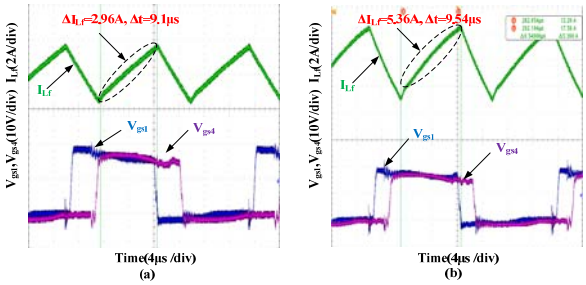



Fig. 3. Experimental waveforms of the output filter inductance current. (a) $I_o$=7A. (b) $I_o$=15A.

$$I_P(t_3) = I_P(t_1)\cos[\arcsin\frac{V_{in}}{Z_1 I_P(t_1)}] = \frac{\sqrt{Z_1^2 I_P^2(t_1) - V_{in}^2}}{Z_1} \tag{14}$$

During $t_3$-$t_4$, the primary current, which is thought to be constant, is freewheeling through the primary side.

$$I_P(t_4) = I_P(t_3) \tag{15}$$

During the time period $t_4$-$t_5$, $Q_4$ is turned off. The primary current begins to charge the parasitic capacitors of $Q_4$ and $Q_3$, and $C_{ds4}$ and $C_{ds3}$. Then the primary current at $t_5$ can be deduced using (4) and (5).

$$I_P(t_5) = I_P(t_4)\cos[\arcsin\frac{V_{in}}{Z_1 I_P(t_4)}] \tag{16}$$

Detailed formulas for the minimum dead-time and the maximum dead-time can be deduced by substituting (10)-(16) into (6) and (9).

However, the traditional analysis is not comprehensive since many factors are not considered.

### *B. Nonlinear Output Filter Inductance Phenomenon*

The output filter inductance is thought to be constant in the traditional analysis. However, when the nonlinear magnetizing permeability of the core material is considered, the actual value of the output filter inductance is variable over a wide load range. Fig. 3 gives experimental waveforms of the current through the output filter inductor in a PSFB converter under different loads (with the same input and output voltages). In Fig. 3, the output filter inductance with a 15A load decreases drastically compared to the 7A load condition. According to (13), the output filter inductance has a significant effect on the primary current. The calculation of the dead-time is affected correspondingly.

### *C. Miller Plateau Phenomenon*

As a part of the dead-time, the length of the Miller Plateau varies with the load current. Fig. 4 gives experimental waveforms of the switching signals of $Q_4$.

From Fig. 4, there is a Miller Plateau during the turn-off procedure of $Q_4$. An obvious difference inthe length of the Miller Plateau between the two kinds of operating conditions is observed. The length of the Miller Plateau at a 3A load is much shorter than that at a 15A load. Therefore, the affection of the Miller Plateau is significant when the converter operates over a

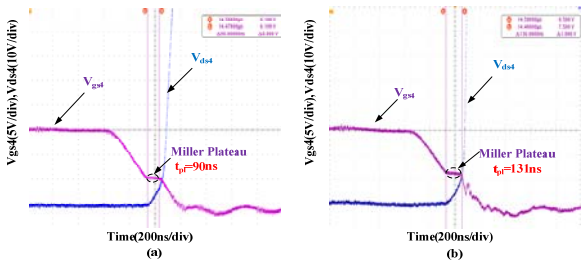



Fig. 4. The experimental switching waveforms of Q4. (a) $I_o$=3A. (b) $I_o$=15A.

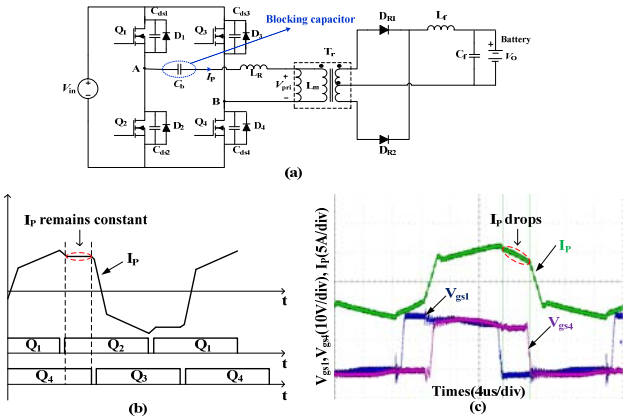



Fig. 5. (a) PSFB converter with blocking capacitor. (b) Primary current without blocking capacitor. (c) Primary current with blocking capacitor.

wide load range and should be taken into consideration.

### *D. Blocking Capacitor Effect*

Ideally, the magnetizing current has no dc bias since the PSFB converter has a symmetrical structure. However, the offset on the magnetizing current appears in practice despite this symmetry. A simple way to prevent the transformer from becoming saturated is to introduce a blocking capacitor in series with the primary winding, as shown in Fig. 5(a). However, the performance of the PSFB converter and the calculation of the dead-time will be affected significantly when the blocking capacitor is considered. Fig. 5(b) and (c) give the waveforms of the primary current without and with the blocking capacitor. From Fig. 5, obvious differences in the primary current can be observed. Consequentially, the setting of the dead-time is affected consequentially.

Based on the descriptions above, phenomena such as the nonlinear output filter inductance, the Miller Plateau and the blocking capacitor effect are important for accurately calculating the dead-time in PSFB converters over a wide load range. The detailed analysis and equation derivations will be presented in the next section.

## III. Comprehensive Analysis and Calculation of Dead-Time

### *A. Effect of the Nonlinear Output Filter Inductance*

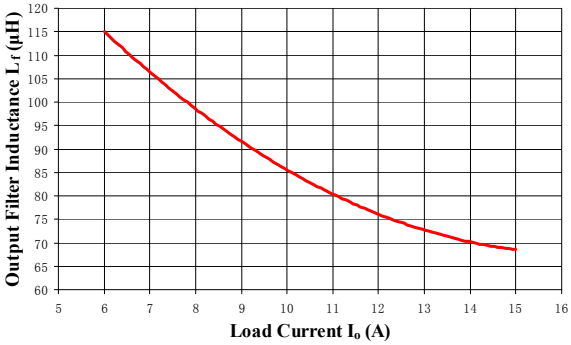



Fig. 6. Nonlinear characteristic of the output filter inductance.

It is well known that permeability is nonlinear when the current flowing through the inductance varies [19]. With an increase incurrent, the energy stored in the inductance increases and the permeability becomes closer to saturation. Normally, when considering the restrictions of size and cost, the output inductor is designed at the full-load operating condition with an allowable maximum stored magnetizing capability before actual magnetizing saturation. Therefore, the nonlinear characteristic of the inductance is certain to exist when it operates over a wide load range according to the magnetization curve.

Fig. 6 gives a fitting curve of the output filter inductance with respect to different load currents. Based on the analysis in [19], the relationship between the current and the nonlinear inductance can be modeled by an $m$'s order polynomial equation as:

$$L_f(i)=\sum_{k=1}^{m}\alpha_k i^{k-1} \tag{17}$$

Where $\alpha_k$ and $m$ are constants that can be obtained from the magnetizing core datasheet by the curve fitting method.

Based on (13) and (17), the primary current at $t_1$ can be rewritten as:

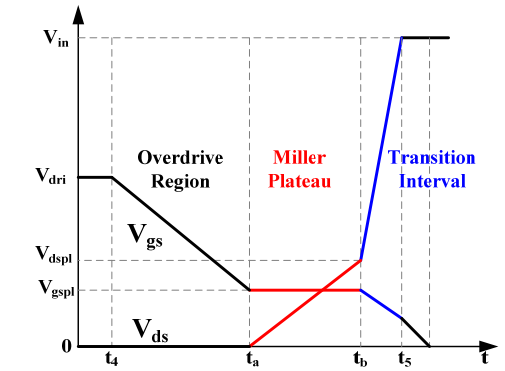
$$I_P(t_1)=\frac{I_o}{N}+\frac{(\frac{V_{in}}{N}-V_o)V_oT_s}{4(\sum_{k=1}^{m}\alpha_k I_o^{k-1})V_{in}}+\frac{NT_sV_o}{2L_m} \tag{18}$$

Therefore, according to (18), the nonlinear characteristic of $L_f$ influences the primary current at $t_1$. The slope of the primary current has a similar variation as the output current ripple. Thus, calculation of the dead-time is inevitably affected.

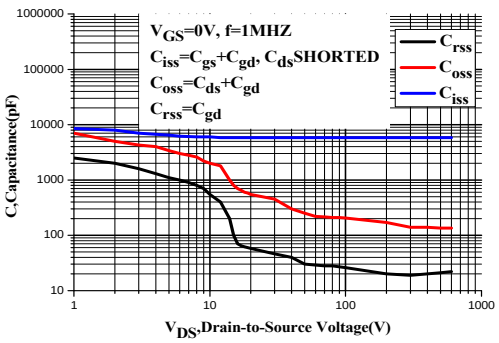
In conclusion, the output current ripple changes with the load current because of the nonlinearity of the output filter inductance. When it is reflected to the primary side, the slope of the primary current has a similar variation. With a larger load current, the output current ripple and the slope of the primary current also become larger.

### *B. Effect of the Miller Plateau*

The turn-on/off procedure of the MOSFET is a part of the dead-time. Since the switches in the PSFB converter can




(a)




(b)

Fig. 7. (a) Turn-off procedure of MOSFET. (b) Nonlinear characteristic of the parasitic capacitance of the MOSFET with respect to the drain-to-source voltage $V_{ds}$.

achieve ZVS-on, there is no Miller Plateau in the turn-on procedure. However, a Miller Plateau occurs during the turn-off procedure because the parasitic capacitors $C_{ds}$ of the two switches are charged in this interval. Moreover, the load current has a significant affection on the length of the Miller Plateau. Detail analyses are shown as follows.

The turn-off procedure of the switch $Q_4$ is shown in Fig. 7 (a). The time period $t_4$-$t_5$ is divided into three intervals. Therefore, the minimum dead-time of the PSFB converter can be expressed as:

$$t_{45} = t_{4a} + t_{ab} + t_{b5} \tag{19}$$

*Interval 1*[$t_4$-$t_a$]: It is the overdrive section, where it is necessary to discharge the gate-to-source capacitor $C_{gs}$ and the gate-to-drain capacitor $C_{gd}$ from the overdrive voltage to the Miller plateau level.

$$t_{4a} = (C_{gs} + C_{gd})\frac{V_{dri} - V_{gspl}}{I_{dri}} \tag{20}$$

Where $I_{dri}$ and $V_{dri}$ are the driving current and voltage. $V_{gspl}$ is the gate-to-source voltage at the beginning of the Miller Plateau.

*Interval 2*[$t_a$-$t_b$]: This is the Miller Plateau. This stage begins the moment the gate-to-source voltage $V_{gs}$ decreases to the Miller Plateau level $V_{gspl}$. During this stage, the gate-to-drain capacitor $C_{gd}$ is charged by the driving current, and the drain-to-source capacitor $C_{ds}$ is charged by the primary current. The charging formulas of $C_{gd}$ and $C_{ds}$ are defined as:

$$\frac{dV_{gd}}{dt} = \frac{I_{dri}}{C_{gd}} \tag{21}$$

$$\frac{dV_{ds}}{dt} = \frac{I_P(t_4)}{2C_{ds}} \tag{22}$$

When the charging rate of $C_{gd}$ is slower than that of $C_{ds}$, the driving current is fully applied to charge $C_{gd}$. Thus, $V_{gs}$ is approximately constant and the Miller Plateau occurs.

Meanwhile, the drain-to-source voltage $V_{ds}$ has a remarkable influence over $C_{gd}$. Fig. 7(b) shows the characteristic of $C_{gd}$ with respect to $V_{ds}$[20]. $C_{gd}$ decreases sharply with arise of the drain-to-source voltage $V_{ds}$. According to [21], $C_{gd}$ is a function of $V_{ds}$, and is approximated by the following equation.

$$C_{gd} = \frac{C_{gd,0}}{K\sqrt{V_{ds}}} \tag{23}$$

where $C_{gd,0}$ and $K$ are related factors that can be found in the datasheet of the MOSFET.

With a rising $V_{ds}$, $C_{gd}$ drops to a certain degree, where the charging rates of both $C_{gd}$ and $C_{ds}$ are identical and the Miller Plateau comes to an end.

By combining (21) and (22), the gate-to-drain capacitance at the end of the Miller plateau $C_{gdpl}$ can be calculated from (24).

$$\frac{I_{dri}}{C_{gdp1}} = \frac{I_P(t_4)}{2C_{ds}} \tag{24}$$

According to (24), a larger output current means a smaller $C_{gdp1}$. In addition, according to (23), a smaller $C_{gdp1}$ means a larger $V_{dspl}$, which is the drain-to-source voltage at the end of the Miller Plateau. Therefore, the value of $V_{dspl}$ increases with an increase of the output current.

Then, the drain-to-source voltage at the end of the Miller Plateau $V_{dspl}$ can be derived from (23). Thus, the length of the Miller Plateau can be obtained from (21), (23) and (24).

$$t_{ab} = \frac{\overline{C_{gd}} V_{dspl}}{I_{dri}} \tag{25}$$

where $\overline{C_{gd}}$ is the average value of $C_{gd}$ in the Miller Plateau.

*Interval 3*[$t_b$-$t_5$]: This is the drain voltage transition interval when $V_{ds}$ rises from $V_{dspl}$ to the supply the voltage $V_{in}$.

$$t_{b5} = \frac{1}{\omega_1}\arcsin\frac{V_{in} - V_{dspl}}{Z_1 I_P(t_4)} \tag{26}$$

In conclusion, due to the nonlinear characteristic of the parasitic capacitance of the MOSFET, the drain-to-source voltage at the end of the Miller Plateau $V_{dspl}$ increases with the load current. As a result, the length of the Miller Plateau increases since the driving current $I_{dri}$ is constant.

### *C. Effect of the Blocking Capacitor*

When a blocking capacitor is introduced into the primary side of the PSFB converter in series with the transformer, ZVS of the lagging leg would be affected. The operation of the

PSFB converter, especially the primary current, has distinct changes in the intervals as follows.

[$t_3$-$t_4$]: In this interval, the switches $Q_2$ and $Q_4$ are conducting and the voltage across the primary side of the transformer is clamped to zero. Due to the introduction of the blocking capacitor, a reverse voltage is impressed across the resonant inductance. Therefore, the primary current decreases in this period. The blocking capacitor and the resonant inductance form a resonant tank in this interval.

$$L_R \frac{dI_P(t)}{dt} + V_{Cb}(t) = 0 \tag{27}$$

$$C_b \frac{dV_{Cb}(t)}{dt} = I_P(t) \tag{28}$$

Where $V_{Cb}(t)$ is the voltage across the blocking capacitor $C_b$, and $I_p(t)$ is the primary current.

Equations (27) and (28) can be rearranged as:

$$\frac{d^2 I_P(t)}{dt^2} + \frac{I_P(t)}{L_R C_b} = 0 \tag{29}$$

$$\frac{d^2 V_{Cb}(t)}{dt^2} + \frac{V_{Cb}(t)}{L_R C_b} = 0 \tag{30}$$

The characteristic equations of (29) and (30) dictate the characteristics of $I_P(t)$ and $V_{Cb}(t)$. The roots of the characteristic equations are:

$$s_{1,2} = \pm j\omega_2 \tag{31}$$

where:

$$\omega_2 = \frac{1}{\sqrt{L_R C_b}}$$

Then, $I_P(t)$ and $V_{Cb}(t)$ can be obtained as:

$$I_P(t) = A_1 \cos[\omega_2 (t - t_3)] + A_2 \sin[\omega_2 (t - t_3)] \tag{32}$$

$$V_{Cb}(t) = B_1 \cos[\omega_2 (t - t_3)] + B_2 \sin[\omega_2 (t - t_3)] \tag{33}$$

where the constants $A_1$ and $B_1$ can be deduced based on the initial conditions $I_P(t_3)$ and $V_{Cb}(t_3)$.

$$A_1 = I_P(t_3) \tag{34}$$

$$B_1 = V_{Cb}(t_3) \tag{35}$$

Using (27) and (35), $A_2$ and $B_2$can be obtained as:

$$A_2 = -\frac{V_{Cb}(t_3)}{\omega_2 L_R} \tag{36}$$

$$B_2 = \omega_2 L_R I_P(t_3) \tag{37}$$

Therefore, (32) and (33) can be rewritten as:

$$I_P(t) = I_P(t_3)\cos[\omega_2 (t - t_3)] - \frac{V_{Cb}(t_3)}{\omega_2 L_R}\sin[\omega_2 (t - t_3)] \tag{38}$$

$$V_{Cb}(t) = V_{Cb}(t_3)\cos[\omega_2 (t - t_3)] + \omega_2 L_R I_P(t_3)\sin[\omega_2 (t - t_3)] \tag{39}$$

In order to calculated the primary current $I_P(t)$, the voltage across the blocking capacitor at $t_3$ needs to be evaluated first. During $t_0$-$t_3$, the blocking capacitor is charged by the primary current. Therefore, the voltage $V_{Cb}(t_3)$ can be deduced as:

$$V_{Cb}(t_3) = V_{Cb}(t_0) + \frac{1}{C_b}\int_{t_0}^{t_3} I_P(t)dt \tag{40}$$

Based on the expressions of the primary current $I_p$ in different time intervals (10), (13) and (14), the integration of the primary current can be expressed as:

$$\int_{t_0}^{t_3} I_P(t)dt = \frac{(I_o - \frac{\Delta I_o}{2})V_o T_s}{2V_{in}} + \frac{(V_{in} - NV_o)V_o^2 T_s^2}{8L_f V_{in}^2} + \frac{N^2 V_o^2 T_s^2}{8L_m V_{in}} + \frac{I_P(t_1)}{\omega_1}\arcsin\frac{V_{in}}{Z_1 I_P(t_1)} \tag{41}$$

According to the analysis in [22] and [23], the voltage across the blocking capacitor $V_{Cb}(t)$ at $t_0$ and $t_4$havethe same value but opposite in direction.

$$V_{Cb}(t_0) = -V_{Cb}(t_4) \tag{42}$$

By substituting (39) and (41) into (40), $V_{Cb}(t_3)$ can be expressed as:

$$V_{Cb}(t_3) = \frac{\frac{1}{C_b}\int_{t_0}^{t_3} I_P(t)dt - \omega_2 L_R I_P(t_3)\sin[\omega_2 (t_4 - t_3)]}{1 + \cos[\omega_2 (t_4 - t_3)]} \tag{43}$$

where:

$$t_4 - t_3 = (1 - D_{eff} - D_{loss})\frac{T_s}{2} \tag{44}$$

$D_{loss}$ is the duty cycle loss and can be obtained from [17]:

$$D_{loss} = \frac{I_p(t_1) + I_p(t_5)}{[V_{in} + V_{cb}(t_4)]T_s} \tag{45}$$

The full expression of $V_{Cb}(t_3)$ can be obtained by substituting (41), (44) and (45) into (43). However, this is too long and not fully visualized here.

Therefore, the primary current at time $t_4$ can be deduced by substituting (42) into (38).

$$I_P(t_4) = I_P(t_3)\cos[\omega_2 (t_4 - t_3)] - \frac{V_{Cb}(t_3)}{\omega_2 L_R}\sin[\omega_2 (t_4 - t_3)] \tag{46}$$

[$t_4$-$t_5$]: The switch $Q_4$ is turned off at $t_4$. The parasitic capacitors of the switches $Q_3$ and $Q_4$, $C_{ds3}$ and $C_{ds4}$, and the resonant inductance $L_R$ form the resonant tank. The blocking capacitor does not take part in the resonant process in this time period because it is much larger than $C_{ds3}$ and $C_{ds4}$.

$$I_P(t_5) = I_P(t_4)\cos[\arcsin\frac{V_{in}}{Z_1 I_P(t_4)}] \tag{47}$$

$$V_{Cb}(t_5) \cong V_{Cb}(t_4) \tag{48}$$

[$t_5$-$t_6$]: During the time period $t_5$-$t_6$, the switch $Q_2$ remains on and the parasitic diode $D_3$ is forward biased. The primary current flows through $Q_2$ and $D_3$. The drain voltage of the switch $Q_4$ is clamped to one forward diode drop above the input voltage $V_{in}$. Here, a resonant tank is formed by the resonant inductance and the blocking capacitance. Thus:

$$L_R \frac{dI_P(t)}{dt} + V_{Cb}(t) + V_{in} = 0 \tag{49}$$

$$C_b \frac{dV_{Cb}(t)}{dt} = I_P(t) \tag{50}$$

Then, the primary current and the voltage across the blocking capacitor during this time period can be expressed as:

$$I_P(t) = I_P(t_5)\cos[\omega_2 (t - t_5)] - \frac{V_{in} + V_{Cb}(t_5)}{\omega_2 L_R}\sin[\omega_2 (t - t_5)] \tag{51}$$

$$V_{Cb}(t) = [V_{Cb}(t_5) + V_{in}]\cos[\omega_2 (t - t_5)] + \omega_2 L_R I_P(t_5)\sin[\omega_2 (t - t_5)] \tag{52}$$

At time $t_6$, the primary current drops to zero.

$$I_P(t_6)=0 \tag{53}$$

This time interval can be given as:

$$t_{56}=\frac{\arcsin[I_P(t_5)\Big/\sqrt{I_P^2(t_5)+[\frac{V_{in}+V_{Cb}(t_5)}{\omega_2 L_R}]^2}]}{\omega_2} \tag{54}$$

According to the above discussions, the primary current during the freewheeling period decreases a lot due to the ac voltage of the blocking capacitor. The ac voltage and the variation of the primary current become larger with a smaller capacitance.

### *D. Equations of the Dead-time*

In summary, accurate formulas of the minimum and maximum dead-time, considering the effects of the nonlinear output filter inductance, the Miller Plateau and the blocking capacitor, can be concluded as follows:

$$t_{d\min}=(C_{gs}+C_{gd})\frac{V_{dri}-V_{gspl}}{I_{dri}}+\frac{\overline{C_{gd}}V_{dspl}}{I_{dri}}+\frac{1}{\omega_1}\arcsin\frac{V_{in}-V_{dspl}}{Z_1 I_P(t_4)} \tag{55}$$

$$t_{d\max}=t_{d\min}+t_{56}=t_{d\min}+\frac{\arcsin[I_P(t_5)\Big/\sqrt{I_P^2(t_5)+[\frac{V_{in}+V_{Cb}(t_5)}{\omega_2 L_R}]^2}]}{\omega_2} \tag{56}$$

where $V_{gsp1}$, $V_{dsp1}$, $I_p(t_4)$, $I_p(t_5)$ and $V_{Cb}(t_5)$ can be obtained from (24)-(25) and (46)-(48).

The theoretical analysis and calculations will be verified separately in next section.

## IV. Measurement Results

In order to verify the above analysis and calculations, a 1.5kW PSFB battery charger prototype is built. A STM32F051MCU is chosen to provide the PWM driving signals. The main parameters of the prototype are listed in Table I. Several tests are carried out separately in order to verify the above analysis.

### *A. Nonlinear Output Filter Inductance Phenomenon Experiment*

Fig. 8 gives experimental waveforms of the output filter inductor current and primary current with respect to different load currents.

The input voltage is 280V and the output voltage is controlled at 90V. From Fig. 8, it can be seen that the slope of the output filter inductance current ripple at a heavy load is larger than that at a light load. A similar difference can be observed on the slope of the primary current during the time period $t_0$-$t_1$, which is equal to the sum of the magnetizing current and the reflected output current ripple. It should be pointed out that there is an oscillation at $t_0$ due to the parasitic capacitance of the output diode. In order to acquire precise results, the oscillation interval has been neglected. Therefore, the time interval may be different for each calculation. However, it has little influence on the final results. The experimental results in Fig. 8 are consistent with the analysis in Section III (A).

TABLE I
Main Parameters of the PSFB Prototype

| | |
|---|---|
| Input Voltage | 260~380Vdc |
| Output Voltage | 60~100Vdc |
| Maximum Load | 15A |
| Switching Frequency | 35KHz |
| Output Inductance | 118μH |
| Resonant Inductance | 57μH |
| MOSFET | IRFPS30N60K |

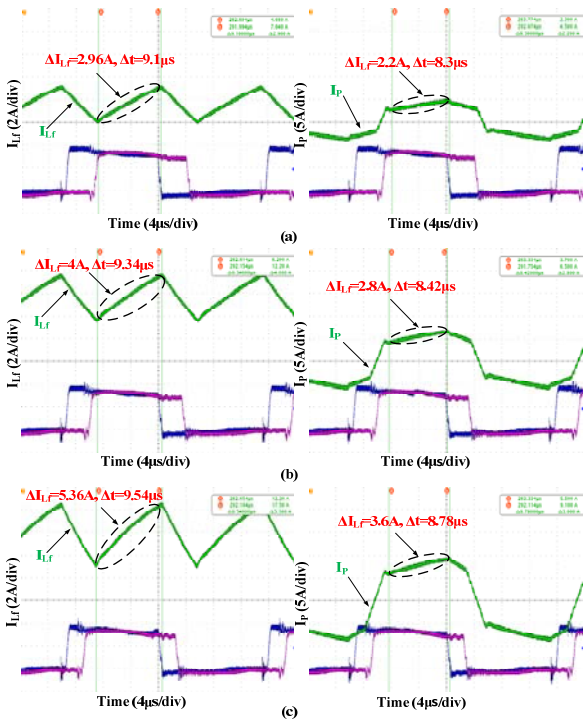



Fig. 8. Experimental waveforms of output filter inductance current $I_{Lf}$ and primary current $I_p$ with respect to different load currents. (a) $I_o$=7A. (b) $I_o$=11A. (c) $I_o$=15A.

### *B. Miller Plateau Phenomenon Experiment*

Fig. 9 shows the experimental results of the turn-off procedure of the MOSFET switch at different load currents. The length of the Miller Plateau and the value of $V_{dspl}$ at various load currents are shown. It can be seen that the length of the Miller Plateau at a full load is much longer than that at a light load. There is also a significant difference in the voltage across drain-to-source $V_{dspl}$ when the Miller Plateau ends with different load currents.

Both the calculated and experimental results of the length of the Miller Plateau for various load currents are presented in Fig. 10. It can be seen that the two curves are almost the same. According to the experimental results, the analysis in Section III(B) is well verified.

### *C. Blocking Capacitance Effect Experiment*

Fig. 11 shows experimental waveforms of the primary current

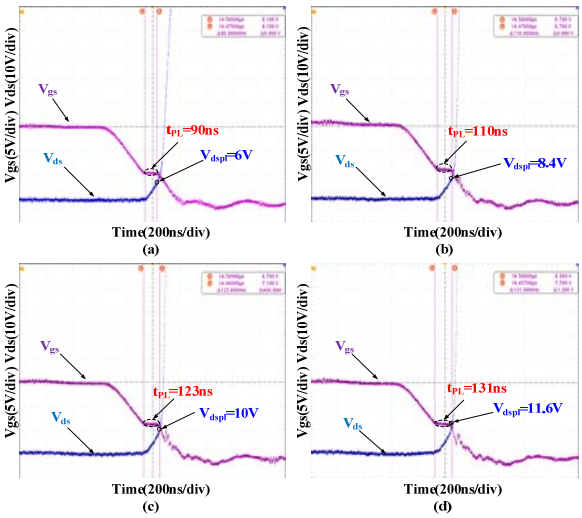



Fig. 9. Experimental waveforms of the turn-off procedure of the MOSFET. (a) $I_o$=3A. (b) $I_o$=7A. (c) $I_o$=11A. (d) $I_o$=15A.

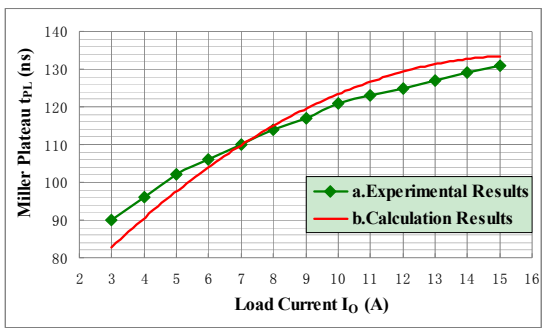



Fig. 10. Effect of load variation on the Miller Plateau length.

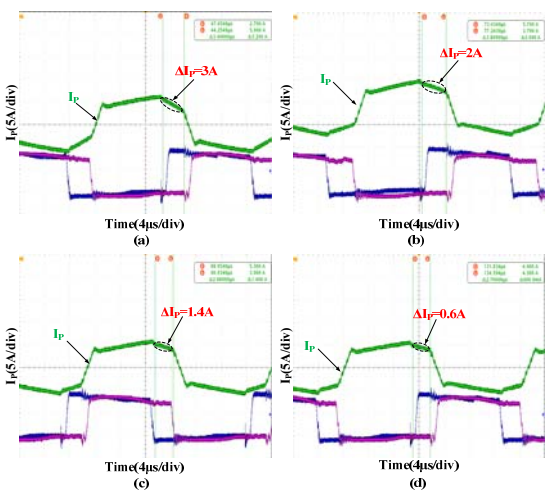



Fig. 11. Experimental waveforms of the primary current with respect to different blocking capacitances. (a) $C_b$=0.66μF. (b) $C_b$=1μF. (c) $C_b$=1.22μF. (d) $C_b$=1.66μF.

with different blocking capacitances. The load current is set at 10A. From Fig. 11, it can be seen that the primary current has an obvious change during the time period $t_3$-$t_4$,and that the primary current changes drastically with a small blocking capacitance.

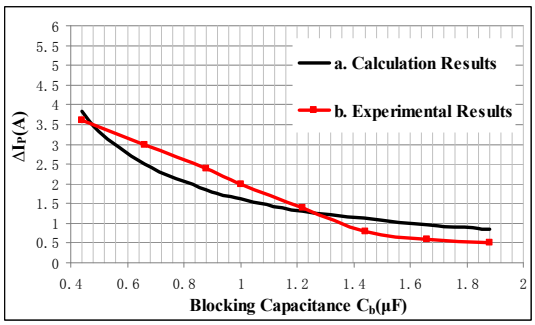



Fig. 12. Effect of the blocking capacitance variation on the primary current.

Fig. 12 gives the calculated and experimental results of the primary current variation during the time period $t_3$-$t_4$ for varying blocking capacitances. The two results are similar and have the same trend.

### *D. ZVS Experiments Compared with the Previous Method*

As mentioned before, a long dead-time will make the adjustment range of the duty cycle narrow and reduce the dynamic performance of the converter. Thus, under most circumstances (especially in high frequency converters), the dead-time should be selected based on the minimum requirements. In the proposed 1.5kW PSFB battery charger prototype, the minimum dead-time which can ensure the ZVS of the MOSFETs over the load range (5~15A) is 633ns using the proposed method, and it is 595ns using the traditional analysis. A security margin of5% is added in real applications. As a result, the dead-time is selected to be 633(1+5%)=664ns and 595(1+5%)=624ns,respectively. ZVS and efficiency tests are run over a wide load range and the results are shown in Fig. 13 and Fig. 14.

According to Fig. 13, the ZVS of $Q_4$ in the lagging leg is achieved from a full load to the minimum load when the dead-time is selected to be 660ns using the proposed method. Meanwhile, the ZVS of the lagging leg failed when the load current was smaller than 10A with 620ns calculated by the conventional analysis.

The tiny difference between the selected value and real-time applications is due to the limitation of the digital PWM resolution. The efficiency curve in Fig. 14 verifies the ZVS results. While the efficiency with the proposed method is maintained when the output current is higher than 10 A, it shows a higher level under light load conditions compared to the conventional method.

In addition, in some low frequency applications, the dead-time has a weak influence on the adjustment range of the duty cycle. A long dead-time is preferred by designers to avoid shoot-through problems. Similarly, the dead-time is set to 997 (1-5%)=947ns based on the proposed method and 1597(1-5%)=1517ns based on the conventional analysis. ZVS and efficiency tests are run over a wide load range and the results are shown in Fig. 15 and Fig. 16.

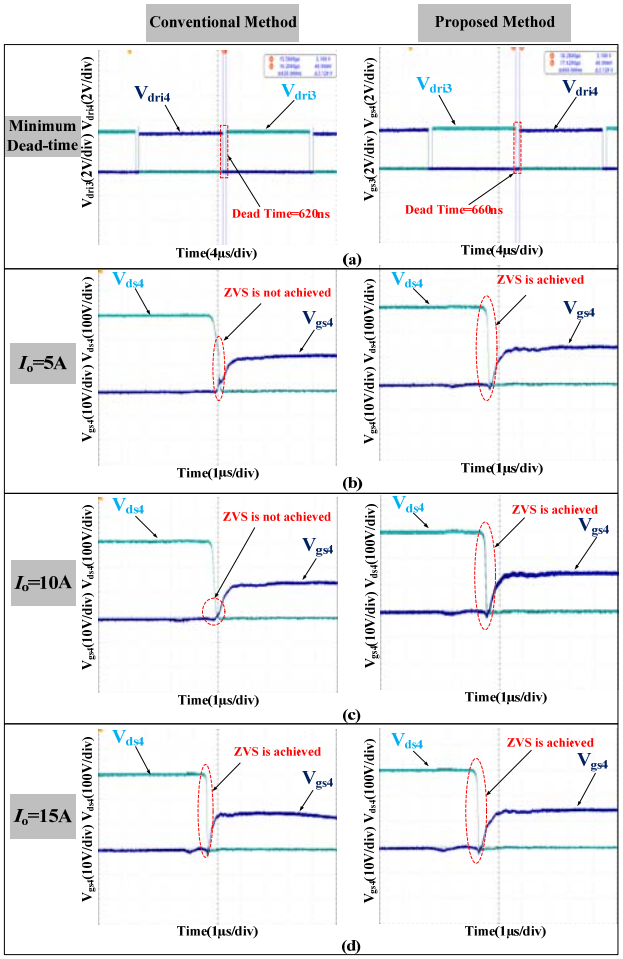



Fig. 13. ZVS conditions at different loads with the minimum dead-time calculated using the conventional and the proposed method. (a) Dead-time. (b) $I_o$=5A. (c) $I_o$=10A. (d) $I_o$=15A.

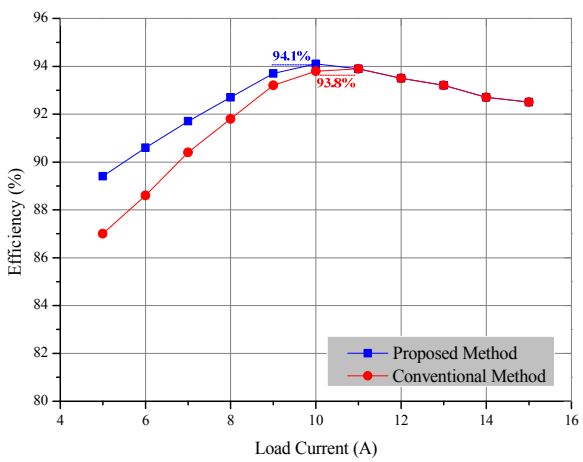



Fig. 14. Efficiency with the minimum dead-time.

According to Fig. 15, the ZVS of $Q_4$ in the lagging leg is achieved from a full load to the minimum load when the dead-time is selected to be 940ns using the proposed method, while the ZVS of the lagging leg failed with a 1520ns dead-time calculated by the conventional analysis. The improved efficiency is shown in Fig. 16.

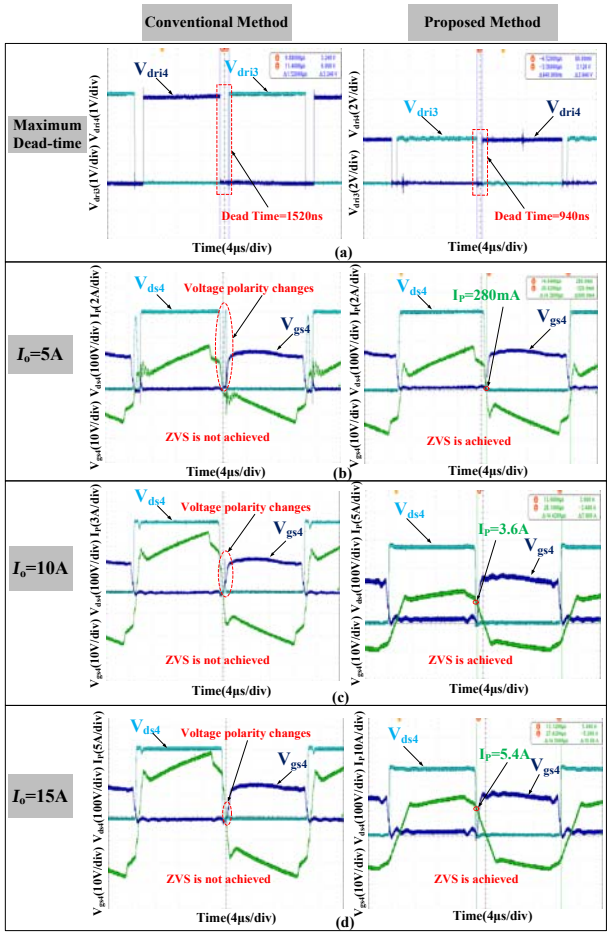



Fig. 15. ZVS conditions at different loads with the maximum dead-time calculated using the conventional and the proposed method. (a) Dead-time. (b) $I_o$=5A. (c) $I_o$=10A. (d) $I_o$=15A.

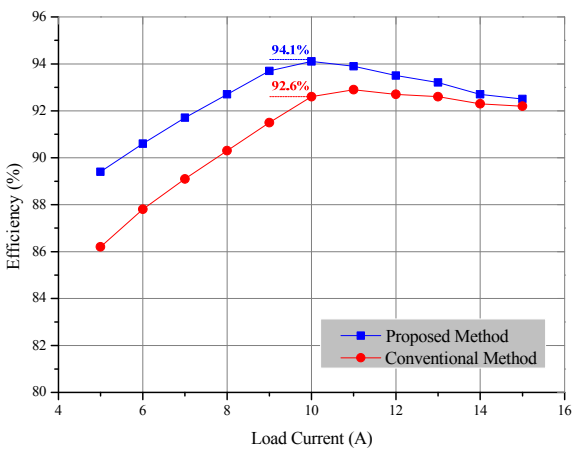
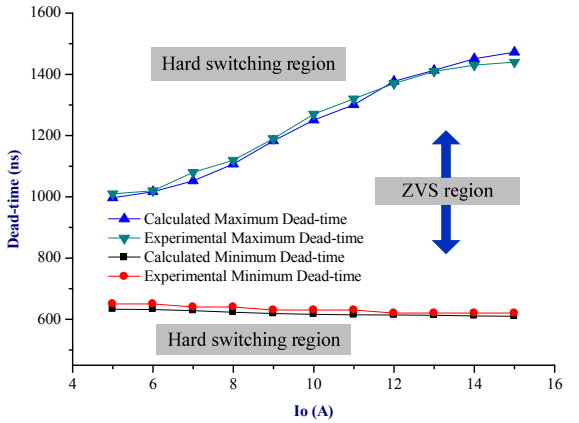
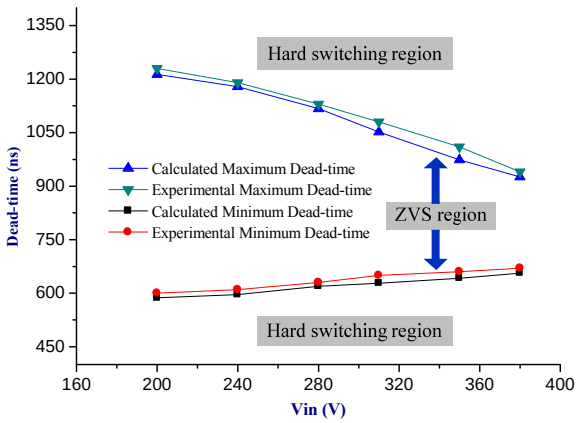



Fig. 16.Efficiency with the maximum dead-time.

Furthermore, experimental results of the dead-time range for ZVS and the calculation results using the proposed method when the input voltage or load current changes are shown in Fig. 17. In Fig. 17(a), when the input voltage is fixed at 310Vdc, the dead-time range obtained from the proposed method and the experimental results are given with load changes from 5A to 15A.In addition, when the output




(a)




(b)

Fig. 17.Calculated and experimental results of the dead-time range. (a) The load varies from 5A to 15A. (b) The input voltage varies from200Vdc to 380Vdc.

terminal is fixed at 7A and 70V, the dead-time ranges obtained from the proposed method and the experimental results are given with input voltage changes from 200Vdc to 380Vdc, as shown in Fig. 17(b). The experimental results of the dead-time range are obtained from massive ZVS tests, and dead-time changes with a 10ns step, which is the minimum resolution of the digital PWM in the proposed prototype. According to Fig. 17, the dead-time calculated using the proposed method matches well with the experimental results.

Therefore, using the proposed method, an optimal dead-time can be selected to meet the specific requirements of a system. At the same time, ZVS can be achieved over a wide load range. Strictly speaking, when ZVS failed with the dead-time calculated using the conventional method, system designers can adjust the dead-time and run the ZVS tests again until ZVS is achieved. However, it is time consuming, and more importantly, the optimal dead-time is very hard to determine by experiments.

## V. CONCLUSIONS

Dead-time for the ZVS in a battery charger with the PSFB topology is comprehensively analyzed and calculated in this paper. The effects of the nonlinear output filter inductance, the Miller Plateau length and the blocking capacitor are considered and analyzed for the first time. Based on these, analytical equations of the dead-time range for ZVS are deduced. A 1.5kW prototype is built to verify the above analysis. The analysis results of the three effects are verified separately. Subsequently, ZVS experimental results show that, compared to traditional analysis, the optimal dead-time can be obtained from the proposed method to meet specific system requirements and to achieve ZVS over the entire load range at the same time.

## ACKNOWLEDGMENT

This work was supported by the National Nature Science Foundation of China (51277026), Qing Lan Project and Suzhou Application Basic Research Project (SYG201450).

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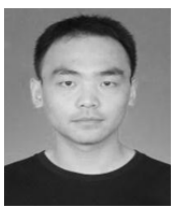

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