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A High-Efficiency High Step-Up Interleaved Converter with a Voltage Multiplier for Electric Vehicle Power Management Applications

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Abstract

This paper proposes a novel high-efficiency high-step-up interleaved converter with a voltage multiplier, which is suitable for electric vehicle power management applications. The proposed interleaved converter is capable of achieving high step-up conversion by employing a voltage-multiplier circuit. The proposed converter lowers the input-current ripple, which can extend the input source's lifetime, and reduces the voltage stress on the main switches. Hence, large voltage spikes across the main switches are alleviated and the efficiency is improved. Finally, a prototype circuit with an input voltage of 24 V, an output voltage of 380 V, and an output rated power of 1 kW is implemented and tested to demonstrate the functionality of the proposed converter. Moreover, satisfying experimental results are obtained and discussed in this paper. The measured full-load efficiency is 95.2%, and the highest measured efficiency of the proposed converter is 96.3%.

Key words: High step-up conversion, Interleaved boost converter

I. INTRODUCTION

Due to their cleanliness and sustainability, renewable energy sources are being employed worldwide out of consideration for environment-protection issues [1]-[10]. Generally speaking, the voltage levels of renewable energy sources, such as photovoltaic cells and fuel cells, are low. Thus, DC-DC converters that feature high step-up conversion have been widely utilized in such renewable energy systems to raise their voltage levels [11]-[15]. Fig. 1 shows a block diagram of a typical electric vehicle power management system. This kind of electric vehicle, powered by fuel cell stacks, is fueled with hydrogen and only emits water and heat without any pollutants. Referring to Fig. 1, the high step-up interleaved converters serving as DC/DC power converters are capable of converting the low levels of input voltage from fuel cell stacks into high levels of output voltage, which are then fed into a battery set or a DC/AC inverter for supplying a tractions motor with an AC load. Hence, high efficiency, high step-up DC/DC converters play an important role in this kind of power management system.

The conventional DC/DC converters for raising voltage levels, such as boost converters and flyback converters, adopt an extremely high duty cycle or a high turns ratio of the coupled inductor to achieve a high voltage gain. Adopting an extremely high duty cycle in the step-up converters incurs large conduction losses and serious diode reverse-recovery problems. Due to the high voltage stresses that occur on the power devices, power switches with a low $R_{DS(ON)}$ and power diodes with a low reverse-recovery time cannot be employed in this type of high-step-up converter.

Some high-step-up converters that utilize coupled inductors and switched capacitors, which recycle the leakage-inductance energy and lower the voltage stresses, have been proposed in the literature [16]-[22]. This paper proposes a novel high-step-up interleaved converter with a built-in transformer and a voltage-multiplier circuit to raise the voltage gain of the presented converter and to lower the voltage stresses on the power devices. The presented

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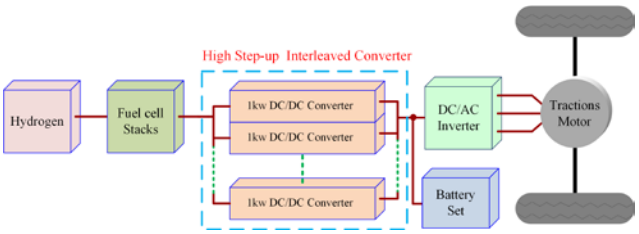


Fig. 1. Block diagram of a typical electric vehicle power management system.

converter features high step-up conversion, high circuit efficiency, a low input-current ripple, increased lifetime of the input renewable energy source, and it is suitable for electric vehicle power management applications. In addition, the built-in transformer and voltage-multiplier circuit extend the voltage gain and lower the voltage stresses. As a result, low-voltage-rated semiconductor devices (such as power MOSFETs and diodes) can be adopted in the presented converter. The key characteristics of the proposed converter are listed as follows: (1) Lowering the input-current ripple and reducing the conduction losses results in an increased lifetime of the renewable energy sources. (2) The converter easily obtains a high step-up gain. (3) By recycling the leakage energy, the voltage stresses of the clamp diodes are alleviated and the circuit efficiency is improved. (4) The voltage stresses on the semiconductor components are substantially lower than the output voltage.

This paper is organized as follows. Section II describes and analyzes the proposed high-step-up interleaved converter with a voltage multiplier. Section III analyzes the voltage gain, voltage stresses and conduction losses in the presented converter. Section IV presents experimental results of a prototype circuit for supplying a 1kW rated load. Finally, some conclusions are provided in Section V.

II. Description and Analysis of the Proposed High-Step-up Interleaved Converter with a Voltage Multiplier

A circuit diagram of the proposed interleaved high-step-up converter is shown in Fig. 2. As illustrated, it contains a built-in transformer and a voltage-multiplier circuit. In addition, L_1 and L_2 are the energy storage inductors; S_1 and S_2 are the power switches; C_1 and C_2 are the clamp capacitors; C_{o1}, C_{o2} and C_{o3} are the output capacitors; D_1 and D_2 are the clamp diodes; and D_3, D_4, D_5 and D_6 are the rectified diodes. The built-in transformer consists of a primary winding N_p, a secondary winding N_s, and a leakage inductor L_k. The turns ratio n is the ratio of the secondary winding N_s and the primary winding N_p. Using inductors on the input terminal of the interleaved converter can achieve a low level of input-current ripple. The voltage-multiplier circuit, which includes diodes (D_1 and D_2) and capacitors (C_1 and C_2), raises the voltage gain of the converter, clamps the voltages and

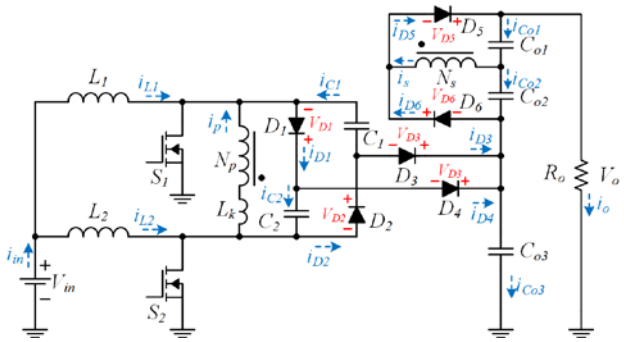


Fig. 2. Circuit diagram of the proposed high-step-up interleaved boost converter.

alleviates the spikes across the power switches. Furthermore, a high step-up and a reduction of the losses across the power switches are attained by utilizing the built-in transformer, which includes a primary winding N_p connected with power switches S_1 and S_2, and a secondary winding N_s connected with capacitors C_{o1} and C_{o2} and diodes D_5 and D_6.

The gate-driving signals of the two power switches are interleaved with a 180-degree phase shift, and the principal waveform of the proposed converter operating in the continuous-conduction mode (CCM) is depicted in Fig. 3. Fig. 4 shows the corresponding operational modes of the equivalent circuit. There are 10 main operational modes in one switching period. Due to the symmetrical nature of the interleaved topology, operating modes 1 to 5 are similar to modes 6 to 10. In order to simplify the analysis of the proposed converter's operating principle, only modes 1 to 5 are analyzed and discussed. A detailed analysis of each operational mode in the proposed converter is shown in the following.

Mode 1 [t_0, t_1]:

At t=t_0, both power switches (S_1 and S_2) turn on. All of the diodes (D_1, D_2, D_3, D_4, D_5 and D_6) are reverse-biased. The path of the current flow is shown in Fig. 4(a). The inductors (L_1 and L_2) are charged by the input voltage V_{in}, and the currents increase linearly though the inductors (L_1 and L_2). The inductor currents (i_{L1} and i_{L2}) are given by:

$$i_{L1}(t) = I_{L1}(t_0) + \frac{V_{in}}{L_1} \cdot t \tag{1}$$

$$i_{L2}(t) = I_{L2}(t_0) + \frac{V_{in}}{L_2} \cdot t \tag{2}$$

In addition, the capacitors C_{o1}, C_{o2} and C_{o3} provide energy to the output load R_o.

Mode 2 [t_1, t_2]:

At t=t_1, the power switch S_2 turns off, and its parasitic capacitor is charged by the inductor current i_{L2}. The path of the current flow is shown in Fig. 4(b). The voltage of the parasitic capacitor is given by:

$$V_{DS2}(t) = \frac{I_{L2}(t_1)}{C_{ds2}} \cdot t\,. \tag{3}$$

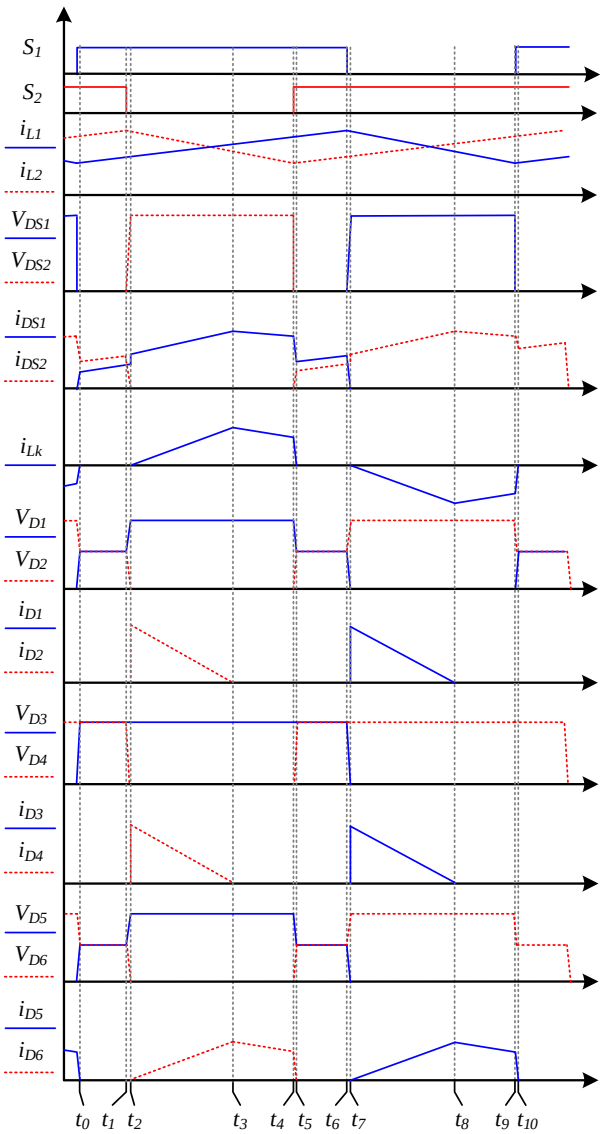


Fig. 3. Principal waveform of the proposed interleaved boost converter in CCM.

The capacitors C_{o1}, C_{o2} and C_{o3} continue providing energy to the output load R_o.

Mode 3 [t_2, t_3]:

At t=t_2, the power switch S_2 remains off. The voltages of the clamp diode D_2 and the rectified diodes (D_4 and D_5) decrease. Then D_2, D_4 and D_5 begin to turn on at t=t_2. The path of the current flow is shown in Fig. 4(c). The input voltage V_{in} and inductor L_2 provide energy to the primary winding N_p of the built-in transformer, and to the clamp capacitor C_1.

The drain-source voltage of the power switch S_2 is clamped by the capacitor C_1. In addition, the input voltage V_{in}, the inductor L_2 and the capacitor C_2 provide energy to the capacitor C_{o3} through the diode D_4. The energy on the primary winding N_p is transferred to the capacitor C_{o1} and the load R_o through the built-in transformer. The currents through L_2, L_k and S_1 are given by:

$$i_{L2}(t) = i_{D2}(t) + i_{D4}(t) + n \cdot i_{D5}(t) \quad (4)$$

$$i_{Lk}(t) = n \cdot i_{D5}(t) \quad (5)$$

$$i_{DS1}(t) = i_{L1}(t) + i_{D2}(t) + n \cdot i_{D5}(t) \quad (6)$$

Mode 4 [t_3, t_4]:

At t=t_3, the power switch S_2 is still off. The diode currents (i_{D2} and i_{D4}) decrease to zero, and the clamp capacitor voltage V_{C1} is equal to the drain-source voltage of the power switch S_2. The path of the current flow is shown in Fig. 4(d). The input voltage V_{in} and the inductor L_2 still transfer energy to the output capacitor C_{o1} and the load R_o through the built-in transformer. The currents through L_2, L_k and S_1 are respectively given by:

$$i_{L2}(t) = i_{D4}(t) + n \cdot i_{D5}(t) \quad (7)$$

$$i_{Lk}(t) = n \cdot i_{D5}(t) \quad (8)$$

$$i_{DS1}(t) = i_{L1}(t) + n \cdot i_{D5}(t) \quad (9)$$

Mode 5 [t_4, t_5]:

At t=t_4, the power switch S_2 turns on. The rectified diode D_5 remains forward-biased because the leakage inductor current i_{Lk} still exists. Because a major portion of the inductor current i_{L2} still flows into the power switch S_1 through the leakage inductor L_k of the primary winding, the switch loss across the power switch S_2 is reduced. The product of V_{DS} and i_{DS} can be decreased. Thus, the conversion efficiency is improved. The path of the current flow is shown in Fig. 4(e). The inductor current through i_{L2} is given by:

$$i_{L2}(t) = i_{DS2} + n \cdot i_{D5}(t). \quad (10)$$

This mode ends when the leakage inductor current i_{Lk} decreases to zero at t=t_5, and rectified diode D_5 begins to be reverse-biased.

III. Analysis of the Voltage Gain, Voltage Stresses, and Conduction Losses

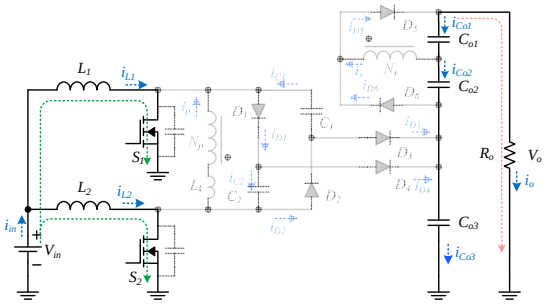
To simplify the analysis of the presented converter operating in the CCM, the transient characteristics of circuits are disregarded, and small-ripple approximation is used for calculation. Thus, all of the currents passing through the components are approximately represented by their DC components. In addition, some formulated assumptions are shown in the following.

1) All of the components in the proposed interleaved boost converter possess ideal characteristics.

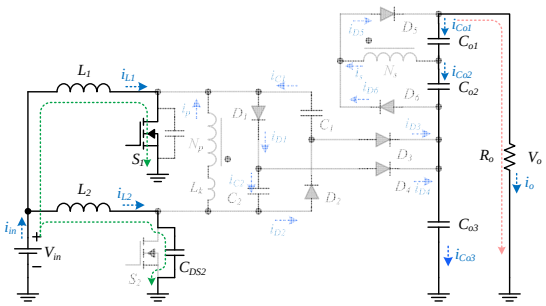
2) The coupling coefficient of the built-in transformer is unity. Hence, there is no leakage inductor in either the primary or secondary side of the transformer.

3) The voltages on capacitors and currents through the inductors are considered to be constant due to infinitely large capacitances and inductances.

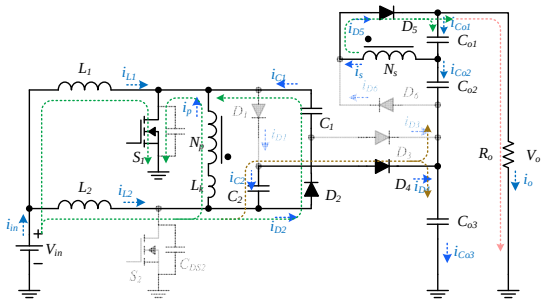
4) Due to a completely symmetrical interleaved structure and operation, symmetrical components with the same characteristic and effects are defined by identical symbols. For example, D_1 and D_2 are defined as D_c; D_3 and D_4 are



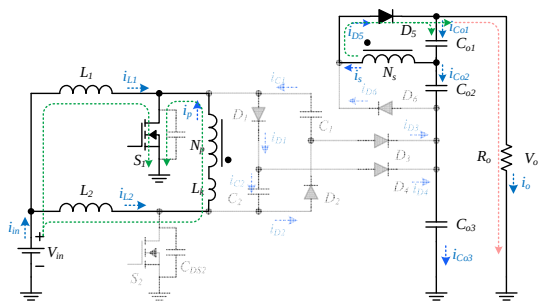
(a) *Mode 1* [t_0, t_1].



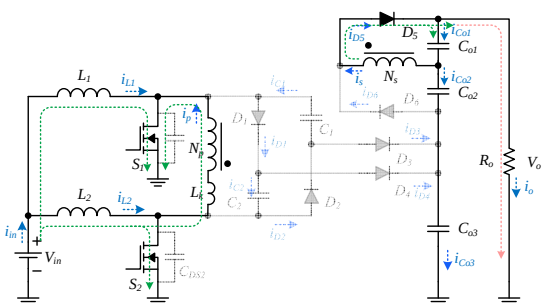
(b) *Mode 2* [t_1, t_2].



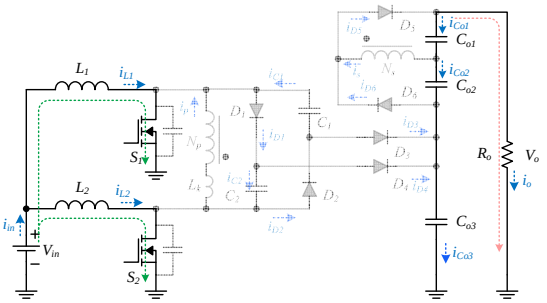
(c) *Mode 3* [t_2, t_3].



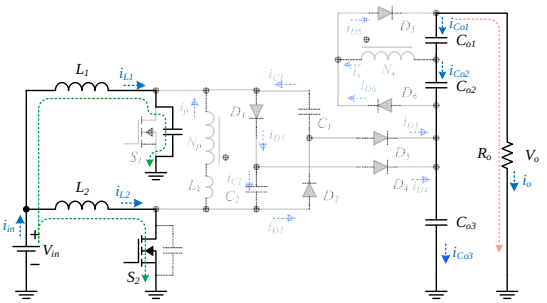
(d) *Mode 4* [t_3, t_4].



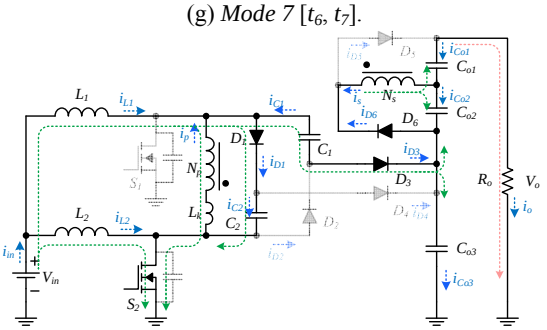
(e) *Mode 5* [t_4, t_5].



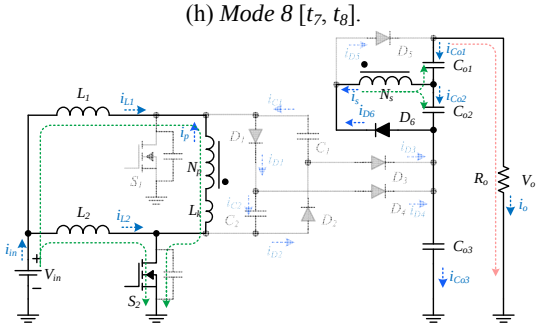
(f) *Mode 6* [t_5, t_6].



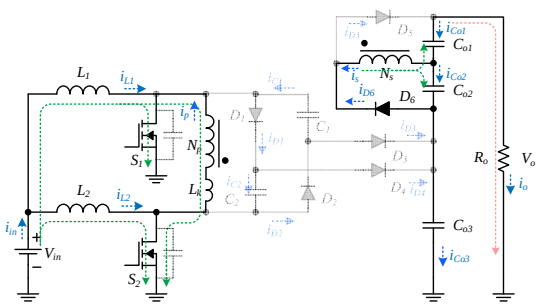
(g) *Mode 7* [t_6, t_7].



(h) *Mode 8* [t_7, t_8].



(i) *Mode 9* [t_8, t_9].



(j) *Mode 10* [t_9, t_{10}].

Fig. 4. The operating modes of the proposed interleaved boost converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9. (j) Mode 10.

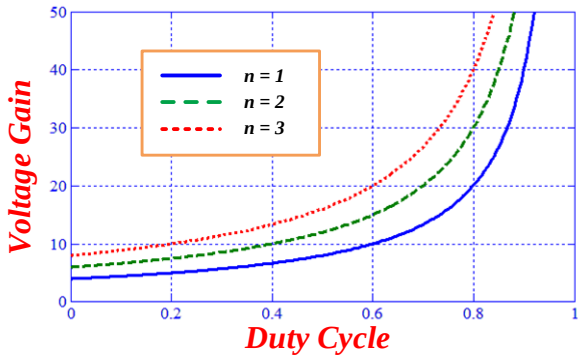


Fig. 5. The voltage gain versus duty cycle in the proposed converter under different levels of turns ratio n.

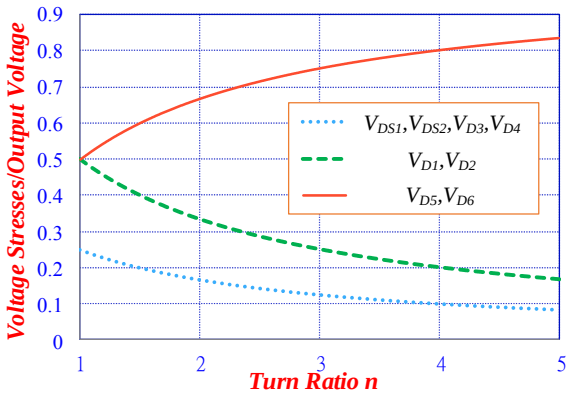


Fig. 6. The estimated voltage stresses on power switches and diodes.

defined as D_{fp}; and D_5 and D_6 are defined as D_{fs}.

A. Voltage Gain

All of the voltages on the capacitors can be derived by the voltage-second balance theorem. The voltage on the clamp capacitors (C_1 and C_2) can be expressed as:

$$V_{C1} = V_{C2} = \frac{1}{1-D} \cdot V_{in}, \tag{11}$$

The voltages on the output capacitors (C_{o1}, C_{o2} and C_{o3}) can be derived from:

$$V_{Co1} = V_{Co2} = \frac{n}{1-D} \cdot V_{in} \tag{12}$$

$$V_{Co3} = \frac{2}{1-D} \cdot V_{in} \tag{13}$$

The output voltage V_o is equal to the sum of the voltage on the output capacitors (C_{o1}, C_{o2} and C_{o3}). Hence, the output voltage V_o can be given by:

$$V_o = V_{Co1} + V_{Co2} + V_{Co3} = \frac{2 \cdot (1+n)}{1-D} \cdot V_{in} \tag{14}$$

The ideal voltage gain of the proposed interleaved boost converter can be obtained as:

$$\frac{V_o}{V_{in}} = \frac{2 \cdot (1+n)}{1-D}. \tag{15}$$

Equation (15) confirms that the proposed interleaved converter has a high step-up voltage conversion gain without adopting a large turns ratio or an extremely high duty cycle. When the duty cycle is 0.6, the conversion gain reaches 15 at a turns ratio n of 2. The curves of the voltage gain related to the duty cycle in the proposed converter, under different turns ratio levels for the built-in transformer, are shown in Fig. 5.

B. Voltage Stresses

All of the voltage stresses on the semiconductor components can be derived by the known voltages of the capacitors. The voltage stresses of the power switches S_1 and S_2 are clamped, and are derived from:

$$V_{DS1} = V_{DS2} = \frac{1}{1-D} V_{in}. \tag{16}$$

The voltage stresses on the diodes (D_1, D_2, D_3 and D_4) are given by:

$$V_{D1} = V_{D2} = \frac{2}{1-D} V_{in} \tag{17}$$

$$V_{D3} = V_{D4} = \frac{1}{1-D} V_{in} \tag{18}$$

$$V_{D5} = V_{D6} = V_o = \frac{2n}{1-D} V_{in} \tag{19}$$

The relationship between the voltage stresses versus the output voltage V_o and the turns ratio n is illustrated in Fig. 6. All of the voltage stresses on the components are lower than the output voltage V_o. The voltage stress on the power switches (S_1 and S_2) and rectified diodes (D_3 and D_4) is less than 0.25, and the voltage stress on the champed diodes (D_1 and D_2) is lower than 0.5. Although the voltage stress on the rectified diodes (D_5 and D_6) is higher than the voltage stresses on the semiconductor components, they are still lower than the output voltage V_o. Thus, the proposed converter has low voltage stresses on its semiconductor components. Hence, low-voltage-rated power devices, such as MOSFETs with a low $R_{DS(ON)}$ and Schottky diodes with a shorter reverse-recovery time, can be employed for improving the circuit efficiency.

C. Conduction Losses

An equivalent circuit for analyzing the conduction losses of the inductors and semiconductor components in the proposed converter is shown in Fig. 7, in which r_{L1} and r_{L1} are the copper resistances of the inductors, r_{DS1} and r_{DS2} are the on-resistances of the power switches, V_{D1}, V_{D2}, V_{D3}, V_{D4}, V_{D5} and V_{D6} are the forward voltages of the diodes, and r_{D1}, r_{D2}, r_{D3}, r_{D4}, r_{D5} and r_{D6} are the forward resistances of the diodes.

Due to the symmetrically interleaving structure and operation, symmetrical components with the same characteristic are defined by identical symbols in Equations (18) and (19). For example, r_{L1} and r_{L2} are defined as r_L, r_{D1} and r_{D2} are defined as r_{Dc}, r_{DS1} and r_{DS2} are defined as r_{DS}, V_{D1} and V_{D2} are defined as V_{Dc}, r_{D3} and r_{D4} are defined as r_{Df}, V_{D3}

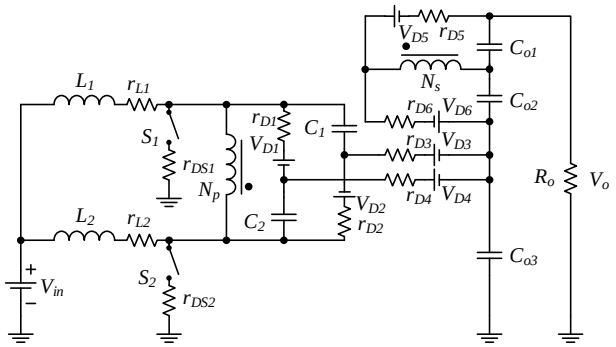


Fig. 7. Equivalent circuit for analyzing conduction losses in the proposed converter.

and V_{D4} are defined as r_{Dfp}, and V_{D5} and V_{D6} are defined as r_{Dfs}. A small-ripple approximation is used to calculate the conduction losses. Thus, all of the currents passing through the components are approximately represented by their DC components. The magnetizing currents and capacitor voltages are assumed to be constant because of the infinite values of the magnetizing inductors and capacitors. Finally, by using the voltage-second balance and capacitor-charge balance theorems, the voltage conversion ratio, including the conduction losses of the power devices, can be derived from:

$$\frac{V_o}{V_{in}} = \frac{\dfrac{2(1+n)}{1-D} - \dfrac{V_{Dc}+V_{Dfp}+2V_{Dfs}}{V_{in}}}{\dfrac{r_w}{2R_o\cdot(1-D)^2} + \dfrac{r_x+r_y+r_z}{2R_o\cdot(1-D)} + 1}, \tag{20}$$

where:

$$r_w = (2D-1)\cdot(2+2n)^2\cdot(r_L+r_{DS})$$
$$r_x = (2+2n)^2\cdot r_L$$
$$r_y = (3+4n)^2\cdot r_{Dc}$$
$$r_z = r_{Dc}+r_{Dfp}+4r_{Dfs}$$

In addition, the circuit efficiency is expressed by:

$$\eta = \frac{V_{in} - \dfrac{(1-D)\cdot(V_{Dc}+V_{Dfp}+2V_{Dfs})}{2\cdot(1+n)}}{V_{in}\cdot\left[\dfrac{r_w}{2R_o\cdot(1-D)^2} + \dfrac{r_x+r_y+r_z}{2R_o\cdot(1-D)} + 1\right]} \tag{21}$$

Fig. 8 shows the calculated voltage gain and circuit efficiency versus the duty cycle including the conduction losses of the power devices. Referring to Fig. 8, the calculated voltage gain is smaller than the ideal one shown in Fig. 5 due to the conduction loss. As illustrated, it is easy for the proposed converter to achieve high step-up voltage conversion. As a result, the converter is suitable for electric vehicle power management applications.

IV. Experimental Results

A 1kW prototype circuit of the proposed high-step-up converter has been built and tested. The electrical specifications for the presented converter are shown in Table I. The design considerations of the proposed converter include the component selection and inductor design, both of which are based on the analysis presented in the previous section. Because the proposed converter possesses a high step-up gain, the turns ratio can be set as 1.5 for the prototype circuit. This has the effect of reducing the cost, volume and conduction losses of the windings inside the built-in transformer.

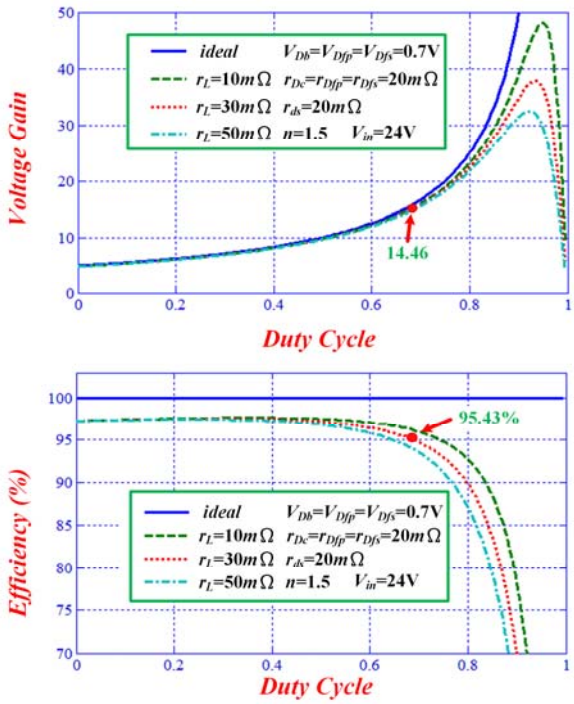
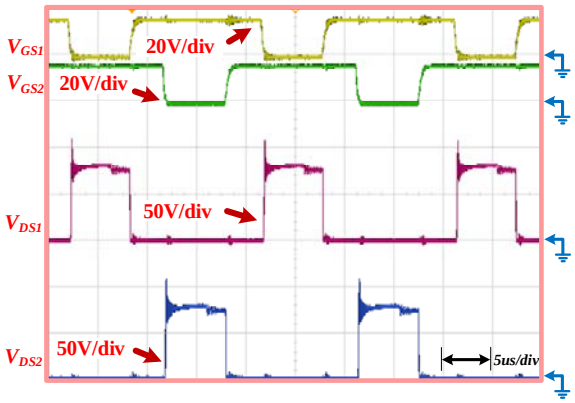


Fig. 8. Calculated voltage gain and circuit efficiency versus duty cycle including conduction losses of power devices.

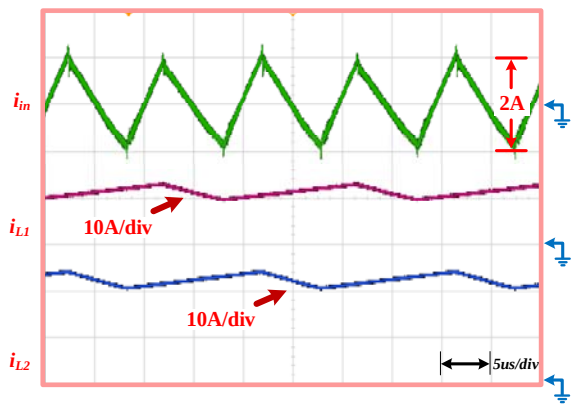
TABLE I
Electrical Specifications

Components	Parameters
Input Voltage V_{in}	24V
Output Voltage V_o	380V
Switching Frequency f_s	50kHz
Maximum Power P_o	1kW
Main Switches S_1 and S_2	IRFP4310
Diodes D_1, D_2, D_3 and D_4	MBR20200
Diodes D_5 and D_6	MUR1640
Capacitors C_1 and C_2	4.7 μF
Output Capacitors C_{o1}, C_{o2} and C_{o3}	330 μF
Filter Inductors L_1 and L_2	110 μH
Turn Ratio N_s / N_p	1:1.5

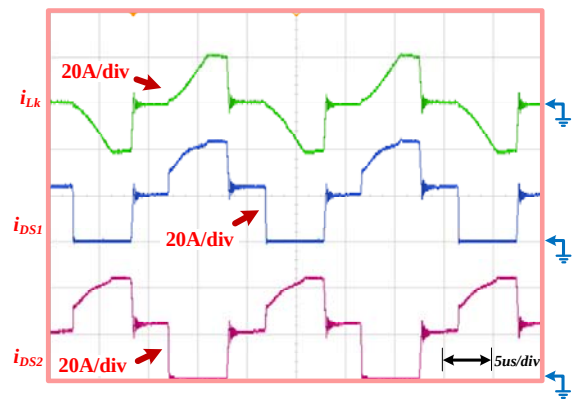
Fig. 9 shows experimental waveforms of the proposed converter measured at a full load of 1 kW. Fig. 9(a) shows the interleaved pulse-width modulation (PWM) signals V_{GS1} and V_{GS2}, as well as the voltage stresses V_{DS1} and V_{DS2} on the power switches. Although spikes occur on S_1 and S_2, caused



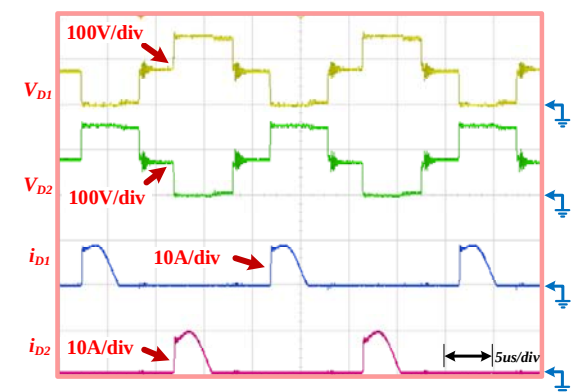
(a)



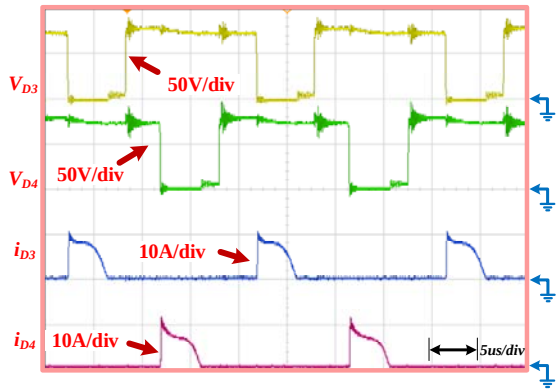
(b)



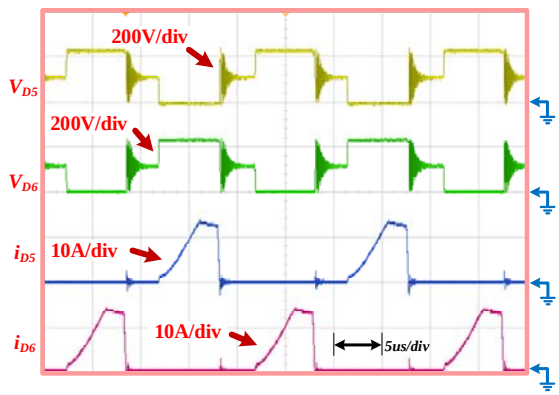
(c)



(d)



(e)



(f)

Fig. 9. The experimental waveforms for the proposed converter measured at a full load of 1 kW: (a) V_{GS1}, V_{GS2}, V_{DS1} and V_{DS2}, (b) i_{in}, i_{L1}, and i_{L2}, (c) i_{Lk}, i_{DS1} and i_{DS2}, (d) V_{D1}, V_{D2}, i_{D1} and i_{D2}, (e) V_{D3}, V_{D4}, i_{D3} and i_{D4}, and (f) V_{D5}, V_{D6}, i_{D5} and i_{D6}.

by the resonance of the parasitic inductors in the circuit and equivalent drain-to-source capacitor C_{DS} of the MOSFETs, the leakage energy can still be recycled to the output load. In addition, the voltage stresses V_{DS1} and V_{DS2} are clamped at 80 V, which is much lower than the output voltage. Fig. 9(b) shows the measured ripple of the input current i_{in} and the inductor currents i_{L1} and i_{L2}. It also demonstrates a small ripple occurring on the input current. The current ripple is approximately one-twentieth of the input current at a full load. Fig. 9(c) shows the leakage-inductor current i_{Lk} and the currents through the power switches S_1 and S_2. Fig. 9(d) shows the measured voltage and current waveforms of the diodes D_1 and D_2. The voltage stresses on the diodes D_1 and D_2 are equal to V_{DS2} plus V_{C2} and V_{DS1} plus V_{C1}, respectively. Fig. 9(e) shows the measured voltage and current on the diodes D_3 and D_4. In addition, the voltage stresses on the diodes D_3 and D_4 are equal to V_{Co3} minus V_{DS}. Fig. 9(f) shows the measured voltage and current on the diodes D_5 and D_6. In addition, the voltage stresses on the diodes D_5 and D_6 are equal to V_{Co1} plus V_{Ns} and V_{Co1} plus V_{Ns}, where V_{Ns} is equal to V_{Co3} minus $V_{C(clamp)}$. The currents i_{D1}, i_{D2}, i_{D3} and i_{D4} decrease to zero with very slight reverse-recovery losses for the diodes. The ringing effects of the diode voltages, shown in Fig. 9(d),

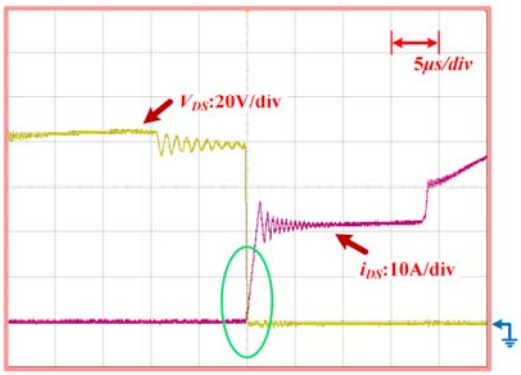


Fig. 10. The current i_{DS} and voltage V_{DS} on the power switch *S*.

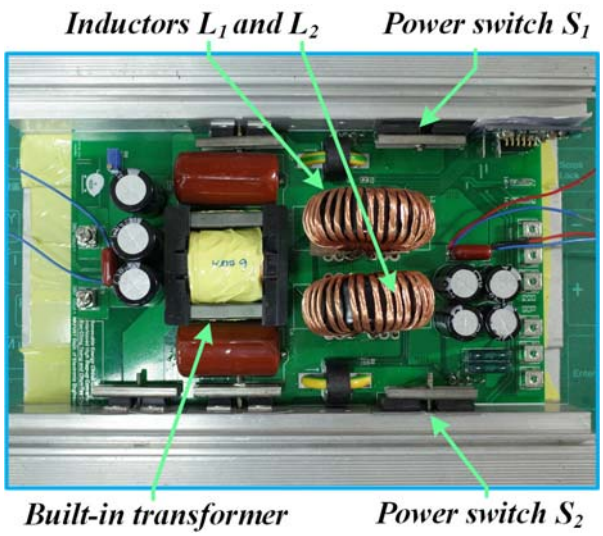


Fig. 11. Photo of the presented converter.

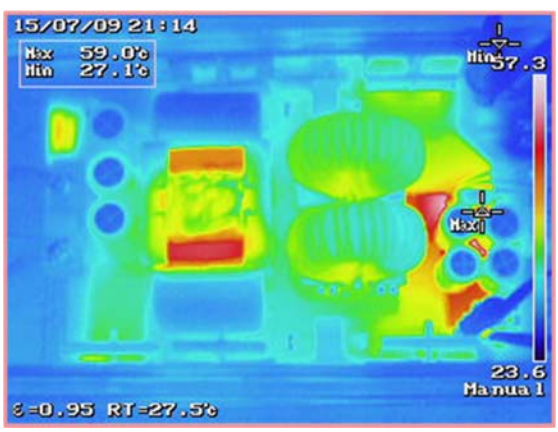


Fig. 12. Temperature distribution in the proposed converter.

Fig. 9(e) and Fig. 9(f), are caused by the resonance due to the parasitic inductors in the circuit, the leakage inductors of the transformer in the primary and secondary sides, and the junction capacitors of the diodes. Fig. 10 shows i_{DS} and V_{DS} on the power switch *S*. The switch loss is lower than that of other hard-switching converters. Fig. 11 shows a photo of the presented converter, and some of the key components are marked. Fig. 12 shows the temperature distribution in the

Fig. 13. The measured data of the proposed converter under a full-load condition.

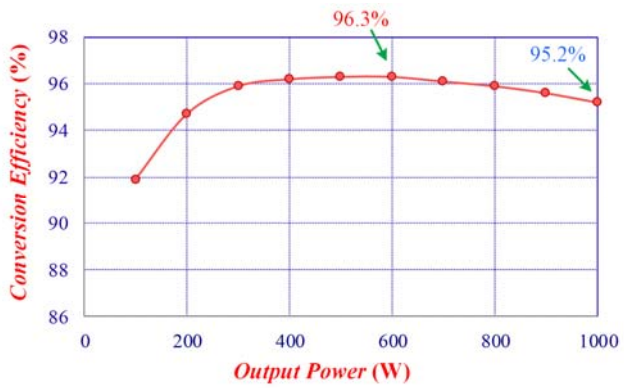


Fig. 14. The efficiency curves of the proposed high-step-up converter.

proposed converter at a full load of 1 kW by using a true infrared (IR) thermal imager (Agilent U5855A). The measured maximum and minimum temperatures are 59 ^{o}C and 27.1 ^{o}C, respectively.

Fig. 13 presents the measured data of the proposed converter under the full-load condition (1 kW), obtained using a power analyzer (HIOKI 3390). The efficiency of the proposed converter measured per 100 W is illustrated in Fig. 14. In addition, the measured highest efficiency is 96.3% at 600 W, and the measured efficiency is 95.2% at a full load of 1 kW. Fig. 8 shows the calculated voltage gain and circuit efficiency under the 1kW load condition (the circuit parameters are: r_L=30$m\Omega$, V_{Db}=V_{Dfp}=V_{Dfs}=0.7V, r_{ds}=20$m\Omega$, r_{Dc}=r_{Dfp}= r_{Dfs}=20$m\Omega$ and R_o =144Ω). At a duty cycle *D* of 0.68, the measured voltage gain shown in Fig. 13 is approximately 15.8 (380.26V/24.069V) which is slightly larger than the calculated one 14.46. The measured efficiency under the full-load condition shown in Fig. 14 is 95.2%, which is slightly smaller than the calculated one (95.43%). The measured waveforms when the converter starts and a load step-up/down from 20% to 80% of the rated load are shown in Fig. 15 and Fig. 16, respectively.

In addition, Table II shows some comparisons (including the voltage gain, component counts, switching losses, transformer type, voltage multiplier type, input current ripple, converter specifications, maximum efficiency and full-load

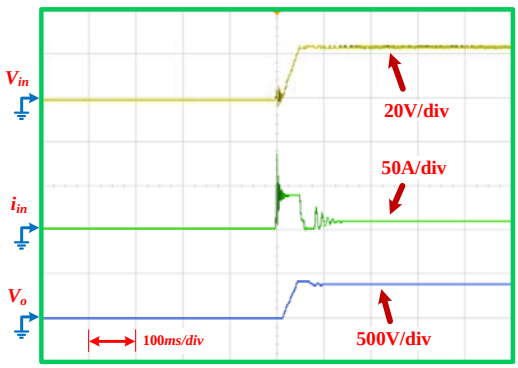


Fig. 15. The measured waveform when the proposed converter starts.

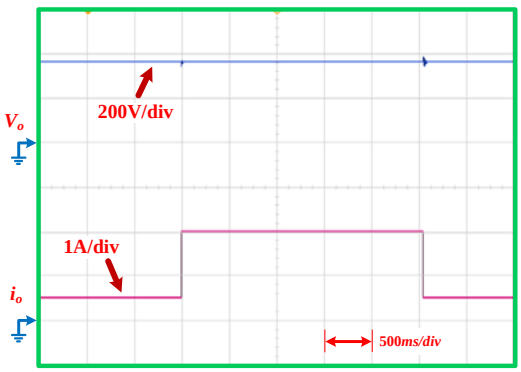


Fig. 16. The measured waveform when the load step-up/down from 20% to 80% rated load.

TABLE II

COMPARISON BETWEEN THE EXISTING HIGH STEP-UP CONVERTERS ([23], [24], [25] AND [26]) AND THE PROPOSED ONE

Topology	Converter introduced in [23]	Converter introduced in [24]	Converter introduced in [25]	Converter introduced in [26]	Proposed high power converter
Voltage gain	$n_2+1+\frac{2n_2D+1}{1-D}$	$\frac{2+2n}{1-D}$	$\frac{2+2n}{1-D}$	$\frac{1+2n}{1-D}$	$\frac{2+2n}{1-D}$
Quantities of power switches	2	2	2	2	2
Quantities of diodes	6	6	6	4	6
Quantities of magnetic cores	2	3	2	3	3
Quantities of capacitors	5	5	5	3	5
Switching losses	High	Low	High	High	Medium
Transformer type	Coupled inductor	Built-in transformer	Coupled inductor	Coupled inductor	Built-in transformer
voltage-multiplier type	Series and parallel	Series	Series and parallel	Parallel	Series and parallel
Input current ripple	Small	Very Small	Small	Small	Very Small
Converter specifications	48V to 380V	35V to 380V	35V to 380V	16V to 180V	24V to 380V
Maximum efficiency	About 96.5% at 300W	About 95.7% at 400W	About 97.1% at 400W	About 95.4% at 100W	About 96.3% at 600W
Full-load efficiency	About 92.6% at 2kW	About 94.5% at 1kW	About 96.4% at 1kW	About 91% at 500W	About 95.2% at 1kW

efficiency) between the existing high step-up converters (including Ref. [23], [24], [25] and [26]) and the proposed converter. As shown in table II, the input current ripples in the proposed high step-up converter and those in [24] are smaller than those in [23], [25], and [26]. In addition, the full-load efficiencies in the proposed high step-up converter and in [25] are larger than those in [23], [24], and [26].

V. CONCLUSION

This paper proposed a highly efficient, high-step-up interleaved boost converter with a built-in transformer for electric vehicle power management applications. Analysis of the operational modes, voltage gain and stresses are included, and a 1kW prototype converter has been developed and tested. The presented interleaved boost converter reduces the input-current ripple, recycles the leakage energy through the lossless passive-clamp circuit, and lowers the voltage spikes across the power switches. Furthermore, the measured full-load efficiency is 95.2% at a rated output power of 1 kW, and the highest efficiency is 96.3% at an output power of 600 W. Experimental results have demonstrated the functionality of the proposed converter and shown that it has advantages in terms of high a step-up voltage gain and a high efficiency.

REFERENCES

[1] J. T. Bialasiewicz, "Renewable energy systems with photovoltaic power generators: Operation and modeling," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 7, pp. 2752-2758, Jul. 2008.

[2] Y. Xiong, X. Cheng, Z. J. Shen, C. Mi, H. Wu, and V. K. Garg, "Prognostic and warning system for power-electronic modules in electric, hybrid electric, and fuel-cell vehicles," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 6, pp. 2268-2276, Jun. 2008.

[3] H. Tao, J. L. Duarte, and M. A.M. Hendrix, "Line-interactive UPS using a fuel cell as the primary source," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 8, pp. 3012-3021, Aug. 2008.

[4] R. J. Wai, W. H. Wang, and C. Y. Lin, "High-performance stand-alone photovoltaic generation system," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 1, pp. 240-250, Jan. 2008.

[5] R. J. Wai and W. H. Wang, "Grid-connected photovoltaic generation system," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 55, No. 3, pp. 953-964, Apr. 2008.

[6] K. Jin, X. Ruan, M. Yan, and M. Xu, "A hybrid fuel cell system," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 4, pp. 1212-1222, Apr. 2009.

[7] L. Gao, R. A. Dougal, S. Liu, and A. P. Iotova, "Parallel-connected solar PV system to address partial and rapidly fluctuating shadow conditions," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 5, pp. 1548-1556, May 2009.

[8] B. Yang, W. Li, Y. Zhao, and X. He, "Design and analysis of a grid-connected photovoltaic power system," *IEEE Trans. Power Electron.*, Vol. 25, No. 4, pp. 992-1000, Apr. 2010.

[9] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison, "Cascaded dc-dc converter photovoltaic systems: Power optimization issues," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 2, pp. 403-411, Feb. 2011.

[10] T. Kefalas and A. Kladas, "Analysis of transformers working under heavily saturated conditions in grid-connected renewable energy systems, " *IEEE Trans. Ind. Electron.*, Vol. 59, No. 5, pp. 2342-2350, May. 2012.

[11] S. K. Changchien, T. J. Liang, J. F. Chen, and L. S. Yang, "Novel high step-up DC-DC converter for fuel cell energy conversion system," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 6, pp. 2007-2017, Jun. 2010.

[12] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1239-1250, Apr. 2011.

[13] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, design and experimental results of wide range ZVS active-clamped L-L type current-fed dc/dc converter for fuel cells to utility interface," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 1, pp. 473-485, Jan. 2012.

[14] W. Li, W. Li, X. He, D. Xu, and B. Wu, "General derivation law of nonisolated high-step-up interleaved converters with built-in transformer," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 3, pp. 1650-1661, Mar. 2012.

[15] K. C. Tseng, C. C. Huang, and W. Y. Shih, "A high step-up converter with a voltage multiplier module for a photovoltaic system," *IEEE Trans. Power Electron.*, Vol. 28, No. 6, pp. 3047-3057, Jun. 2013.

[16] C. T. Pan and C. M. Lai, "A high-efficiency high step-up converter with low switch voltage stress for fuel-cell system applications," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 6, pp. 1998-2006, Jun. 2010.

[17] S. M. Chen, T. J. Liang, L. S. Yang, and J. F. Chen, "A safety enhanced, high step-up dc-dc converter for ac photovoltaic module application," *IEEE Trans. Power Electron.*, Vol. 27, No. 4, pp.1809-1817, Apr. 2012.

[18] T. J. Liang, J. H. Lee, S. M. Chen, J. F. Chen, and L. S. Yang, "Novel isolated high-step-up DC-DC converter with voltage lift," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 4, pp. 161-171, April 2013.

[19] Y. Zhao, X. Xiang, W. Li, X. He, and C. Xia, "Advanced symmetrical voltage quadrupler rectifiers for high step-up and high output-voltage converters," *IEEE Trans. Power Electron.*, Vol. 28, No. 4, pp.1622-1631, April 2013.

[20] W. Li, X. Xiang, C. Li, W. Li, and X. He, "Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for distributed PV generation system," *IEEE Trans. Ind. Electron.*, Vol. 28, No. 1, pp. 300-313, Jan. 2013.

[21] F. Evran and M. T. Aydemir, "Isolated high step-up DC-DC converter with low voltage stress," *IEEE Trans. Power Electron.*, Vol. 29, No. 7, pp. 3591-3603, July 2014.

[22] K. C. Tseng and C. C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 3, pp. 1311-1319, Mar. 2014.

[23] K. C. Tseng, J. Z. Chen, J. T. Lin, C. C. Huang, and T. H. Yen, "High step-up interleaved forward-flyback boost converter with three-winding coupled inductors" *IEEE Trans. Power Electron.*, Vol. 30, No. 9, pp. 4696-4703, Sep. 2015.

[24] W. Li, W. Li, X. Xiang, Y. Hu, and X. He, "High step-up interleaved converter with built-in transformer voltage multiplier cells for sustainable energy applications," *IEEE Trans. Ind. Electron.*, Vol. 29, No. 6, pp. 2829-2836, Jun. 2014.

[25] K. C. Tseng and C. C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 3, pp. 1311-1319, Mar. 2014.

[26] Gustavo A. L. Henn, R. N. A. L. Silva, Paulo P. Praca, Luiz H. S. C. Barreto, and Demercil S. Oliveira, Jr, "Interleaved-boost converter with high voltage gain," *IEEE Trans. Power Electron.*, Vol. 25, No. 11, pp. 2753-2761, Nov. 2010.

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