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A Fabrication and Testing of New RC CMOS Oscillator Insensitive Supply Voltage Variation

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***Abstract*:** A controller area network (CAN) receiver measures differential voltage on a bus to determine the bus level. Since 3.3V transceivers generate the same differential voltage as 5V transceivers (usually ≥1.5V), all transceivers on the bus (regardless of supply voltage) can decipher the message. In fact, the other transceivers cannot even determine or show that there is anything different about the differential voltage levels. A new CMOS RC oscillator insensitive supply voltage for clock generation in a CAN transceiver was fabricated and tested to compensate for this drawback in CAN communication. The system consists of a symmetrical circuit for voltage and current switches, two capacitors, two comparators, and an RS flip-flop. The operational principle is similar to a bistable multivibrator but the oscillation frequency can also be controlled via a bias current and reference voltage. The chip test experimental results show that oscillation frequency and power dissipation are 500 kHz and 5.48 mW, respectively at a supply voltage of 3.3 V. The chip, chip area is 0.021 mm^2, is fabricated with 0.18 μm CMOS technology from SK hynix.

***Keywords*:** RC oscillator, CAN(controller area network), CMOS oscillator

1. Introduction

Current controller area network (CAN) communication is widely used at a maximum transmission speed of 1Mbps in power grid applications. There are necessary application blocks [1] in CAN communication. One of these blocks is the clock generator, which determines the transmission rate and error compensation for data rate transmission.

The clock generator uses an integrated RC oscillator in order to reduce the cost and power dissipation of microprocessor, and transceiver (CAN and FlexRay) [2, 3]. The clock generator is also needed for temperature stability. The way to provide these features is to design core RC oscillation and a stable bias circuit for variation of temperature and supply voltage [4-7]. This proposed CMOS RC oscillator insensitive temperature and supply voltage can use CAN and FlexRay transceiver applications. The oscillator consists of a core oscillation circuit and a bias circuit insensitive temperature and supply voltage. This paper shows a design for the core RC oscillator and bias current circuits. Chip fabrication and testing were also performed.

This paper is organized as follows. Section 2 describes the circuit configuration and operating principle of the proposed RC oscillation and the comparator circuit. Section 3 discusses the experimental data and its interpretation. Section 4 concludes this paper.

2. Circuit Configuration and Operation Principle

Figs. 1 and 2 show the proposed RC oscillator and timing diagram, respectively. This oscillator is composed of the following: four switching transistors, an RS flip-flop (F/F), two comparators, a bias circuit block, two voltage reference sources (V_{REF_H}, V_{REF_L}), and two capacitors. The oscillator configuration is a symmetrical circuit that has both sides (i.e. right and left sides) that operates the same, and its operation can be described as using one side only. The operating principle is explained below.

Assuming that the comparator is operating identically and ideally, and that the Q signal of the RS-F/F is on low (0V) status, then transistor M_2 turns on when transistor M_1

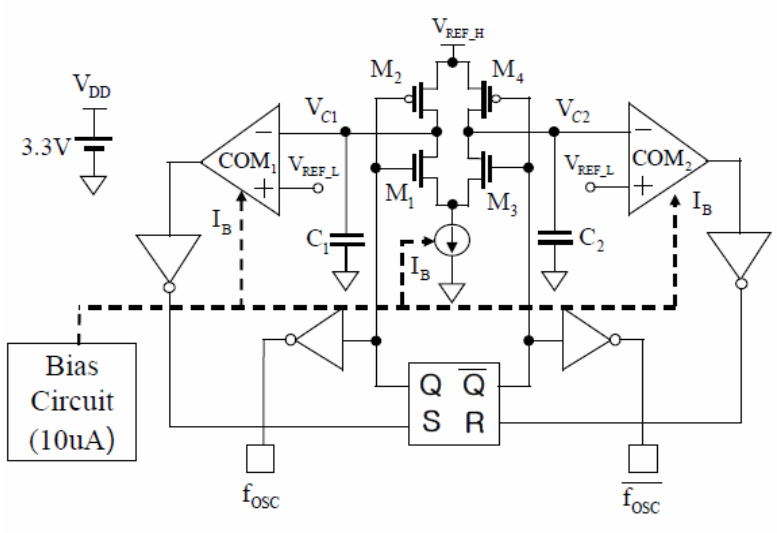

Fig. 1. Block diagram of the proposed oscillator.

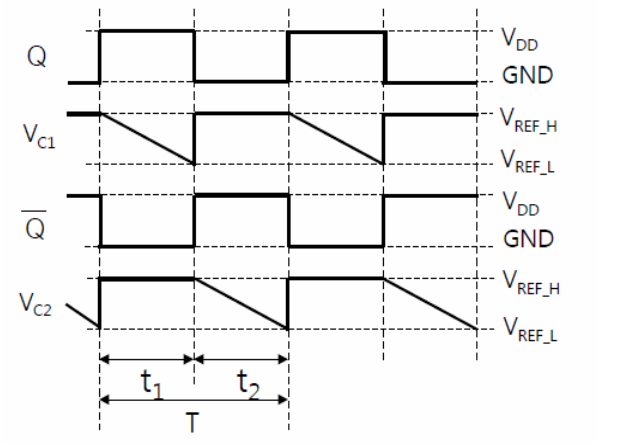

Fig. 2. Timing diagram (b).

turns off. The voltage of V_{C1} therefore will increase (charging) to V_{REF_H}. Timing t_1, can be defined as follow:

$$t_1 = \frac{C_2}{I_B} \cdot \left(V_{REF\_H} - V_{REF\_L} \right) \tag{1}$$

On the other hand, switching transistor M_2 will turn off and M_1 will turn on if the Q signal of the RS-F/F is set to high voltage (V_{DD}). Therefore, the voltage of V_{C1} decreases (discharging) to V_{REF_L}:

$$t_2 = \frac{C_1}{I_B} \cdot \left(V_{REF\_H} - V_{REF\_L} \right) \tag{2}$$

If capacitors $C_1 = C_2 = C$, then the frequency, f_{osc}, of the oscillator can be written as

$$T = |t_1| + |t_2| = 2\frac{C}{I_B} \cdot \left(V_{REF\_H} - V_{REF\_L} \right) \tag{3}$$

$$f_{osc} = \frac{I_B}{2C} \cdot \frac{1}{\left(V_{REF\_H} - V_{REF\_L} \right)} \tag{4}$$

This shows that bias current I_B and voltage references V_{REF_H}, and V_{REF_L} have insensitive variation in supply voltage and temperature. The proposed oscillator needs to

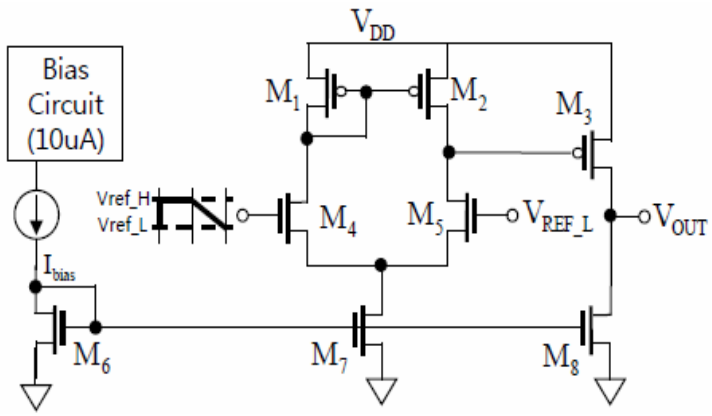

Fig. 3. Circuit diagram of the proposed comparator.

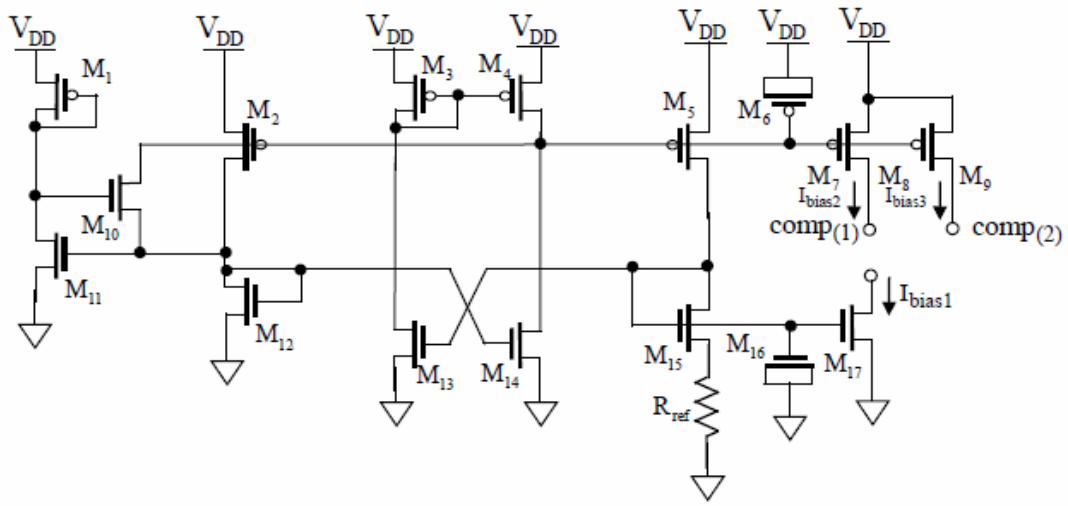

Fig. 4. Bias circuit diagram for current references.

operate on independent supply voltage and temperature. Also, the oscillation frequency can be controlled by I_B, V_{REF_H}, and V_{REF_L}.

The comparator circuit shown in Fig. 3 can be configured as a differential and common source amplifier.

This comparator generates an oscillation waveform. The oscillation frequency can be determined from the difference between the reference voltages. The voltage difference should stay at 0.5V only and it should be independent of the changes or reference voltage variation value. Whenever there are changes in the supply voltage, the voltage difference produced makes the discharging time a constant of the capacitor; thereby, the operating frequency of the oscillator is the same over a wide range of supply voltages, which are V_{REF_H} and V_{REF_L}, so the operating frequency of the oscillator is in the same range as that between supply voltages. The bias circuit shown in Fig. 4 is configured as a beta-multiplier.

3. Experimental Data

The performance of the RC oscillator circuit, as shown in Fig. 1, was analyzed by comparing it against a simulated result using Spectre in the fabricated chip's test. The chip is fabricated with a 0.18μm CMOS process from Magna/SKhynix. The values of the device are $C_1 = C_2 = 18$ pF, bias current $I_B = 10$ uA, supply voltage $V_{DD} = 3.3$ V, $V_{REF\_H} = 2.5$ V, and V_{REF_L}=2.

Fig. 5 shows a simulated result for the oscillation frequency of the RC oscillator. The upper, middle, and lower waveforms are V_{C2}, V_{C1}, and the Q terminal, respectively. This result shows that RC oscillator operation is the same, theoretically.

Fig. 6 shows measured waveforms of the fabricated chip for the circuits shown in Fig. 1. The upper and lower waveforms are V_{C2} and the Q terminal, respectively. The chip test results show that oscillation frequency and power dissipation are 500 kHz and 5.48mW, respectively, at a supply voltage of 3.3V. The chip area is 0.021mm^2.

Fig. 7 shows the insensitivity testing between the

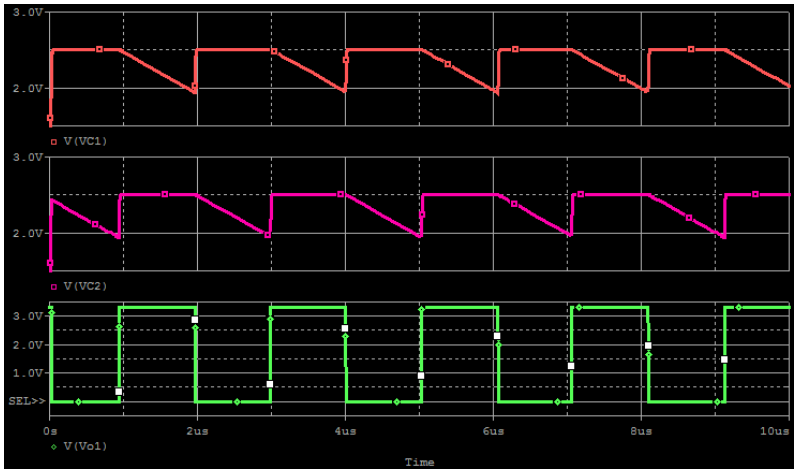

Fig. 5. Simulation result of the proposed oscillator shown in Fig. 1.

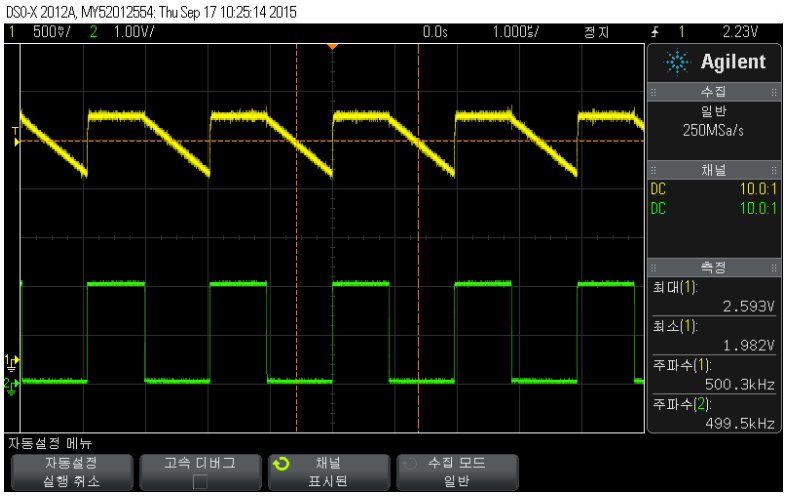

Fig. 6. Measurement waveforms of the fabricated chip for the circuits shown in Fig. 1.

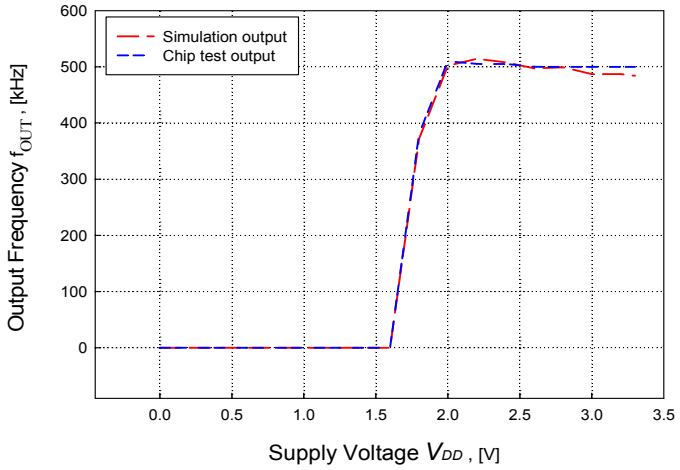

Fig. 7. V_{DD} insensitivity testing results of the Simulated and Chip test output.

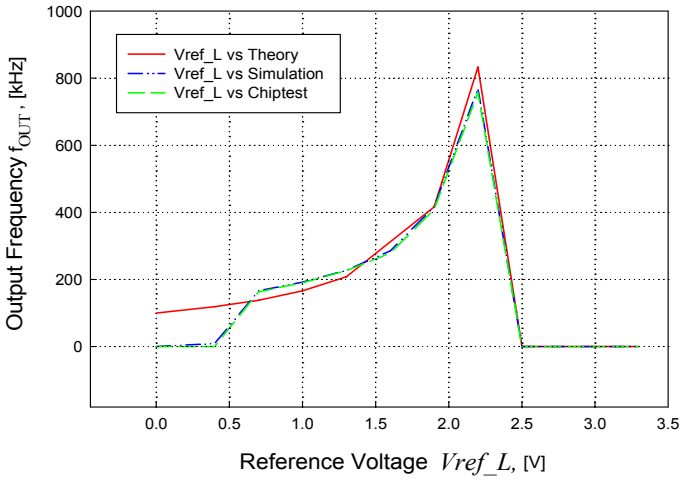

Fig. 8. Comparison of voltage variation of Vref_L level between Theoretical, Simulation and Chiptest frequency result.

simulated and chip test results. It shows that the proposed oscillator will not operate if the $V_{DD} < 2V$ and when V_{DD} is beyond 2V, the frequency is independent on changing supply voltage, this occur on both for simulation and chip testing. In Fig. 8 shows the comparison between the theoretical, simulation and chip testing frequency results during the variation of V_{REF_L}. In setting the comparator circuit in operating region, the V_{REF_L} should be between

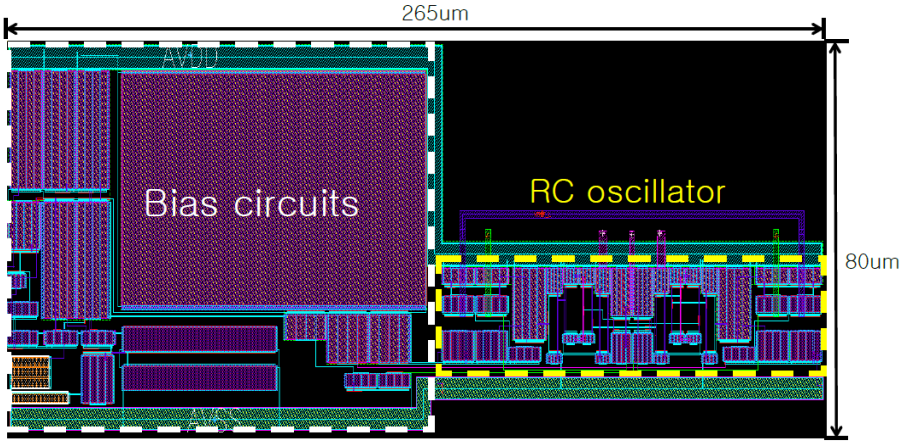

Fig. 9. Layout plot of the proposed RC oscillator.

0.6 to 2.4 V while V_{REF_H} should always be in 2.5V. As it shown in Fig.8, the output frequencies are almost the same between theoretical, simulated and in chip testing.

In Eq. (4) shows theoretically the value of C_1 and C_2 should be 20 pF to get 500 kHz output frequency. However, because of the existence of the parasitic capacitor (*i.e.* almost 2 pF), it affects the simulation results during experiment. Therefore during simulation and in chip testing, the necessary capacitor value should be in 18 pF because of this phenomenon.

4. Conclusion

In this paper, the proposed circuit is compared with a conventional oscillator circuit, and was verified with a stable output frequency. However, an additional circuit is needed to internally adjust the reference voltage that is applied from an exterior source. The proposed RC oscillator circuit design was simulated using a Magna/ SKhynix 0.18μm CMOS process. The chip was fabricated, and the operational principle was validated.

In the future study, the designed comparator should have high slow rate, speed, frequency and bias circuit (reference voltage and current) insensitive to temperature and supply voltage. Also, the designed RC oscillator should consider temperature insensitivity and supply voltage to compensate for the changes in temperature affecting passive elements, such as the capacitor.

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