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Analysis on Self-Heating Effect in 7 nm Node Bulk FinFET Device

Sung-Won Yoo[1], Hyunsuk Kim[1], Myounggon Kang[2], and Hyungcheol Shin[1,*]

***Abstract*—The analyses on self-heating effect in 7 nm node non-rectangular Bulk FinFET device were performed using 3D device simulation with consideration to contact via and pad. From self-heating effect simulation, the position where the maximum lattice temperature occurs in Bulk FinFET device was investigated. Through the comparison of thermal resistance at each node, main heat transfer path in Bulk FinFET device can be determined. Self-heating effect with device parameter and operation temperature was also analyzed and compared. In addition, the impact of interconnects which are connected between the device on self-heating effect was investigated.**

***Index Terms*—Bulk FinFET, self-heating effect, thermal conductivity R_{th}, lattice temperature**

I. INTRODUCTION

Self-heating effect (SHE) arises from the joule heating by carrier-to-lattice scattering [1, 2]. This effect can cause the performance degradation of operating devices. Especially, 3D devices such as FinFETs have lower thermal conductivity due to inefficient heat transfer caused by narrow conduction path compared to the planar MOSFET devices. This results in poor electro-thermal characteristics although 3D devices have better electrostatic performance than conventional planar devices [3, 4] due to short channel effect (SCE) suppression. Thus far, the studies on SHE of silicon-on-insulator (SOI) FinFETs due to their inferior heat transfer caused by low thermal conductivity of SiO_2 have mainly been conducted by many groups [5, 6]. However, as device is extremely scaled under 10 nm node, SHE on bulk FinFET becomes important since the thermal conductivity in narrow structure becomes much smaller as device is continuously scaling [7-9].

In this paper, SHE in 7 nm node non-rectangular Bulk FinFET was analyzed using 3D device simulation with consideration to contact via and pad. SHE with device parameter variation and operation temperature was compared and analyzed. In addition, the impacts of interconnects connected between the devices were analyzed in order to confirm how they work as heat transfer path.

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[1] Department of Electrical and Computer Engineering and the Inter-university Semiconductor Research Center (ISRC), Seoul National University, Seoul 141-744, Republic of Korea.
[2] Korea National University of Transportation, Department of Electronics Engineering, 50 Daehak-ro, Chungju-City, Chungbuk, 380-702, Republic of Korea
E-mail : ronaldo86@snu.ac.kr and hcshin@snu.ac.kr

II. DEVICE STRUCTURE AND SIMULATION SET-UP

In this paper, Sentaurus device simulator was used for device simulation. Fig. 1(a) shows the Fin cross section view in 7 nm node non-rectangular Bulk FinFET device. Fig. 1(b) also shows the cross section view of non-rectangular Bulk FinFET device along the channel direction. In addition, Fig. 1(c) shows the total structure for self-heating simulation including metal contact via and pad. The entire structure is surrounded by SiO_2. The device parameters are based on ITRS 2013 roadmap for Low Power (LP) mode. Tungsten is assumed for the material of contact via, whereas copper is assumed for

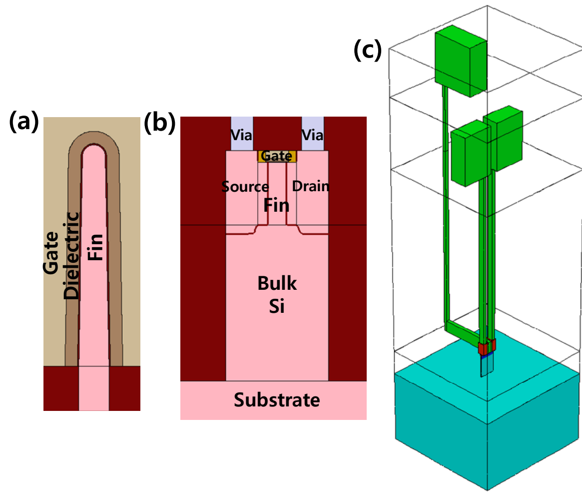

Fig. 1. (a) Fin Cross section view, (b) cross section view along the channel direction in 7 nm node Bulk FinFET device, (c) total structure for self-heating simulation including metal contact via and pad.

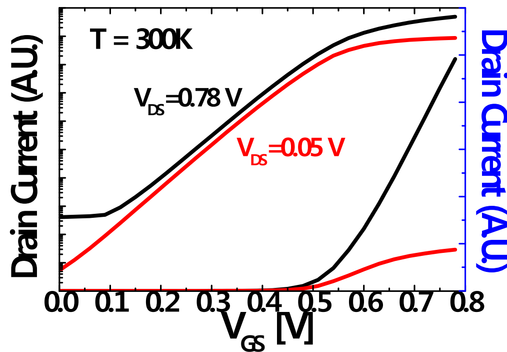

Fig. 2. Transfer curves (I_D-V_{GS}) of 7 nm node Bulk FinFET device at two V_{DS} values. DIBL value is extracted to 37.0 mV/V.

contact pad. In this simulation, Hydrodynamics charge balance model was used in order to consider local lattice and carrier temperature. And, thermal boundary condition at each node (gate, source, drain, and substrate) was specified from surface resistance. Finally, thermal resistance at various interface was also considered in this simulation. Thermal conductivity values at narrow Fin, S/D region and Bulk Si are 0.25, 0.62, 1.5 W/K·cm, respectively [1]. Fig. 2 plots the transfer curves (I_D-V_{GS}) of 7 nm node Bulk FinFET device at two V_{DS} values. From this figure, drain induced barrier lowering (DIBL) value is extracted to 37.0 mV/V.

Fig. 3(a) shows the contour of lattice temperature (T_L) in the cross section of 7 nm node Bulk FinFET device sliced at the middle of the Fin when the device is

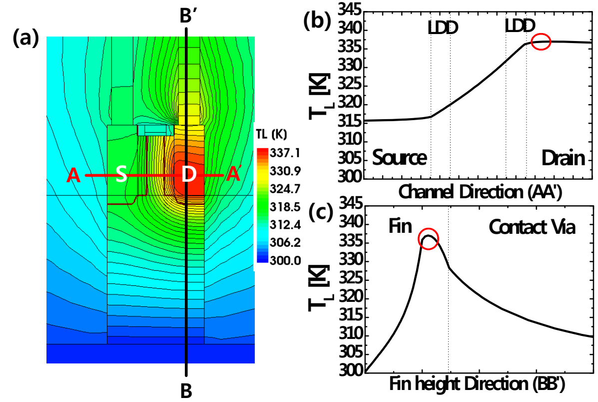

Fig. 3. (a) The contour of lattice temperature in the cross section of 7 nm node Bulk FinFET device, and lattice temperature along the (b) channel direction (*AA'*), (c) Fin height direction (*BB'*).

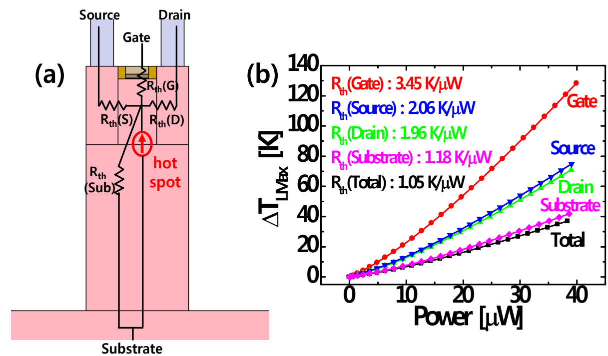

Fig. 4. (a) Equivalent thermal circuit of Bulk FinFET device, (b) temperature increase of hot spot region versus dissipated power.

operated at 300 K. In this simulation, the T_L of hot spot is 337.1 K. Fig. 3(b) and (c) show the T_L along the channel (*AA'*) and Fin height direction (*BB'*), respectively. It is shown that the hot spot which indicates the region where the T_L is maximum exists in the drain & Fin bottom region [7]. This result can be explained as follows. The heat generated by joule heating is largest in lightly doped drain (LDD)/Drain boundary. And, the majority of heat generated at this region flows to the region having larger thermal conductivity (tungsten contact via and bulk Si). On the other hand, drain & Fin bottom region surrounded by lower thermal conductivity region (S/D Si, SiO_2) has much lower heat flux. This means that the large portion of heat remains in this region, which results in higher T_L.

III. Results and Discussion

Fig. 4(a) shows the equivalent thermal circuit of Bulk

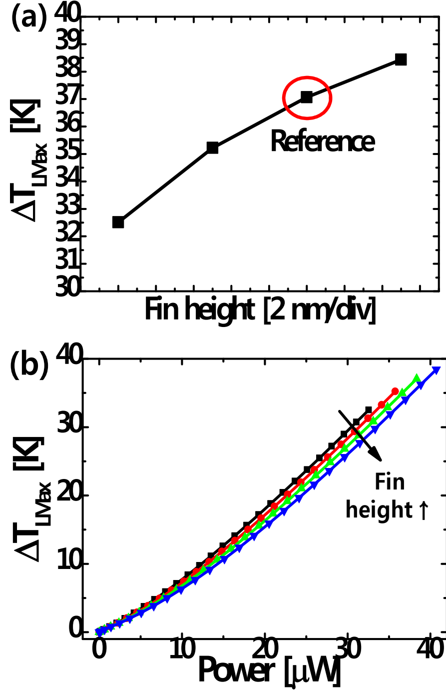

Fig. 5. (a) The maximum lattice temperature increase (ΔT_{LMax}) with Fin height, (b) ΔT_{LMax} versus dissipated power at various Fin height.

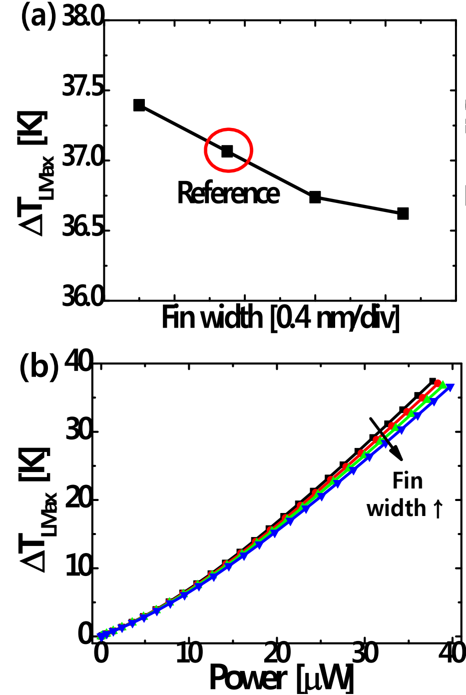

Fig. 6. (a) The maximum lattice temperature increase (ΔT_{LMax}) with Fin width, (b) ΔT_{LMax} versus dissipated power at various Fin width.

FinFET. In the equivalent thermal circuit, there are five nodes which are located at the gate, drain, source, substrate, and hot spot. Assuming that the heat source is located at the hot spot, all the heat flows are modeled by R_{th}'s between the hot spot and the other four nodes [8]. Fig. 4(b) shows the temperature increase of hot spot versus power dissipated in the Bulk FinFET device. Each thermal resistance (R_{th}) can be extracted from the linear slope of the increase of lattice temperature versus power assuming the limited heat path [8]. This figure indicates R_{th} of gate is the largest, whereas R_{th} of substrate is the smallest. This means that the largest portion of heat caused by joule heating flows through the substrate. Fig. 5(a) shows the maximum lattice temperature increase (ΔT_{LMax}) with Fin height at V_{GS}=V_{DS}=0.78 V. As shown in Fig. 5(a), ΔT_{LMax} increases with Fin height since more joule heating is generated because of larger drain current by larger effective Fin width. Fig. 5(b) also shows the ΔT_{LMax} versus dissipated power at various Fin height. Although ΔT_{LMax} increases with Fin height, R_{th} decreases with Fin height due to decrease of thermal conductivity caused by the longer heat transfer path [9].

Fig. 6(a) shows the ΔT_{LMax} decreases with Fin width due to the less joule heating V_{GS}=V_{DS}=0.78 V. Fig. 6(b) also shows the ΔT_{LMax} versus dissipated power at various Fin width. From this figure, R_{th} decreases with Fin width due to decrease of thermal conductivity caused by the broader heat transfer area.

Fig. 7(a) shows the maximum lattive temperature increase (ΔT_{LMax}) versus operation temperature V_{GS}=V_{DS}= 0.78 V. As expected, ΔT_{Lmax} increases with increasing T_L. Fig. 7(b) also shows the increase in ΔT_{Lmax} versus dissipated power at various operation temperature (300, 325, 350, and 375 K). The extracted R_{th} value at various temperatures is indicated in the inset of Fig. 7(b). The R_{th} value increases with increasing T_L (8% increase from 300 K to 375 K). This result comes from the decrease on thermal conductivity of silicon with temperature.

The impact of interconnection as well as single Bulk FinFET device on SHE is simulated and analyzed. Fig. 8 shows the contour of T_L when one transistor is turned on and another transistor is turned off. The temperature of hot spot is 329.3 K which is smaller than that of hot spot in single Bulk FinFET device (337.1 K). This result is due to the flow of heat generated by joule heating through interconnection between two devices as shown in Fig. 8(b) and (c) [8].

Fig. 9 shows the contour of T_L when two transistors

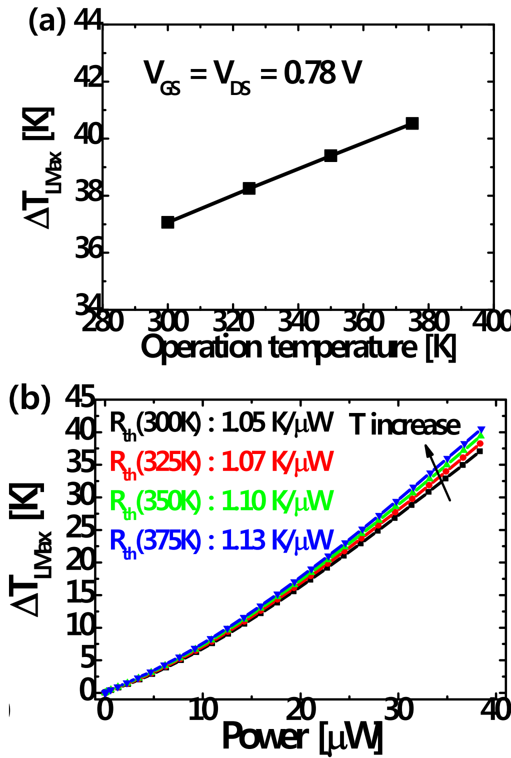

Fig. 7. (a) Maximum temperature increase (ΔT_{LMax}) at hot spot region at various temperature, (b) ΔT_{LMax} at hot spot region versus dissipated power at various temperature.

are connected in series. The temperature of hot spot is 320.4 K which is much smaller than that of hot spot in single Bulk FinFET device (337.1 K). The result comes from the fact that voltage applied on transistor 1 is approximately 0.59 V which is smaller than supply voltage (0.78 V) since the transistor 2 acts as resistor which results in voltage drop across the transistor 2.

IV. CONCLUSION

Self-heating effect in 7 nm node non-rectangular Bulk FinFET was analyzed using 3D device simulation with consideration to contact via and pad. The hot spot exists in the drain & Fin bottom region. Substrate is determined to be the main heat transfer path through the comparison of extracted R_{th} value at each node. Self-heating effect with device parameter and operation temperature was analyzed. In addition, it was confirmed that the impact of interconnects connected between the device is to reduce hot spot temperature by providing the heat transfer path.

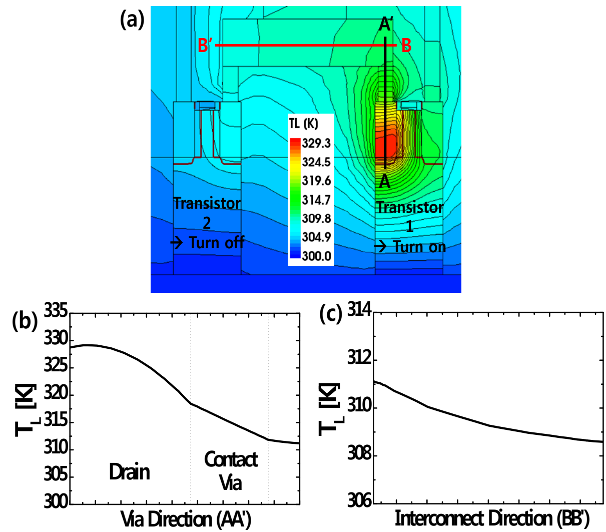

Fig. 8. (a) The contour of lattice temperature (T_L) when one transistor is turned on and another transistor is turned off, the TL along the (b) via direction (*AA'*), (c) interconnect direction (*BB'*).

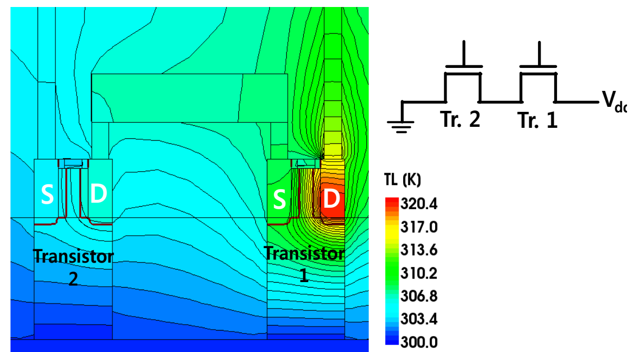

Fig. 9. The contour of lattice temperature (T_L) when two transistors are connected in series.

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Sung-Won Yoo was born in Seoul, Korea, in 1986. He received the B.S. in electrical engineering from Hanyang University, Seoul, Korea, in 2009. He received the M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 2011. He is working toward the Ph. D. degree in electrical engineering and computer science at Seoul National University, Seoul, Korea. His research interests include the device random noise and reliability analysis in DRAM cell and very-scaled Logic devices.

Hyun Suk Kim received the B.S. degree in School of Electrical Engineering from Ajou University, Suwon, Korea in 2014. He is currently working as a Master candidate in Seoul National University (SNU), Seoul, Korea. His current research interests include FinFET simulation and modeling.

Myounggon Kang (S'10) received the Ph.D. degree in the Department of Electrical Engineering, Seoul National University, Seoul, Korea in 2012. From 2005 to 2015, he had worked at Samsung Electronic Company. Currently, he is working at Korea National University of Transportation.

Hyungcheol Shin(S'92–M'93–SM'00) received the B.S. (magna cum laude) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1993. From 1994 to 1996, he was a Senior Device Engineer with Motorola Advanced Custom Technologies. In 1996, he was with the Department of Electrical Engineering and Computer Sciences, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. During his sabbatical leave from 2001 to 2002, he was a Staff Scientist with Berkana Wireless, Inc., San Jose, CA, where he was in charge of CMOS RF modeling. Since 2003, he has been with the School of Electrical Engineering and Computer Science, Seoul National University. He has published over 500 technical papers in international journals and conference proceedings. His current research interests Flash Memory, DRAM cell transistor, Nano-CMOS, CMOS RF, and noise. Prof. Shin was a committee member of the International Electron Devices Meeting. He also has served as a committee member of several international conferences, including the International Workshop on Compact Modeling and SSDM, and as a committee member of the IEEE EDS Graduate Student Fellowship. He is a Lifetime Member of the Institute of Electronics Engineers of Korea (IEEK). He received the Excellent Teaching Award from the Department of Electrical Engineering and Computer Sciences, KAIST, in 1998, The Haedong Paper Award from IEEK in 1999, and the Excellent Teaching Award from Seoul National University in 2005, 2007, and 2009. He is listed in Who's Who in the World. From 2012 to 2013, he has been director of Inter-university Semiconductor Research Center (ISRC).