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3D TCAD Analysis of Hot-Carrier Degradation Mechanisms in 10 nm Node Input/Output Bulk FinFETs

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Abstract—**In this paper, we investigated the hot-carrier injection (HCI) mechanism, one of the most important reliability issues, in 10 nm node Input/Output (I/O) bulk FinFET. The FinFET has much intensive HCI damage in Fin-bottom region, while the HCI damage for planar device has relatively uniform behavior. The local damage behavior in the FinFET is due to the geometrical characteristics. Also, the HCI is significantly affected by doping profile, which could change the worst HCI bias condition. This work suggested comprehensive understanding of HCI mechanisms and the guideline of doping profile in 10 nm node I/O bulk FinFET.**

Index Terms—**Hot carrier injection, input/output devices, bulk FinFET**

I. INTRODUCTION

The continued movement to shrink the device size for higher density is leading to an increase in the internal electric fields of MOS devices. The increased electric field is directly connected to the degradation of Si-SiO_2 interface near the drain junctions due to HCI [1]. Specially, HCI is one of the most important reliability issues on I/O devices due to the larger operation voltage [2-4]. The basic role of the I/O devices is to shift the core level voltage up to I/O level voltage (the operation voltage of the external device) [5].

The operation voltage for the I/O device is generally much higher than the voltage for core device, which is up to 3.3 V [6].

Conventionally, HCI degradation has been indirectly evaluated through maximum substrate current ($V_G \sim V_D/2$) because gate current level is too low to measure, which is direct indication for interface degradation. Also, the substrate current consists of hot holes originated from impact ionization so that there is an assumption that the degradation is proportional to the impact ionization [7, 8]. However, in the recent studies, it has been observed that the lifetime of the devices does not follow the tendency of substrate current and it seems that there are two strong degradation bias conditions at ($V_G \sim V_D/2$) and ($V_G \sim V_D$) [9-11].

In this work, we focus on the gate current because it is directly proportional to the interface damage and includes the HCI current. Also, the gate current has very low level so that measuring it may be easily affected by some noise sources. Therefore, we used the 3D technology computer aided design (TCAD) simulation in order to accurately analyze the behavior of HCI and observe the HCI damage region using TCAD visual tool.

II. SIMULATION SET UP

Fig. 1 shows the structure of the I/O bulk FinFET device in 3D TCAD simulation. The channel length is 200 nm and operation voltage (V_{DD}) is 2 V. The gate oxide thickness is thick enough to stand the high level of operation voltage. The gate current contains HCI and fowler-nordheim (F-N) tunneling currents. The HCI is

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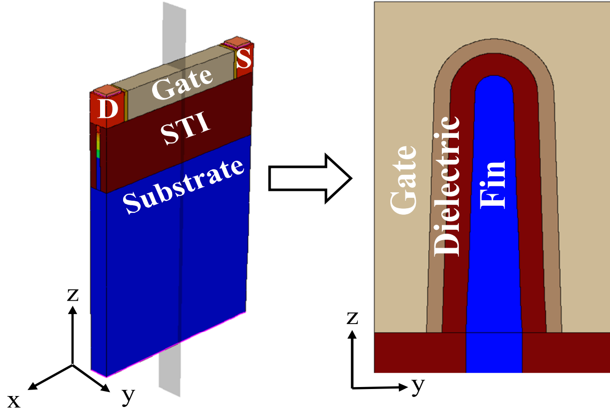

Fig. 1. Structure of the Input/Output bulk FinFET in this work.

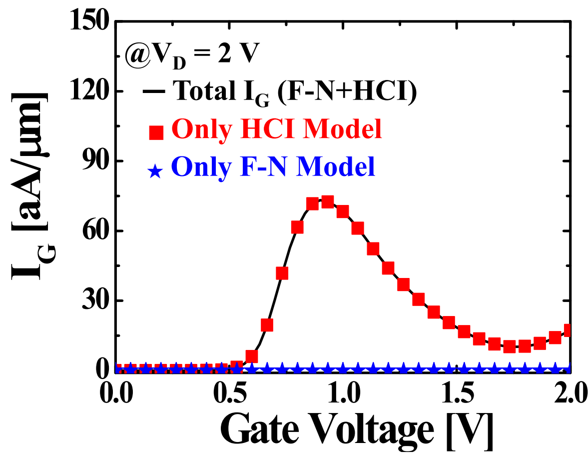

Fig. 2. The comparison of the gate currents with only HCI model, only F-N model, and both combined mechanisms according to the gate bias (at $V_D = 2$ V).

based on lucky electron model (LEM) which has been widely used [12].

Fig. 2 shows the simulation results for the gate current according to gate voltage at V_D = 2 V in 10 nm node I/O bulk FinFET. The black line indicates the gate current with both HCI and FN components. The red square symbols are the current with only HCI component (turn-off the FN mode). Oppositely, the blue star symbols are the current with only F-N component (turn-off the HCI mode). The results show that the most gate current consists of HCI. The current induced by F-N component is ignorable level against HCI component since thick gate oxide thickness suppresses F-N tunneling current. Therefore, the degradation of device is dominantly contributed by HCI mechanism. The result for the gate current shows maximum value around $V_G \sim V_D/2$. Also, the gate current rather increases in high gate bias regime

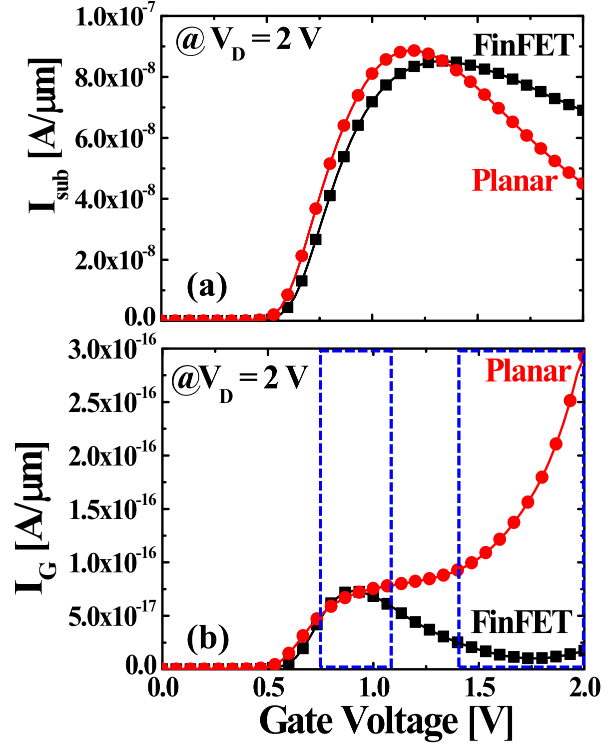

Fig. 3. (a) Substrate current, (b) gate current versus gate bias for planar and FinFET devices. Substrate current has one peak point, while gate current has two increased points.

($V_G \sim V_D$), which is much similar with the behavior for the lifetime of devices above mentioned. The total amount of injected charge by gate current is directly correlated with degradation of device. Therefore, the two points of the gate current should be importantly investigated and reducing the gate current will support the robust lifetime on I/O devices.

III. Analysis of HCI Mechanism

In order for an in-depth study on HCI mechanism in I/O bulk FinFET, we compared the simulation results of the planar device with the identical specification, such as bias condition, doping profile, W/L, gate oxide thickness and so on.

Fig. 3(a) and (b) show the substrate current and gate current of bulk FinFET and planar device according to gate bias at V_D = 2 V, respectively. The substrate currents for both devices follow conventional behavior, which has maximum substrate current value around $V_G \sim V_D/2$ and decreases in high gate bias regime ($V_G \sim V_D$) [13]. However, the gate currents are not proportional to the

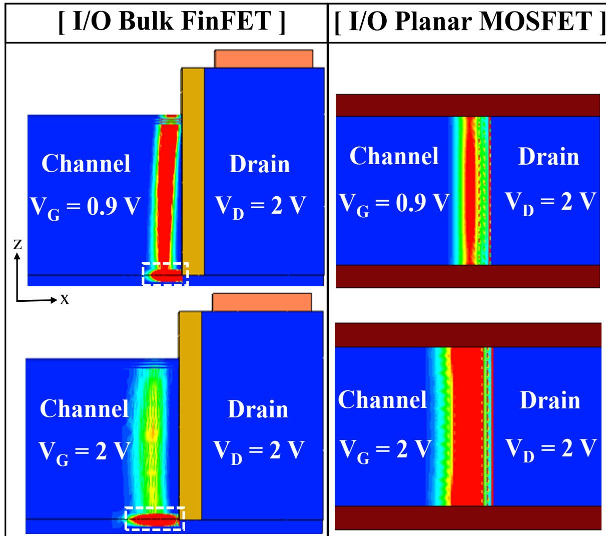

Fig. 4. Interface damage resulting from hot carrier injection for FinFET (side view) and planar (top view) at ($V_G \sim V_D/2$) and ($V_G \sim V_D$).

behavior of substrate currents as shown in Fig. 3(b). Although the behavior of gate currents is similar in both devices around $V_G \sim V_D/2$, the difference of the gate currents becomes larger in high gate bias regime. The planar device seems to be more vulnerable than I/O bulk FinFET at high V_G condition.

Fig. 4 shows the distribution of interface damage resulting from HCI for FinFET (side view) and planar device (top view). The HCI damage in both devices occurs near the drain region as widely reported [13, 14]. However, the both devices have different behavior in ($V_G \sim V_D/2$) and ($V_G \sim V_D$) regime. In case of the planar device, the distribution of HCI damage seems to be uniform behavior in ($V_G \sim V_D/2$) and ($V_G \sim V_D$) regime. The HCI damage becomes more intensified with increasing the gate bias. However, the distribution in the FinFET shows non-uniform behavior. The distribution seems to be locallized in two regions, Fin-channel and Fin-bottom. Most of gate current is injected from Fin-bottom, while the gate current comes through both Fin-channel and Fin-bottom around ($V_G \sim V_D/2$). Also, it is observed that the damage in Fin-channel region becomes weak and the damage in Fin-bottom region becomes strong as the gate bias increases.

Fig. 5 shows the extracted gate current along vertical direction (Fin-bottom to Fin-Top) and channel direction (source to drain) at V_G = 0.9 V and 2 V. Since the gate current shows strong correlation with HCI damage [see

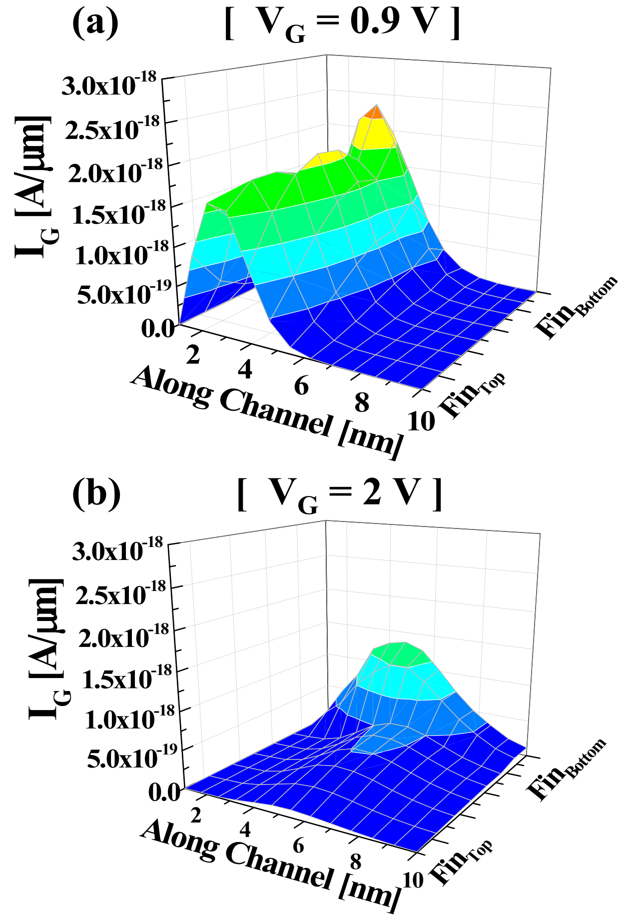

Fig. 5. 3D-mapping of gate current on bulk FinFET at (a) ($V_G \sim V_D/2$), (b) ($V_G \sim V_D$).

Fig. 2], the amount of the gate current is in inverse proportion to the device lifetime. The result shows that most of HCI damage exists within 10 nm from the channel edge in drain side and it is ignorable in the other region. Therefore, we plots the gate current along channel up to 10 nm. In low gate bias region (V_G = 0.9 V), the damage distribution shows uniform characteristic in vertical direction. However, it is clearly observed that the damage moves to Fin-bottom region in high gate bias region (V_G = 2 V).

Fig. 6 shows schematic diagrams to understand characteristics of HCI on planar and bulk FinFET devices. Fig. 6(a) shows energy band diagram along lateral direction (A–A') at ($V_G \sim V_D/2$) and ($V_G \sim V_D$). It explains the HCI mechanism in lateral direction. In low gate bias region ($V_G \sim V_D/2$), the disparity of conduction energy level between channel and drain region is large enough to generate impact ionization and HCI mechanism due to

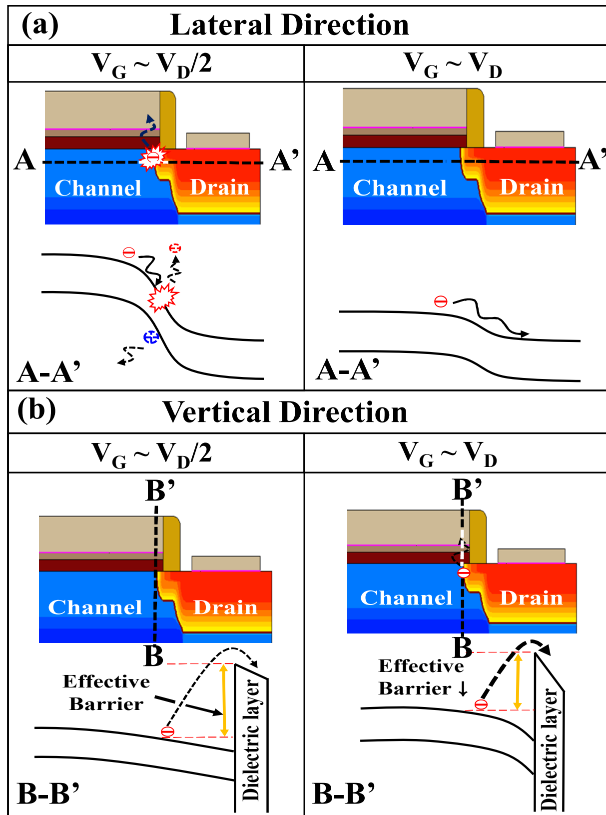

Fig. 6. Scheme of hot-carrier mechanims for lateral direction and vertical direction at ($V_G \sim V_D/2$) and ($V_G \sim V_D$).

strong lateral electric field [13]. When impact ionization occurs, the secondary holes are generated and contribute to a substrate current which is larger than gate current and enough to measure it. Therefore, the substrate current has been indirectly used to analyze degradation of the HCI. Also, the disparity becomes reduced in high gate bias region ($V_G \sim V_D$) because increased gate bias decreases the energy level in the channel side. Therefore, efficiency of HCI mechanism decreases in lateral direction. As a result, the maximum substrate current exists around ($V_G \sim V_D/2$).

On the other hand, Fig. 6(b) shows energy band diagram along vertical direction (B−B') at ($V_G \sim V_D/2$) and ($V_G \sim V_D$). It explains the HCI mechanism in vertical direction. In the vertical direction, the dominent HCI mechanism is induced by the vertical energy band bending between Si-SiO_2 surface and substrate region. As the gate bias increases, the energy band bending becomes stronger and electrons below the surface have lower effective barrier (E_{Beff}) than Si-SiO_2 off-set barrier (3.1 eV). Also, the band bending makes the higher

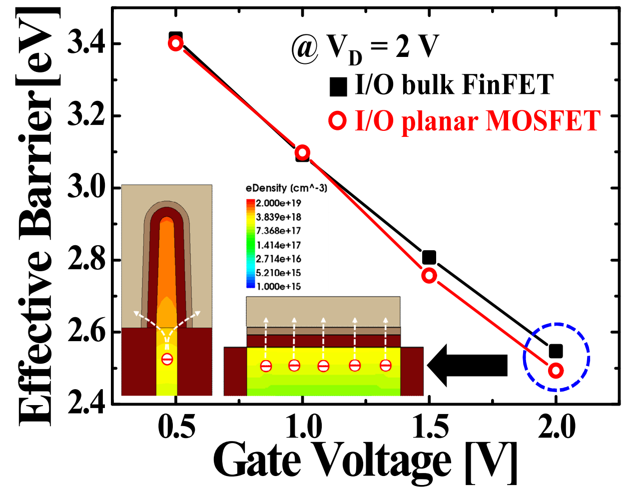

Fig. 7. Effective barrier for electrons located at 20 nm away from Fin-bottom according to V_G and scheme of the HCI path from substrate to gate.

density of carrier in Fin-bottom region. Therefore, the efficiency increases in vertical direction at high gate bias region ($V_G \sim V_D$), while efficiency of HCI mechanism is poor at low gate bias region ($V_G \sim V_D/2$). Thus, the efficiency of HCI mechanism at lateral and vertical direction is inverse behavior.

In this work, the electrons within 20 nm away from Fin-bottom region were considered where 10.5 % of electron moves to the interface without losing energy by following equation [12]:

$$P_s = \exp(-\frac{y}{\lambda}) \quad (1)$$

where P_s is the probability that the electron will travel a distance y to the interface without losing any energy and λ is the scattering mean free path. The λ = 8.9 nm was used in this work.

Fig. 7 shows the effective barrier for electrons located at 20 nm away from Fin-bottom region according to V_G. FinFET's E_{Beff} and planar's E_{Beff} are almost the same in all gate bias region. The inset schematics explain the vertical HCI pathes for FinFET and planar devices at V_G = 2 V. Although both devices have almost identical E_{Beff} lowering, it occurs in the wider region near the drain in the case of planar device. Therefore, the planar devices are much vulnerable to HCI at ($V_G \sim V_D$). The vertical HCI in FinFET is dominantly generated in Fin-bottom and the probability exponentically decreases vertical

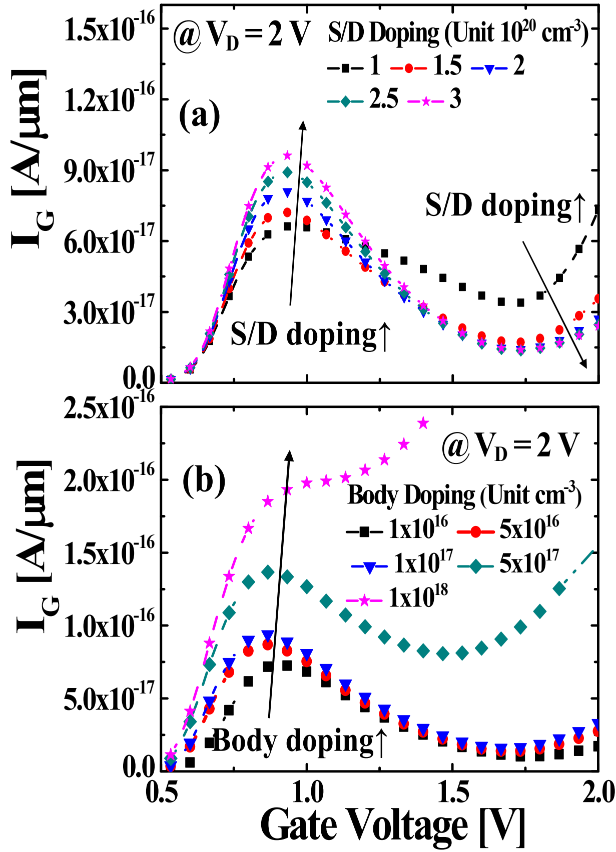

Fig. 8. Gate current behavior according to (a) source/drain doping, (b) body doping concentration.

direction as indicated in Eq. (1).

IV. Guideline for Doping Concentration

The gate current is sensitively affected by doping profile. In this section, the HCI behavior is examined according to body and source/drain doping concentration. Also, the guideline for doping profile is offered through the results.

Fig. 8(a) and (b) show gate current behavior according to source/drain doping and body doping concentration, respectively. Source/drain doping concentration was simulated ranging from 1x10^{20} cm^{-3} to 3x10^{20} cm^{-3}m. The body doping concentration was simulated ranging from 1x10^{16} cm^{-3} to 1x10^{18} cm^{-3}. The results show that the gate current behavior is different at ($V_G \sim V_D/2$) and ($V_G \sim V_D$) according to the source/drain doping concentration. This is due to the fact that lateral electric field is sensitively affected by the source/drain doping concentration. The higher source/drain doping concentration induces the

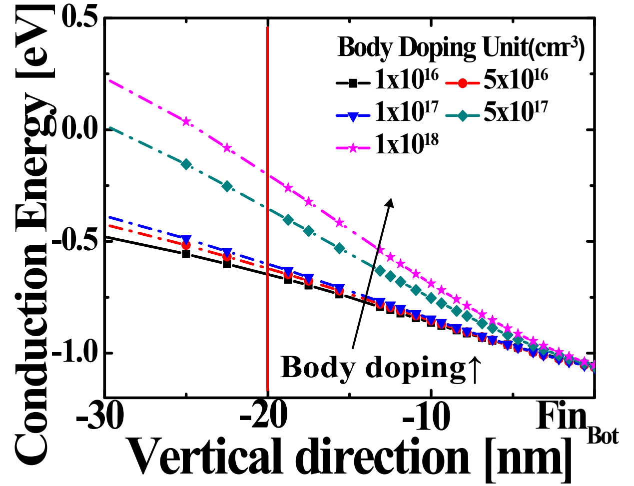

Fig. 9. Conduction band diagram through the vertical direction according to body doping concentration at V_G = 2 V. Red solid line is denoted by 20 nm position away from the Fin-bottom region.

higher lateral electric field so that the lateral HCI mechanism increases as shown in low bias condition in Fig. 8(a). However, the vertical electric field rather decreases at the same bias condition because the lateral electric field interrupts vertical band bending in Fin-bottom region. Therefore, the vertical HCI mechanism decreases as shown in high bias condition in Fig. 8(a).

Meanwhile, in case of body doping, the gate current becomes significantly larger in all gate bias region as the body doping concentration increases. Particularly, the gate current is much larger over 1x10^{18}cm^{-3} of body doping concentration where there is maximum gate current at high gate bias ($V_G \sim V_D$). It is clearly that the efficiency of HCI mechanism much increases in both gate bias region. As a result, the body doping is strongly related to the vertical HCI mechanism (refer to Fig. 9).

Fig. 9 shows the conduction band diagram along the vertical direction under the Fin-bottom according to body doping concentration. Red vertical solid line indicates the 20 nm position away from the Fin-bottom region. We use this position as a reference level to extract the effective energy barrier. Although the position over 20 nm position away from the Fin-bottom has the lower E_{Beff}, it has less carrier density and it is much hard to travel the interface without losing the energy. The energy band bending becomes larger as body doping concentration is higher at a reference line.

Fig. 10 shows E_{Beff} depending on body doping concentration at various gate bias conditions and V_D = 2

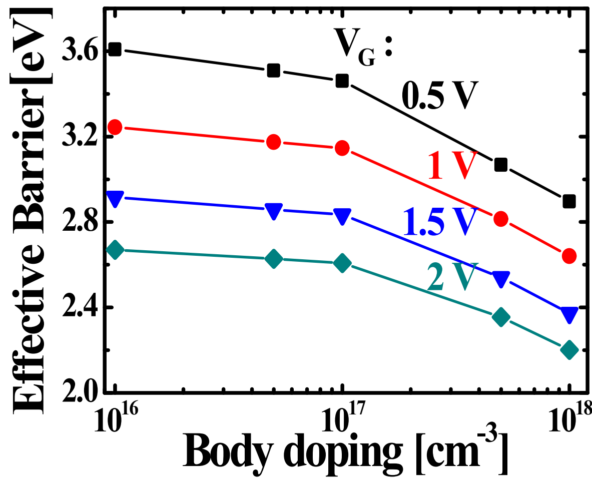

Fig. 10. Effective barrier for electrons at 20 nm away from Fin bottom according to body doping concentration.

V. The results clearly show that E_{Beff} becomes lower as body doping concentration increases in all gate bias conditions. Consequently, higher body doping concentration reduces the E_{Beff}, which boosts the gate current of the all bias conditions and it changes the worst HCI bias condition from (V_G ~ $V_D/2$) to (V_G ~ V_D) at 1×10^{18} cm^{-3} of body doping concentration [see Fig. 8(b)].

V. CONCLUSION

In this work, the HCI mechanism was studied for the 10 nm node I/O bulk FinFET and planar device. As the gate bias increases, energy band bending from Si-SiO_2 surface to substrate becomes stronger, which aggravates the reliability of devices in high gate bias condition (V_G ~ V_D). In the aspect of structure, I/O planar devices have larger HCI damage than I/O bulk FinFET devices because the E_{Beff} lowering mechanism occurs in wider region than I/O bulk FinFET devices.

In addition, the gate current is sensitively affected by doping profile. Specially, the high body doping concentration considerably boosts the gate current in whole bias condition resulting from decreased E_{Beff}. Therefore, the body doping concentration should be decreased to avoid the critical HCI degradation.

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