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Impact of Trap Position on Random Telegraph Noise in a 70-Å Nanowire Field-Effect Transistor

Hyunseul Lee[1], Karam Cho[2], Changhwan Shin[2,*], and Hyungcheol Shin[1]

***Abstract*—A 70-Å nanowire field-effect transistor (FET) for sub-10-nm CMOS technology is designed and simulated in order to investigate the impact of an oxide trap on random telegraph noise (RTN) in the device. It is observed that the drain current fluctuation ($\Delta I_D/I_D$) increases up to a maximum of 78 % due to the single electron trapping. In addition, the effect of various trap positions on the RTN in the nanowire FET is thoroughly analyzed at various drain and gate voltages. As the drain voltage increases, the peak point for the $\Delta I_D/I_D$ shifts toward the source side. The distortion in the electron carrier density and the conduction band energy when the trap is filled with an electron at various positions in the device supports these results.**

***Index Terms*—Nanowire field-effect transistor, random telegraph noise, TCAD**

I. INTRODUCTION

As the feature size of the modern field-effect transistors (FETs) is scaled down below 10 nm, the short channel effect in the electron devices is one of the most difficult technical challenges. As the critical dimensions shrink to a few nanometers, non-conventional device structures that can successfully suppress the short channel effect have been proposed. For example, double-gate FinFET [1, 2], Fully-Depleted Silicon-on-Insulator (FD-SOI) MOSFET [3, 4], and gate-all-around (GAA) MOSFET [5-10] have attracted much attention in the industry. Among them, the nanowire FET has the highest gate-to-channel capacitive coupling primarily because the channel is surrounded and controlled by the gate in all directions, and therefore, silicon nanowire architecture is the most attractive structure for sub-10-nm CMOS technology.

Because even the extremely scaled sub-10-nm device has several defects, random telegraph noise (RTN) created by an oxide trap plays an important role in analyzing device performance [11-13]. The sub-10-nm nanowire FET should be designed considering the impact of oxide traps on its performance. However, there is currently no study on the impact of RTN created by a single-trap in a 70-Å nanowire FET, to the best of authors' knowledge. In this work, the critical effect of a single trap on the performance variation of a 70-Å nanowire FET is discussed in detail, and the impact of various oxide trap positions on the drain current fluctuation is quantitatively analyzed.

II. NANOWIRE FET DESIGN AND SIMULATION APPROACH

Based on the international technology roadmap for semiconductor (ITRS), the nanowire FET design (Fig. 1(a) and (b)) for low-power sub-10-nm technology is optimized using three-dimensional (3-D) device simulations by selecting a channel length of 70 Å, a

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H. Lee and K. Cho are co-first author.
[1] Inter-universitty Semiconductor Research Center (ISRC) and School of Electrical and Computer Engineering, Seoul National University, Korea
[2] School of Electrical and Computer Engineering, University of Seoul, Korea
E-mail : cshin@uos.ac.kr (Corresponding author)

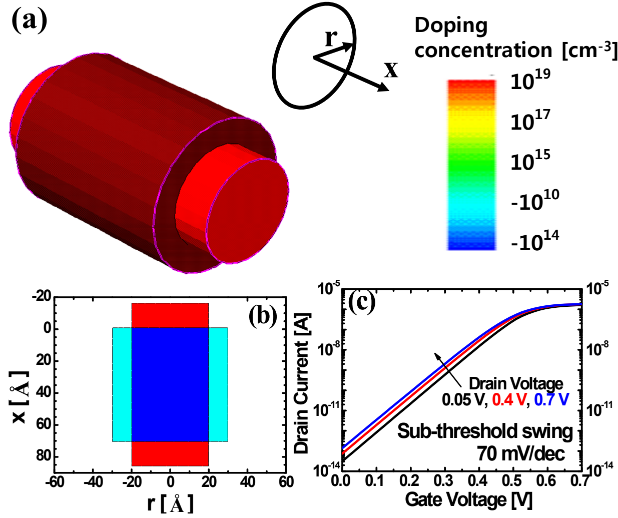

Fig. 1. (a) Three-dimensional bird's-eye view of the nanowire FET (channel length = 70 Å, radius = 20 Å), (b) Cross-sectional view of the nanowire FET, (c) Input characteristic curves (I_D-V_G) for three different drain voltages (*i.e.,* 0.05 V, 0.4 V, and 0.7 V).

radius of 20 Å, a source/drain doping concentration of 10^{20} cm^{-3} to achieve a maximum drive current for an effective oxide thickness (EOT) of 10 Å, a gate work-function of 4.62 eV, and an off-state leakage current specification of ~ 10 pA/μm at 0.7 V power supply voltage. The input characteristic curves (*i.e.*, drain current *vs.* gate voltage) for three different drain voltages are shown in Fig. 1(c) with sub-threshold slope (SS) of 70 mV/dec and an on-state saturation drive current of ~145 μA/μm.

To investigate the effect of the trap position on RTN in the nanowire FET, a single trap is placed at (r_T, x_T), where r_T indicates the distance from the Si-SiO_2 interface to the trap, and x_T represents the distance from the source edge to the trap in the x-direction. Then, the drain current fluctuation in the nanowire FET is simulated for acceptor-like trap occupancy. The quantum confinement effect in the channel is taken into account using the van Dort quantization model. Also, the mobility values are concurrently adjusted with local doping concentrations, the degree of high field saturation, and the intensity of normal electric field.

III. Results and Discussion

When a trap is filled with an electron captured from the channel, the threshold voltage in the 70-Å nanowire FET increases by ~50 mV (Fig. 2(a)), so that there exists a non-negligible amount of drain current fluctuation (ΔI_D). Fig. 2(b) shows the conduction band diagram along the channel for the empty (black) and filled (red) trap conditions for the two different trap positions of x_T =

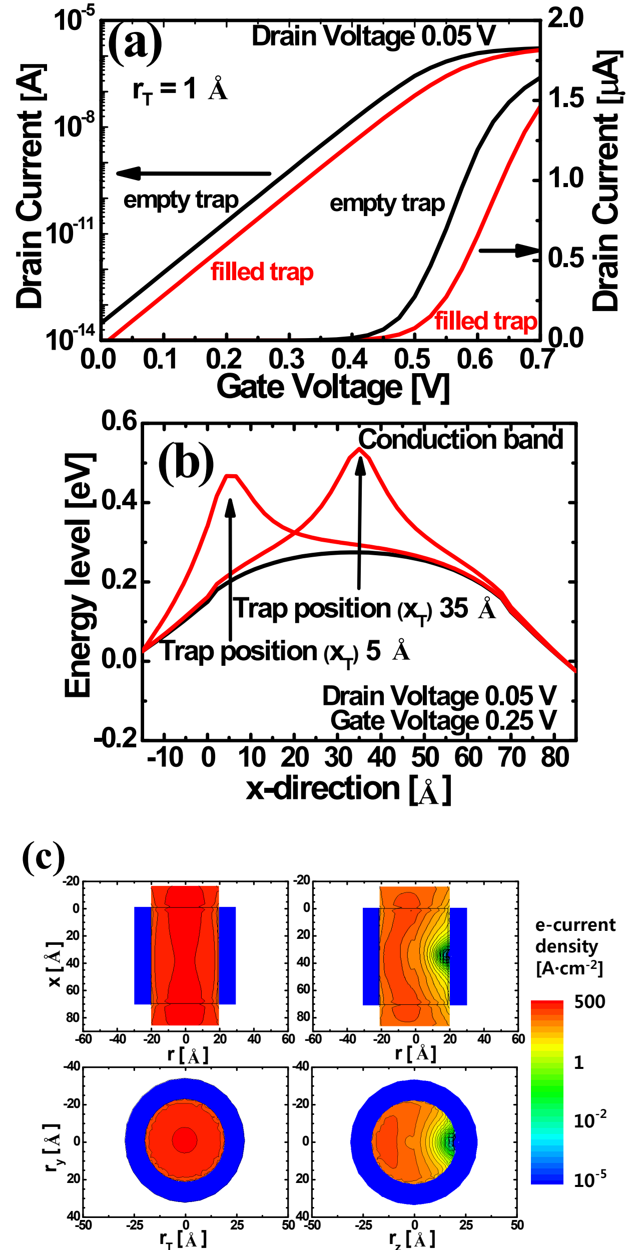

Fig. 2. (a) I_D-V_G with an empty trap (black) and a filled trap (red). Note that the trap is located in the middle of the channel (*i.e.*, x_T = 35 Å) near the Si-SiO_2 interface (*i.e.*, r_T = 1 Å), (b) Conduction band shape along the channel for the empty (black) and filled (red) trap conditions for the two different trap positions of x_T = 5 Å and 35 Å. Note that r_T = 1 Å, (c) Contour plots for the electron current density along the channel when the trap at r_T = 1 Å, x_T = 35 Å is empty (see left-hand side) or filled (see right-hand side) at V_G=0.25 V.

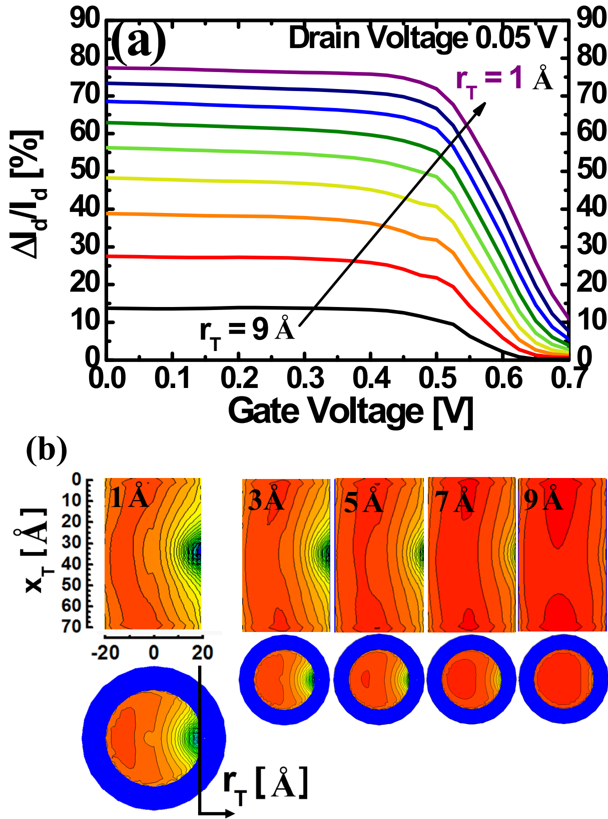

Fig. 3. (a) $\Delta I_D/I_D$ *vs.* V_G with r_T = 1 Å to 9 Å in increments of 1 Å for x_T = 35 Å, (b) Contour plot for the current density with r_T = 1 Å to 9 Å in increments of 2 Å. Note that a lower current density flows near the trap (r_T, x_T) = (1 Å, 35 Å) because of increased distortion in the channel potential by the single filled trap resulting in a locally high threshold voltage.

5 Å and 35 Å (r_T = 1 Å). The single electron captured at the trap significantly raises the conduction band energy level (see the two red-colored curves in Fig. 2(b)) by ~0.2 eV. The impact of the single trap, filled with the captured electron, on the electron current density is clearly depicted in Fig. 2(c). The two contour plots on the left-hand side in Fig. 2(c) show the electron current density with the empty trap site in the r-x (upper) and r_y-r_z (lower) planes. On the right-hand side, the two contour plots show the electron current density with the filled trap site. When present, the single trap should significantly affect the drain current in the channel. Quantitatively, $\Delta I_D/I_D$ is ~78%, as shown in Fig. 3(a).

To investigate the effect of the trap position on the drain current, r_T is first varied from 1 Å to 9 Å for x_T = 35 Å. As shown in Fig. 3(a), the drain current varies between 13 % and 78% at V_G = 0.05 V. The performance variation in the 70-Å nanowire FET intensifies when the trap is close to the channel. The proximity of the trap to the Si-SiO_2 interface significantly distorts the channel potential, resulting in the local variation of the current density (Fig. 3(b)). As is also shown in Fig. 3(a), the amplitude of RTN (*i.e.*, the drain current fluctuation) becomes large when the nanowire FET operates in the sub-threshold region. This increase indicates that the channel potential is more sensitive to the trap because the gate-to-channel controllability is relatively smaller in the sub-threshold region.

Fig. 4(a) shows the effect of trap position along the channel (i.e., in the x-direction from the source to the drain) on the drain current fluctuation at a drain voltage of 0.05 V with the trap located near the Si-SiO_2 interface at 1 Å (i.e., r_T = 1 Å). Interestingly, $\Delta I_D/I_D$ for x_T = 5 Å and 65 Å (or 15 Å and 55 Å, or 25 Å and 45 Å) are almost same because of the symmetric conduction band in the channel (black-colored line in Fig. 4(b)). However, as the drain voltage increases, the conduction band diagram becomes asymmetric (i.e., the conduction band edge is lower on the drain side than on the source side), and therefore, the peak point for $\Delta I_D/I_D$ is shifted toward the source side (Fig. 4(c)). Moreover, conduction band distortion due to the proximity of the trap to the source side (vs. the trap in the middle of the channel) occurs when the gate voltage increases from 0.25 V to 0.7 V (Fig. 4(b) and (d)). Hence, the impact of the trap position near the source and the Si-SiO_2 interface would be the most significant when the nanowire FET is operating in saturation mode.

IV. CONCLUSIONS

The effect of a single trap on the device performance in a 70-Å silicon nanowire FET has been investigated using 3-D TCAD simulations. The impact of the position of the trap on the drain current fluctuation has been quantitatively analyzed. The highest drain current variation (*i.e.*, $\Delta I_D/I_D$ ~ 78%) was observed when the trap was placed near the source side and close to Si-SiO_2 interface. Finally, the peak point for the $\Delta I_D/I_D$ was shown to shift from the middle of the channel toward the source side with an increase in the drain voltage.

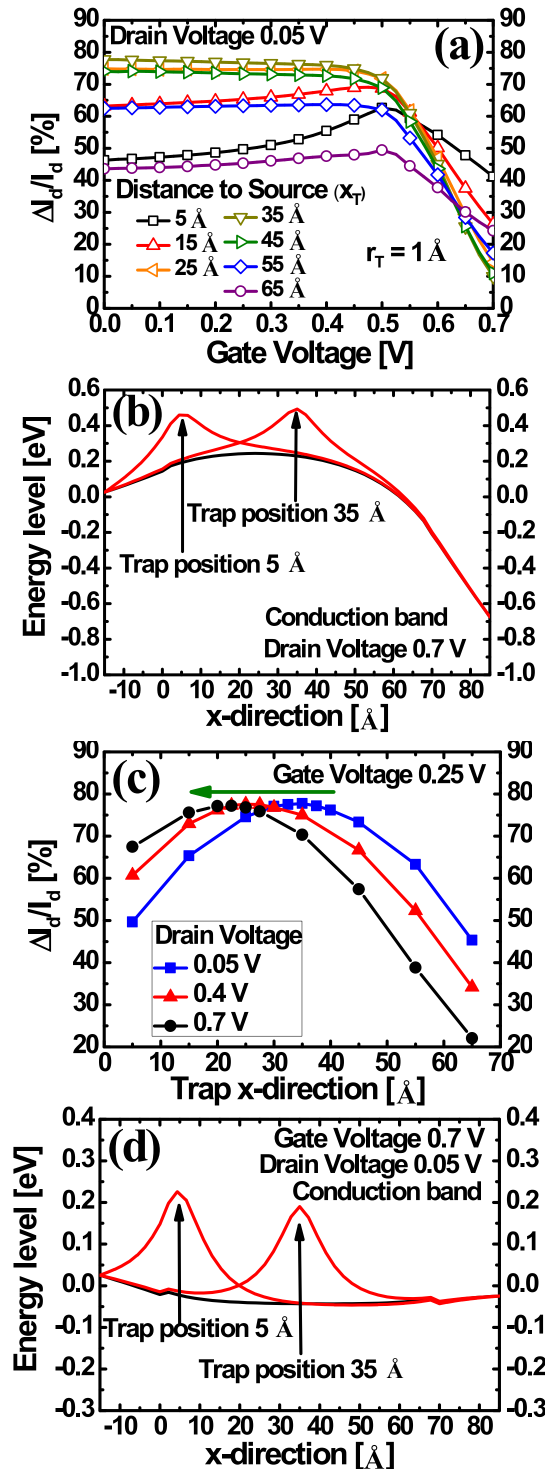

Fig. 4. (a) $\Delta I_D/I_D$ *vs.* V_G with different values of x_T from 5 Å to 65 Å in increments of 10 Å. Note that r_T is 1 Å, (b) Conduction band diagram with an empty (black) or a filled (red) trap at V_D = 0.7 V and V_G = 0.25 V. Note that two trap positions are shown within the nanowire FET, (c) $\Delta I_D/I_D$ *vs.* x_T with various drain voltages (*i.e.,* 0.05 V, 0.4 V, and 0.7 V), (d) Conduction band diagram with an empty (black) and a filled (red) trap at V_D = 0.05 V and V_G = 0.7 V.

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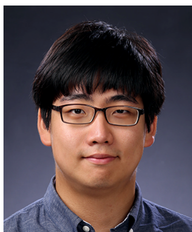

Hyunseul Lee received the B.S degree in the Department of Semiconductor Science from the Dongguk University, Seoul, Korea, in 2010 and the M.S degree in Electrical Engineering from the Seoul National University, Seoul, Korea, in 2015. His research interests include reliability in DRAM device with GIDL RTN.

Karam Cho received the B.S. degree in the Department of Physics from the University of Seoul, Seoul, Korea, in 2015 and she is currently working toward the M.S. degree in the Department of Electrical and Computer Engineering from the University of Seoul. Her research interests include steep-switching CMOS emerging devices.

Changhwan Shin received the B.S. degree (top honors) in Electrical Engineering from Korea University, Seoul, Korea, in 2006 and the Ph.D. degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 2011. In 2011, he joined the Silicon Technology Group, Xilinx Inc., San Jose, CA, as a Senior Process/Device Engineer. In 2012, he joined the Faculty of the University of Seoul, Seoul, Korea. His current research interests include advanced CMOS device designs and their applications to variation-robust SoC memory and logic devices, as well as CMOS extension technology and post-silicon technology. Prof. Shin was the recipient of a fellowship from the Korea Foundation for Advanced Studies (KFAS) in 2004, the General Electric Foundation Scholar Leaders Award in 2005, the Best Paper Award and the Best Student Paper Award at the IEEE International SOI Conference in 2009, and the Best Paper Award at the European Solid State Device Research Conference (ESSDERC) in 2010. He has been serving on technical committees for the IEEE International SOI conference (now, IEEE S3S conference) and the European Solid State Device Research Conference (ESSDERC).

Hyungcheol Shin received the B.S. (*magna cum laude*) and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1993. From 1994 to 1996, he was a Senior Device Engineer with Motorola Advanced Custom Technologies. In 1996, he was with the Department of Electrical Engineering and Computer Sciences, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. During his sabbatical leave from 2001 to 2002, he was a Staff Scientist with Berkeley Wireless, Inc., San Jose, CA, where he was in charge of CMOS RF modeling. Since 2003, he has been with the School of Electrical Engineering and Computer Sciences, Seoul National University. He has published over 400 technical papers in international journals and conference proceedings. He also wrote a chapter in a Japanese book on plasma charging damage and semiconductor device physics. His current research interests include nano-CMOS, Flash Memory, DRAM cell transistor, CMOS RF, and noise. Prof. Shin was a committee member of the International Electron Devices Meeting. He has also served as a committee member of several international conferences, including the International Workshop on Compact Modeling and SSDM, and as a committee member of the IEEE EDS Graduate Student Fellowship. He is a Lifetime member of the Institute of Electronics Engineers of Korea (IEEK). He received the Second Best Award from the American Vacuum Society in 1991, the Excellent Teaching Award from the Department of Electrical Engineering and Computer Sciences, KAIST, in 1998. The Haedong Paper Award from IEEK in 1999, and the Excellent Teaching Award from Seoul National University in 2005, 2007, and 2009. He is listed in *Who's Who in the World*.