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A Study on a Carrier Based PWM having Constant Common Mode Voltage and Minimized Switching Frequency in Three-level Inverter

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Abstract – In this paper, a carrier-based pulse with modulation (PWM) strategy for three-phase three-level inverter is dealt with, which can keep the common mode voltage constant with minimized switching frequency. The voltage gain and the switching frequency in overall operating ranges including overmodulation are investigated and the analytic equations are presented. Finally, the leakage current reduction effect is confirmed by carrying out simulation and experiment. It will be pointed out that the leakage current cannot be perfectly eliminated because of the dead time.

Keywords: Transformerless photovoltaic system, Three-level inverter, Carrier-based PWM, Leakage current elimination, Medium Vector PWM

1. Introduction

Transformerless photovoltaic (PV) system has many advantages such as cost and size reduction and higher efficiency over the PV system with a transformer. A common mode (CM) voltage variation between the PV panels and the ground, however, injects an additional leakage current in the inverter [1-2]. A PWM inverter used in motor drive has a similar problem with a high frequency leakage current that flows through parasitic capacitance between stator windings and a motor frame to the ground [3-4]. Such a leakage current may result in harmonics in the system as well as losses, electromagnetic interference and even electrical safety problem.

One of the most preferred methods to reduce or eliminate the leakage current is by modulation strategy because there is no need to additional hardware. In order to reduce the leakage current, the CM voltage needs to be kept as constant as possible in the adopted PWM scheme.

It was found in [5] that there exist 7 specific space vectors in three-level inverter that produce the same CM voltage, i.e., the 6 medium vectors and one of three zero vectors. Thus, if only these vectors are used to achieve a PWM strategy, the CM voltage will remain constant which leads to leakage current reduction. Such a PWM method with a constant CM voltage can be implemented based on space vector PWM (SVPWM) strategy or carrier based PWM (CBPWM) technique [6].

In [7] and [8], the SVPWMs for reducing the leakage currents in three-level inverter system are presented. In the case of SVPWM, some duty ratio equations should be used with sophisticated vector selection algorithms based on the angle of the reference space vector. However, the CBPWM has a merit such that there is no need to determine the electrical angle of the reference space vector. Moreover, the overmodulation operation is quite simple in CBPWM scheme. Under the aspects of implementation complexity and intuitive understanding, the CBPWM method is preferred to the SVPWM one.

In [9] and [10], some CBPWM techniques for three-level inverter are presented where only the aforementioned space vectors with the same CM voltage are used. The CBPWM in [9] uses single carrier and thus for convenience, it will be called single carrier based medium vector PWM (SCMVPWM) in this paper.

The SCMVPWM scheme seems to be quite simple. But it has much higher switching frequency, i.e., twice that of the conventional SVPWM in linear mode operation. As a result, the overall system efficiency will be considerably deteriorated due to the increased switching frequency. Moreover, because of dead time involved in every switching instant, the output voltage loss will be increased.

On the other hand, the CBPWM in [10] uses double carrier and it is based on specific phase identification strategy. It is named double carrier based medium vector PWM (DCMVPWM). The switching frequency in DCMVPWM is much lower than that of SCMVPWM with the same effect of constant CM voltage as in SCMVPWM. The DCMVPWM can support the true overmodulation from zero to maximum output voltages. In [10], however, only the main idea and basic features of DCMVPWM are presented along with simulation study.

In this paper, the DCMVPWM is further investigated especially focusing on the voltage gain and the switching frequency in overall operating ranges including linear mode modulation and overmodulation. DCMVPWM is compared to SCMVPWM in order to reveal the advantages of the DCMVPWM. Also, the leakage current reduction

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effect with minimized switching frequency is confirmed by carrying out simulation and the experiment.

2. The CM Voltage and the Leakage Current

Fig. 1 shows a three-phase three-level inverter system with a three-phase balanced load in order to investigate the reduction of the CM voltage variation. In the case of the grid-connected transformerless PV system, the three-phase voltage will be utility source and the inductors will be linked reactors. In motor drive system, the load can be regarded as an equivalent circuit of the motor. In Fig. 1, C_g and R_g represent the stray capacitance and the resistance of the path from P-point or N-point to ground, which become a leakage current path. The leakage current flowing through the grounded path may reach high values without any careful hardware and/or software treatments.

The condition to eliminate the leakage current is derived in [8], which is reviewed for self-integration. Fig. 2 shows the simplified circuit for driving the equation of the leakage current from N-point to the ground, where VSI denotes the three-level inverter and the three-phase voltages, v_{AN}, v_{BN}, v_{CN} are the output phase voltages with reference to the N-point. In Fig. 2, Z_f means the combined impedance of L and r_s and $Z_{leakage}$ means the combined impedance of C_g and R_g.

One can obtain the N-point voltage v_N with respect to the ground as follows

$$v_N = \frac{(v_{sa}+v_{sb}+v_{sc})-(v_{AN}+v_{BN}+v_{CN})}{3+Z_f/Z_{leakage}} \tag{1}$$

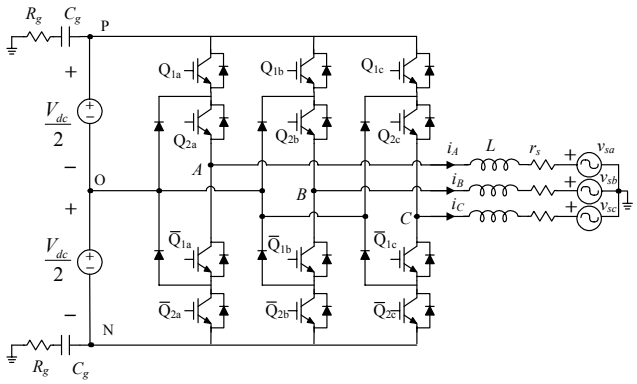

Fig. 1. The three-phase three-level inverter system

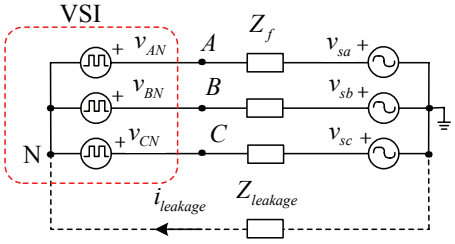

Fig. 2. The circuit for analyzing the leakage current

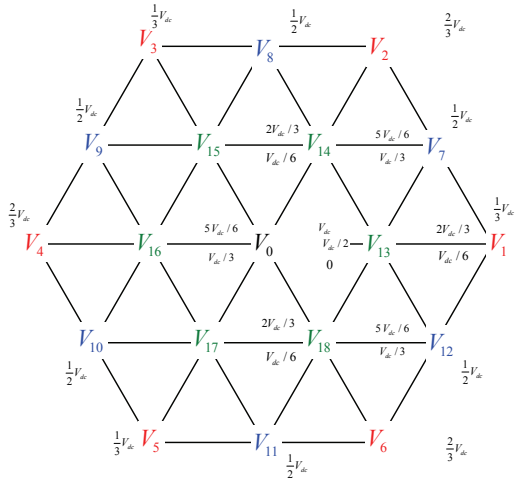

Fig. 3. The Space vectors and the corresponding CM voltages

Assuming the balanced three-phase ac voltage, i.e., $v_{sa}+v_{sb}+v_{sc}=0$, (1) becomes

$$v_N = \frac{-3Z_{leakage}}{Z_f+3Z_{leakage}} v_{CM} \tag{2}$$

where v_{CM} is the CM voltage that is defined by

$$v_{CM} = \frac{v_{AN}+v_{BN}+v_{CN}}{3} \tag{3}$$

Therefore the leakage current $i_{leakage}$ is expressed by

$$i_{leakage} = -\frac{v_N}{Z_{leakage}} = \frac{3}{Z_f+3Z_{leakage}} v_{CM} \tag{4}$$

It can be noticed from (4) that the leakage current can be adjusted by controlling v_{CM}. In order to eliminate the leakage current, the CM voltage needs to be kept constant.

Fig. 3 illustrates the space vectors and the corresponding CM voltages. The CM voltage for each switching state can be calculated by using (3). As an example, for V_1[PNN] vector $v_{AN}=V_{dc}$, $v_{BN}=0$, $v_{CN}=0$ and thus $v_{CM}=(V_{dc}+0+0)/3=V_{dc}/3$. In this case, [PNN] means that A-phase is connected to P-point, B-phase to N-point and C-phase to N-point.

Note that all the medium vectors (V_7~V_{12}), and a zero vector V_0[OOO] has the same CM voltage of $V_{dc}/2$. As a result, if only these seven vectors (V_0[OOO], V_7[PON], V_8[OPN], V_9[NPO], V_{10}[NOP], V_{11}[ONP], V_{12}[PNO]) are used to synthesize the output voltage, the CM voltage will not be changed at all, resulting in the elimination of the leakage current in the system.

3. Review of DCMVPWM

In order to drive the synthesis rule of the phase voltages,

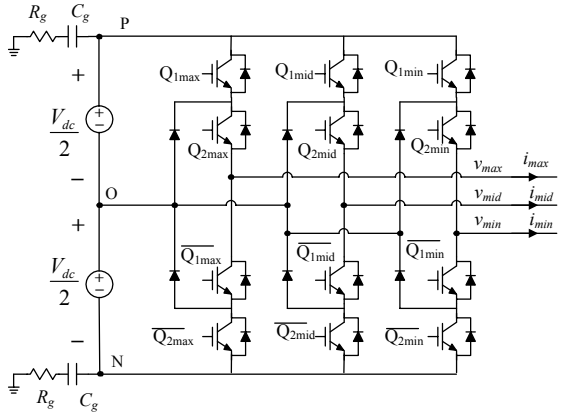

Fig. 4. Identification of the three-phase output terminals

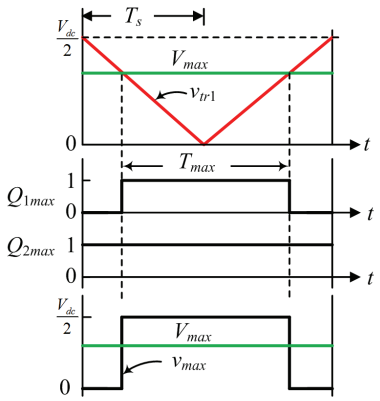

Fig. 5. Synthesis of *max*-phase voltage

the reference phase voltages should be identified according to the magnitude of the reference phase voltages, that is,

$$V_{max} = \max(V_{AOref}, V_{BOref}, V_{COref}) \quad (5)$$
$$V_{min} = \min(V_{AOref}, V_{BOref}, V_{COref}) \quad (6)$$
$$V_{mid} = \mathrm{mid}(V_{AOref}, V_{BOref}, V_{COref}) \quad (7)$$

where V_{AOref}, V_{BOref} and V_{COref} is the reference phase voltage for *A*-, *B*- and *C*-phase, respectively. It is assumed that $V_{AOref} + V_{BOref} + V_{COref} = 0$ for the balanced operation. It should be noted that $V_{max} \geq 0$ and $V_{min} \leq 0$ at any time to satisfy the zero sum condition, i.e.,

$$V_{max} + V_{mid} + V_{min} = 0 \quad (8)$$

Also, the three phases are identified by *max*-, *mid*- and *min*-phase instead of *A*-, *B*- and *C*-phase according to the reference magnitude as shown in Fig. 4.

Fig. 5 illustrates *max*-phase voltage synthesis by using P-point voltage(=V_{dc}/2) and O-point voltage(=0). The reference V_{max} is compared to a triangular signal v_{tri1} to generate the output phase voltage v_{max}. In Fig. 5, the gating signals Q_{1max} and Q_{2max} that generate the output phase voltage v_{max} are depicted. It should be noted that the N-point is never connected to the output terminal at all in *max*-phase because $V_{max} \geq 0$ at all time. Therefore the *max*-phase switching toggles between P-point and O-point. Also,

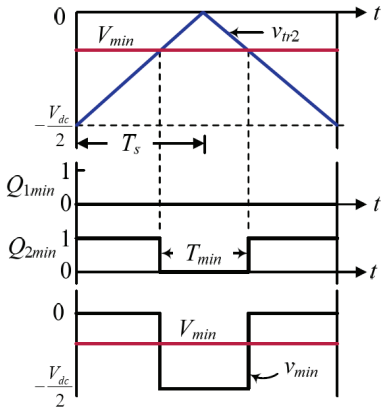

Fig. 6. Synthesis of *min*-phase voltage

the gating signal Q_{2max} is fixed to 1(i.e., turn-on state). The turn-on duration of Q_{1max}, T_{max} is expressed by

$$T_{max} = \frac{V_{max}}{V_{dc}/2} \cdot (2T_s) \quad (9)$$

Similarly, Fig. 6 shows *min*-phase voltage synthesis procedure by using N-point voltage(=$-V_{dc}$/2) and O-point voltage(=0). The reference V_{min} is compared to a triangular signal v_{tri2} to produce the output phase voltage v_{min}. In Fig. 6, the gating signals Q_{1min} and Q_{2min} to obtain the output phase voltage v_{min} are shown. In *min*-phase, there is no chance to connect the P-point to the output terminal and the *min*-phase toggles between N-point and O-point. Note that the gating signal Q_{1min} is fixed to 0(i.e., turn-off state). During the turn-off duration of Q_{2min}, T_{min}, *min*-phase output voltage becomes N-point voltage and T_{min} is given by

$$T_{\min} = \frac{|V_{\min}|}{V_{dc}/2} \cdot (2T_s) \quad (10)$$

Finally, for the *mid*-phase control, it should be noted that because of the dependency of the three phases expressed by zero sum condition of (8), the *mid*-phase voltage v_{mid} will be determined by $v_{mid} = -(v_{max} + v_{min})$ as seen in Fig. 7.

Table 1 shows *mid*-phase voltage and gating signals Q_{1mid} and Q_{2mid} according to v_{max} and v_{min} values. Thus, Q_{1mid} and Q_{2mid} can be expressed by

$$Q_{1mid} = \overline{Q_{1\max}} \cdot \overline{Q_{2\min}} \quad (11)$$
$$Q_{2mid} = \overline{Q_{1\max} \cdot Q_{2\min}} \quad (12)$$

The equations, (11) and (12) guarantee the selection of only the specific seven vectors (V_0[OOO], V_7[PON], V_8[OPN], V_9[NPO], V_{10}[NOP], V_{11}[ONP], V_{12}[PNO]).

Fig. 8 shows the overall block diagram for generating the gating signals. In summary, the gating signal is generated as follows;

1) With the reference signals (V_{AOref}, V_{BOref}, V_{COref}), V_{max} and V_{min} signals are obtained by using the sorting comparator [Eq. (5) and (7)].
2) *max*-phase control (Q_{1max}, Q_{2max}): V_{max} is compared to v_{tr1} whereby Q_{1max} is generated. Q_{2max} is intentionally fixed by high state at all time.
3) *min*-phase control (Q_{1min}, Q_{2min}): V_{min} is compared to v_{tr2} whereby Q_{2min} is obtained. Q_{1min} is intentionally fixed by low state at all time.
4) *mid*-phase control (Q_{1mid}, Q_{2mid}): The *mid*-phase gating signals are obtained by Eq. (11) and (12)
5) The mapping stage: The phase selector translates all the gating signals(Q_{1max}, Q_{2max}, Q_{1min}, Q_{2min}, Q_{1mid}, Q_{2mid}) to the actual gating signals. For example, *A*-phase gating signals (Q_{1a}, Q_{2a}) is determined by

Table 1. *mid*-phase voltage and gating signals

v_{max}	v_{min}	Q_{1max}	Q_{2max}	v_{mid}	Q_{1max}	Q_{2max}
0	0	0	1	0	0	1
0	$-\frac{V_{dc}}{2}$	0	0	$\frac{V_{dc}}{2}$	1	1
$\frac{V_{dc}}{2}$	0	1	1	$-\frac{V_{dc}}{2}$	0	0
$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	1	0	0	0	1

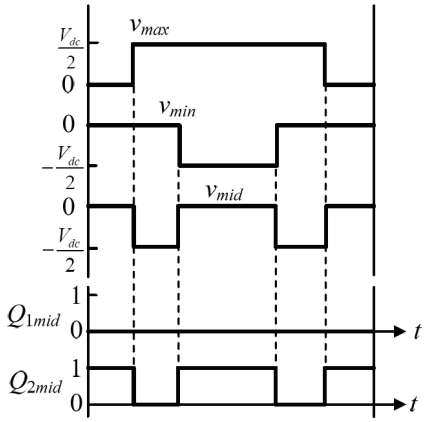

Fig. 7. Synthesis of *mid*-phase voltage

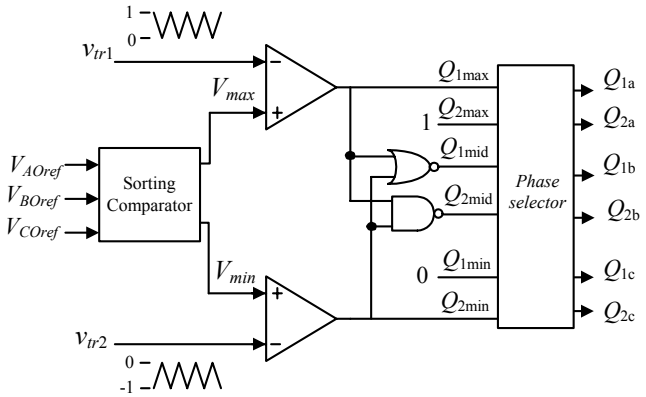

Fig. 8. Control block diagram of DCMVPWM

$$Q_{1a} = \begin{cases} Q_{1max} & if\ V_{AOref} = V_{max} \\ Q_{1min} & if\ V_{AOref} = V_{min} \\ Q_{1mid} & if\ V_{AOref} = V_{mid} \end{cases} \quad (13)$$

$$Q_{2a} = \begin{cases} Q_{2max} & if\ V_{AOref} = V_{max} \\ Q_{2min} & if\ V_{AOref} = V_{min} \\ Q_{2mid} & if\ V_{AOref} = V_{mid} \end{cases} \quad (14)$$

Fig. 9 shows the typical waveforms for the DCMVPWM with amplitude modulation index, m_i=0.8 and frequency modulation index m_f =36. As seen in Fig. 9, the gating signal Q_{1a} comes from one of Q_{1max}, Q_{1min} and Q_{1mid} at each time according to the magnitude of V_{AOref}. Also, it is found from Fig. 9 that the CM voltage is constant, i.e., V_{dc} /2.

4. Characteristics of DCMVPWM

Because the DCMVPWM is basically carrier-based scheme, it has almost the same advantages and features as in the traditional sinusoidal PWM used in the conventional two-level voltage source inverters. In this section, the characteristics of the DCMVPWM are examined.

4.1 The overmodulation capability

The overmodulation is used to increase the inverter

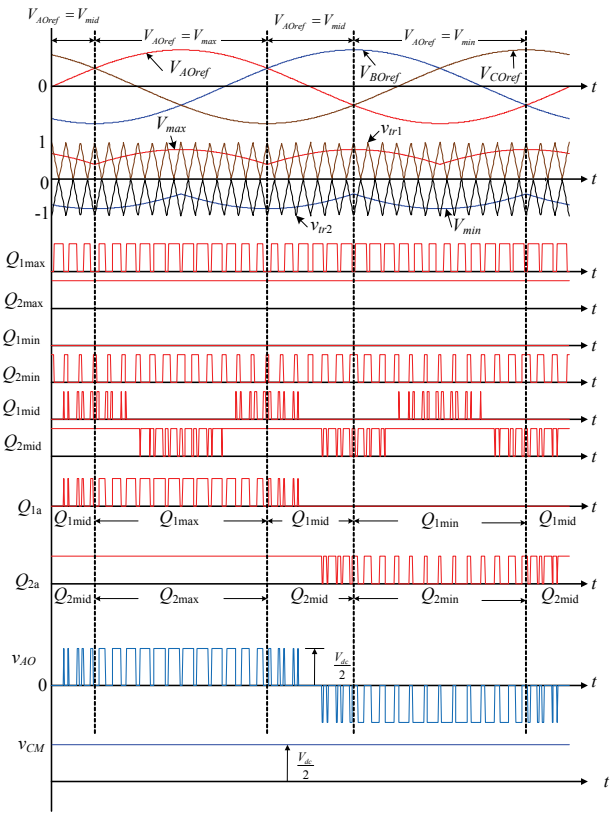

Fig. 9. Typical waveforms of the DCMVPWM

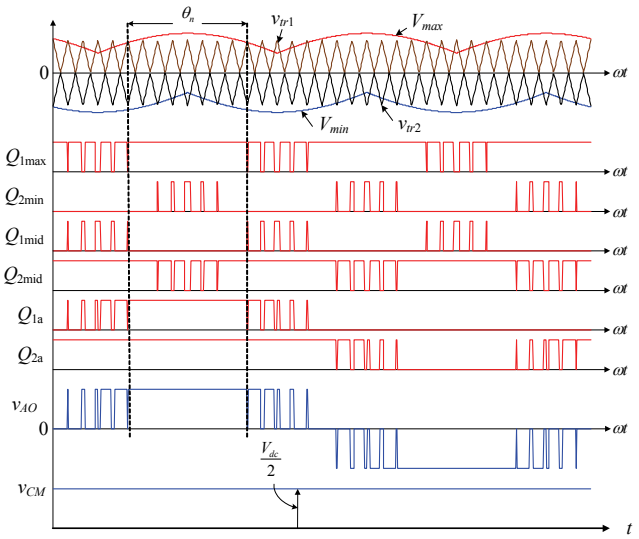

Fig. 10. Typical waveforms of the DCMVPWM in over-modulation (m_i=1.2)

output voltages beyond its maximum in linear operating region at the expense of the sacrificed output voltage waveform quality. For example, in motor drive system, when the motor is operated at enough high speed, further increase in inverter output voltage may be required to maintain the v/f ratio. Also, the overmodulation may be adopted in high power PV system consisting of several inverters in parallel, where the operating frequency is lowered and the output voltage is maximized.

Fig. 10 illustrates the typical overmodulation waveforms with modulation index of 1.2. When the modulation index(m_i) is increased beyond unity, the command signals cannot make the intersection with the carrier signals around their maximum and minimum. It should be noted that even in overmodulation operation, only the medium vectors and a zero vector V_0[OOO] are selected because of the restriction of (11) and (12) and thus the CM voltage is kept constant as seen in Fig. 10

If m_i > 2, there is no intersection between reference signals and carrier signals and thus the output phase voltage waveforms become the quasi-square wave with the four-step change, resulting in the maximum output voltage as seen in Fig. 11.

In four-step mode, the procedure to obtain A-phase gating signals (Q_{1a}, Q_{2a}) is as follows;

1) *max*-phase: because there is no intersection between V_{max} and v_{tr1} and V_{max} is always greater than v_{tr1}, Q_{1max} will be always high state. Q_{2max} is intentionally fixed by high state. Therefore, Q_{1max}=1, Q_{2max}=1.
2) *min*-phase: because there is no intersection between V_{min} and v_{tr2} and V_{min} is always less than v_{tr2}, Q_{2min} becomes always low state. Q_{1min} is given by low state. Therefore, Q_{2min}=0, Q_{1min} =0.
3) *mid*-phase: from Eq. (11) and (12), Q_{1mid} =0, Q_{2mid} =1.
4) Based on (13) and (14), Q_{1a} and Q_{2a} are determined.

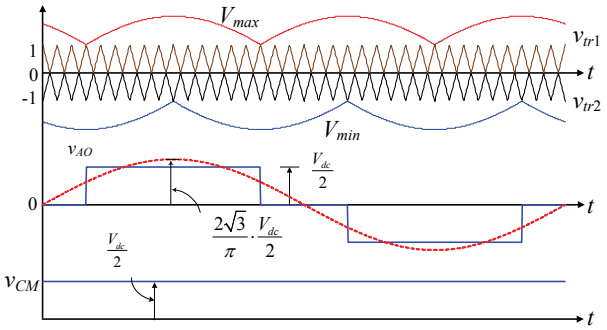

Fig. 11. The maximized four-step mode of DCMVPWM (m_i=2)

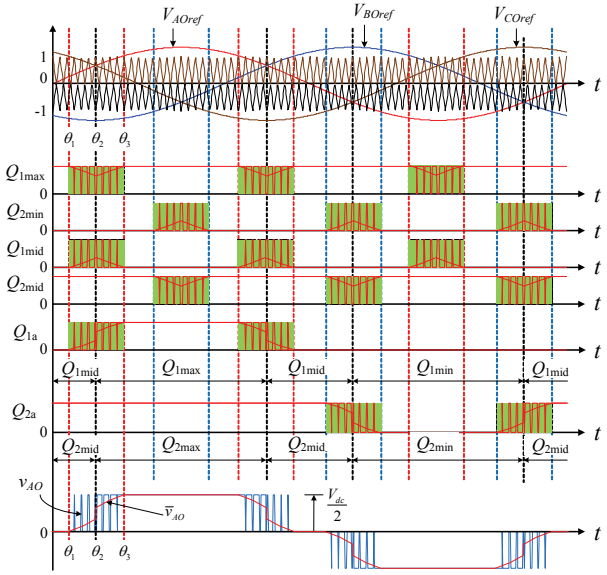

Fig. 12. Moving average of the output phase voltage over switching period in overmodulation operation

$$Q_{1a}=\begin{cases}1 & \text{if } V_{AOref}=V_{max}\\ 0 & \text{otherwise}\end{cases},\quad Q_{2a}=\begin{cases}0 & \text{if } V_{AOref}=V_{min}\\ 1 & \text{otherwise}\end{cases}$$

It is pointed out that in the DCMVPWM the m_i value from which the four-step mode begins is fixed by 2 while such m_i value is changed depending on the frequency modulation index in the SCMVPWM.

4.2 The Voltage Gain

In linear modulation operation, the output phase voltage is proportional to modulation index, m_i. The fundamental component peak value of the output phase voltage, V_{1peak} in linear mode is

$$V_{1,peak}=\left(\frac{1}{2}V_{dc}\right)m_i \quad (0\le m_i\le 1) \tag{15}$$

Fig. 12 illustrates the typical waveforms in overmodulation operation where the moving averages over switching

period are depicted with solid line superposed on each gating signals and the output voltage. In Fig. 12, the shadowed area means the intervals during which PWM operation occur.

Assuming that the carrier frequency is enough high, the electrical angles θ_1 and θ_3 are approximately expressed by

$$\theta_1 = \frac{\pi}{3} - 2\sin^{-1}\left(\frac{1}{m_i}\right) \tag{16}$$

$$\theta_3 = \sin^{-1}\left(\frac{1}{m_i}\right) \tag{17}$$

and $\theta_2 = \pi / 6$.

In Fig. 12, $\overline{v}_{AO}$ denotes the moving average of the output phase voltage, which is a quarter-wave symmetry waveform. Referring to Fig. 12, $\overline{v}_{AO}$ can be expressed by

$$\overline{v}_{AO} = \begin{cases} 0 & (0 \le \theta < \theta_1) \\ \dfrac{V_{dc}}{2} - \dfrac{V_{dc}}{2} m_i \sin\left(\theta + \dfrac{2\pi}{3}\right) & (\theta_1 \le \theta < \theta_2) \\ \dfrac{V_{dc}}{2} m_i \sin(\theta) & (\theta_2 \le \theta < \theta_3) \\ \dfrac{V_{dc}}{2} & \left(\theta_3 \le \theta < \dfrac{\pi}{2}\right) \end{cases} \tag{18}$$

By obtaining the Fourier coefficient of $\overline{v}_{AO}$, one can drive analytic expression for V_{1peak}.

$$V_{1peak} = \frac{\sqrt{3}V_{dc}}{\pi}\left[\frac{(m_i - 1)^2 + \sqrt{3(m_i^2 - 1)}}{2m_i} + \sqrt{3}\, m_i \left\{\frac{1}{2}\sin^{-1}\left(\frac{1}{m_i}\right) - \frac{\pi}{12}\right\}\right] \quad (m_i > 1) \tag{19}$$

In the DCMVPWM, the modulation index can be changed from 0 to maximum (>2.0) while the magnitude of the output voltages is continuously changed.

Fig. 13 shows the output voltage magnitude with respect to the modulation index where the output voltage magnitude curve is obtained from (15) and (19).

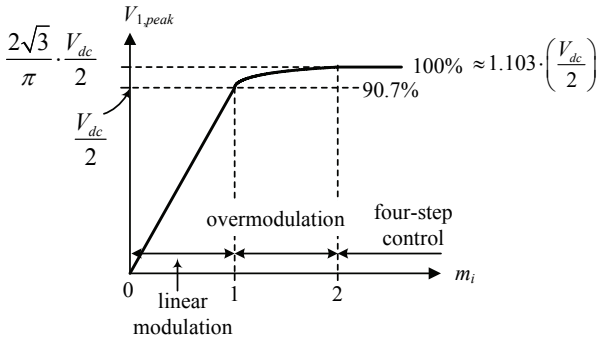

Fig. 13. The voltage gain curve of DCMVPWM

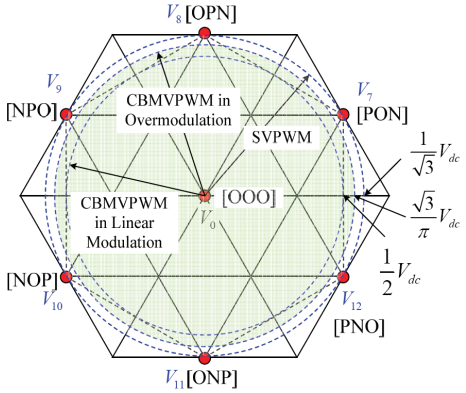

Fig. 14. Maximum output voltage of DCMVPWM

By using overmodulation, the output voltage is increased by about 10 % compared to maximum value in linear mode.

Fig. 14 illustrates the maximum output voltage of the DCMVPWM in linear and overmodulation operation. The maximum peak value of the output phase voltage in linear mode, $V_{p(Linear)}$ becomes the radius of the circle inscribed in the hexagon, which is the same magnitude as in the traditional carrier-based sinusoidal PWM.

$$V_{p(Linear)} = \frac{1}{2}V_{dc} \tag{20}$$

In the overmodulation operation, the magnitude of the fundamental component of the output phase voltage can be extended to its maximum, $V_{p(Overmod)}$.

$$V_{p(Overmod)} = \frac{\sqrt{3}}{\pi}V_{dc} \tag{21}$$

Comparing to SVPWM, the magnitudes $V_{p(Leanear)}$ and $V_{p(overmod)}$ are 86.6% and 95.5% of SVPWM respectively.

4.3 The switching frequency

In DCMVPWM, the switching states of two phases are changed at the same time as seen in Fig. 7. This implies that the switching frequency of DCMVPWM is higher than that of SVPWM.

The total number of commutations per a switching period in the three-level inverter is counted to eight. If f_c is the carrier frequency, the total number of commutations per a second becomes $8f_c$. Because the three-level inverter has 12 IGBTs, the effective averaged switching frequency f_{sw} per each IGBT switch becomes

$$f_{sw,DCMVPWM} = \frac{8f_c}{12} = \frac{2}{3}f_c \quad (0 \le m_i < 1) \tag{22}$$

Fig. 15 shows the waveform comparisons during the sector I (0^o~60^o) for the DCMVPWM, the SCMVPWM

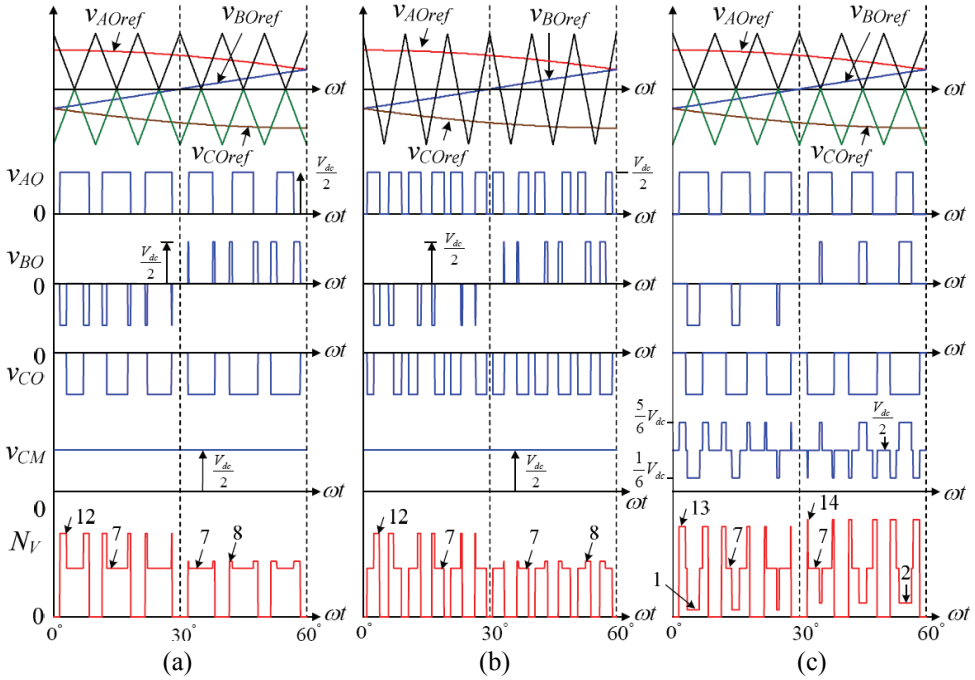

Fig. 15. Reference and carrier signals, output phase voltages, the CM voltages and the space vector numbers selected during sector I (0^o~60^o); (a) DCMVPWM, (b) SCMVPWM, (c) SVPWM

and the conventional SVPWM schemes. In Fig. 15, N_v is the space vector number selected during sector I.

It can be seen from Fig. 15 that N_v = 0, 7, 8, 12 in the DCMVPWM and SCMVPWM and thus the CM voltages are constant for both DCMVPWM and SCMVPWM. In case of SVPWM, the CM voltage fluctuates between $(1/6)V_{dc}$ and $(5/6)V_{dc}$ since N_v=0, 1, 2, 7, 13, 14. Therefore, the amount of leakage currents in DCMVPWM and SCMVPWM will be much less than that of SVPWM.

In the case of SVPWM, the total number of commutations per a second is $6f_c$ and thus the effective switching frequency will be

$$f_{sw,SVPWM} = \frac{6f_c}{12} = \frac{1}{2}f_c \quad (0 \le m_i < 1) \tag{23}$$

For the SCMVPWM, the total number of commutations per a second is $12f_c$ and thus the effective switching frequency becomes

$$f_{sw,SCMVPWM} = \frac{12f_c}{12} = f_c \quad (0 \le m_i < 1) \tag{24}$$

Regarding the effective switching frequency per a IGBT with the same carrier frequency, the SVPWM has the lowest switching frequency but it cannot produce the constant CM voltage whereas the SCMVPWM can produce the constant CM voltage but it has the highest switching frequency. On the contrary, the switch frequency of the DCMVPWM is higher than that of SVPWM by 33% but it can produce the constant CM voltage. Compared to SCMVPWM, the DCMVPWM has 33% lower switching frequency than SCMVPWM with the same effect on the CM voltage.

Notice that in Fig. 15, the output phase voltages, v_{AO} and v_{CO} in DCMVPWM and SVPWM are exactly same while only the output phase voltage, v_{BO} is different. During sector I, *B*-phase becomes *mid*-phase and thus the gating signals are modified by (11) and (12) whereas the gating signals for the *max*- and *mid*-phase are determined as in SVPWM.

In overmodulation operation, the effective switching frequency per IGBT will be decreased because of switching drops. Assuming that the carrier frequency is enough high, the interval θ_n (see Fig. 10) is approximately expressed by

$$\theta_n = \begin{cases} \pi - 2\sin^{-1}\left(\dfrac{1}{m_i}\right) & (1 < m_i < 2) \\ \dfrac{2\pi}{3} & (m_i \ge 2) \end{cases} \tag{25}$$

where the maximum value of θ_n, $\theta_{n,max}$=120°.

Therefore, using (22) and (25), the averaged switching frequency, $f_{sw,(Overmod)}$, in overmodulation region can be approximately obtained.

$$f_{sw,(Overmod)} = \begin{cases} f_c\left[\dfrac{2}{\pi}\sin^{-1}\left(\dfrac{1}{m_i}\right) - \dfrac{1}{3}\right] & (1 < m_i < 2) \\ f_o & (m_i \ge 2) \end{cases} \tag{26}$$

where f_o is the inverter output voltage frequency.

5. Simulation Results

To verify the feasibility and effectiveness of the DCMVPWM method, simulation and experiment are carried out with parameters listed in Table 2. In [2], it is mentioned that the stray capacitance C_g of PV cells has typical value of 100-200 pF whereas C_g may is increased to 9 nF for the wet panels. In this paper, C_g value of 10 nF is chosen considering worst case. Also, R_g of 1.3 Ω is chosen based on the resistance of earth wires. Because the leakage currents are not affected by the balanced three-phase utility voltages (v_{sa}, v_{sb}, v_{sc}) as described in Eq. (1), the three-phase system without the utility AC sources is considered in the simulation and experimental setup.

5.1 The linear modulation operation

Fig. 16 shows the simulation waveforms such as the *A*-phase output voltage, the line-to-line output voltage, the *A*-phase line current and the leakage current in the case of amplitude modulation index m_i=0.9. As seen in Fig. 16, the DCMVPWM is operated well to generate sinusoidal line current. The leakage current is measured at the ground to N-point path through R_g and C_g. The rms value of the leakage current is estimated to be about 50 mA.

According to the international standard IEC 602109-2, the maximum leakage current allowed is 60 mA/kW. Also, the German standard DIN VDE 0126-1-1 states that the leakage mean level of 30 mA should be disconnected with 0.3 sec [2]. The leakage current in this simulation is more or less the standard level. If the stray capacitance is reduced, the leakage current will be within the fully safe level.

Table 2. System parameters

Parameters	Value
DC-link voltage, V_{dc}	200 V
Stray capacitance, C_g	10 nF
Ground resistance, R_g	1.3 Ω
Linked reactor, L	1.5 mH
Load resistance, r_s	7.7 Ω
Carrier frequency, f_c	7.5 kHz
Dead time, t_d	2.7 μ s
Inverter frequency, f_o	60 Hz

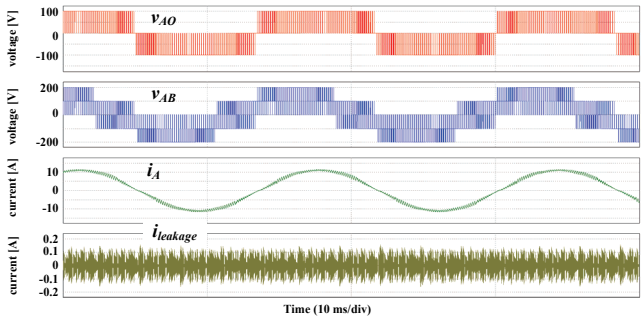

Fig. 16. The simulation waveforms when m_i=0.9; the *A*-phase output voltage, v_{AO}, the *A*-phase to *B*-phase line-to-line voltage, v_{AB}, the *A*-phase line current i_A and the leakage current $i_{leakage}$

It is true that the DCMVPWM can perfectly eliminate the leakage current owing to the constant the CM voltage. However the practical three-level inverter has the dead time for safe switching operation. During very short dead time, the CM voltage of the inverter can be deviated from its constant value. That is, because of the inevitable dead time, the leakage current cannot be completely eliminated.

Fig. 17 shows the CM voltage and the leakage current where one can see that the CM voltage is not perfectly constant but changed with pulse train pattern. The height of the pulse is about 33 V.

Fig. 18 shows the *A*-phase output voltage and the *A*-phase current for DCMVPWM and SCMVPWM cases. In Fig. 18, the moving average voltages $\overline{v}_{AO}$ are shown superposed on the corresponding v_{AO} waveforms. It can be seen that the amplitude of the $\overline{v}_{AO}$ in case of DCMVPWM is about 88 V whereas the amplitude of the $\overline{v}_{AO}$ in SCMVPWM is at most about 74 V. Because m_i=0.9, the theoretical amplitude value of $\overline{v}_{AO}$ will be 90 V. Therefore the voltage losses in the DCMVPWM and SCMVPWM are 2V and 16 V, respectively. Such voltage loss is due to the dead time. As a result, the phase current in case of SCMVPWM is smaller than DCMVPWM case due to the severe voltage loss. Comparing DCMVPWM with SCMVPWM, the switching frequency of SCMVPWM is much higher and thus the amount of the dead time is

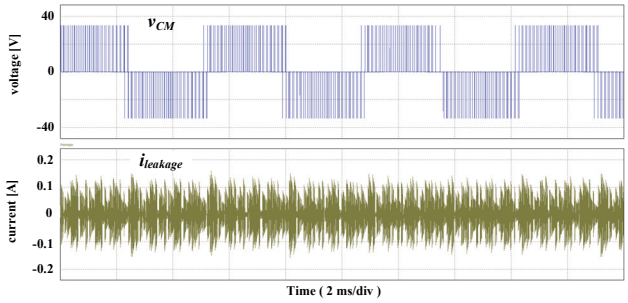

Fig. 17. The simulation waveforms when m_i = 0.9 ; the common mode voltage, v_{CM} and the leakage current $i_{leakage}$

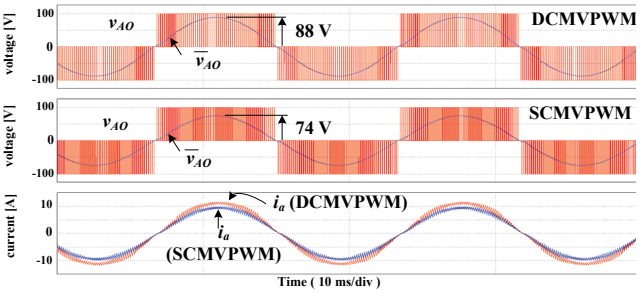

Fig. 18. The simulation waveforms when m_i=0.9 ; the *A*-phase output voltage, v_{AO} and the *A*-phase current i_a for DCMVPWM and SCMVPWM

much larger in SCMVPWM. This leads to the more voltage losses in SCMVPWM than DCMVPWM.

Fig. 19 shows the leakage currents in the case of DCMVPWM. SCMVPWM and SVPWM, respectively. It can be seen in Fig. 19 that SCMVPWM and DCMVPWM has lower leakage current level than that of SVPWM. The leakage current of DCMVPWM is slightly higher than that of SCMVPWM but such difference may be negligible because many minor factors are actually omitted and the model used in simulation is idealized for simulation convenience.

It is concluded that DCMVPWM is better than SCMVPWM because the leakage current is almost same but the voltage loss is much smaller.

5.2 The Overmodulation operation

In the case that the amplitude modulation index m_i is greater than unity, the overmodulation occurs as seen in Fig. 20.

One can notice from Fig. 20 that there exist some time duration during which any switching operation does not occur like "halt time". The higher modulation index is, the longer such a halt time is. It is observed from Fig. 20 that the CM voltage has intermittent pulse train with halt time.

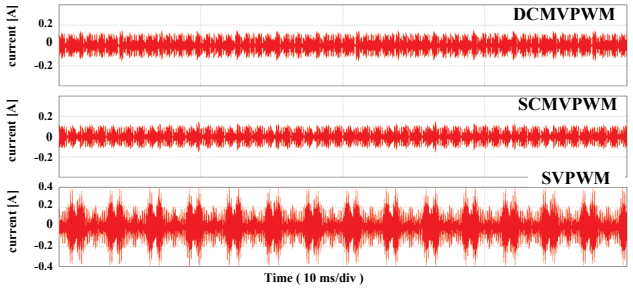

Fig. 19. The simulation waveforms when m_i=0.9 ; the leakage current $i_{leakage}$ in the case of DCMVPWM, SCMVPWM and SVPWM

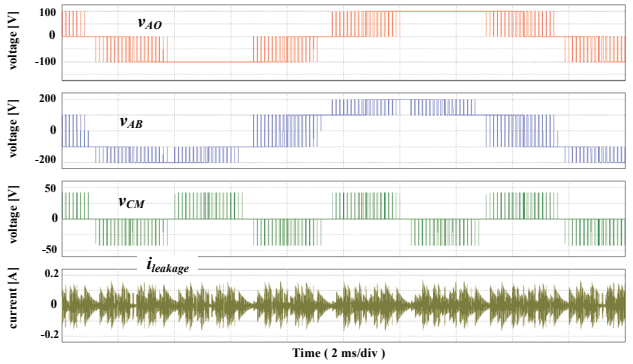

Fig. 20. The overmodulation simulation waveforms in the case of m_i=1.2 ; the A-phase output voltage, v_{AO}, the A- to B-phase line-to-line voltage, v_{AB}, the common mode voltage, v_{CM} and the leakage current $i_{leakage}$

Therefore, the leakage current has intermittent pattern synchronized with the CM voltage.

6. Experimental Results

6.1 The linear modulation operation

Fig. 21 shows the experimental waveforms with the same conditions that are given to obtain the simulation waveforms of Fig. 16. It is found that comparing the waveforms of Fig. 16 and Fig. 21 the proposed DCMVPWM is actually well operated to reduce the leakage current within the sufficiently low level.

Fig. 22 shows the experimental waveforms of the CM voltage and the leakage current in the case of m_i=0.9. As in simulation waveform of Fig. 17, it is observed that the CM voltage has pulse train pattern and the leakage current has sharp pulses during dead time.

In Fig. 23, the waveforms during the time slot is expanded and shown in the right side of Fig. 23 in order to the investigate the effect of dead time on the leakage

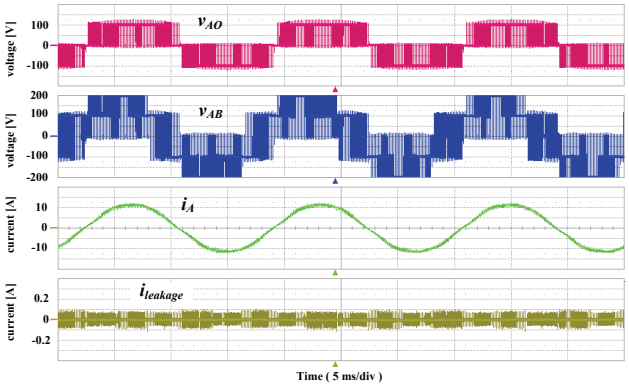

Fig. 21. The experimental waveforms when m_i=0.9; the A-phase output voltage, v_{AO}, the A-phase to B-phase line-to-line voltage, v_{AB}, the A-phase line current i_A and the leakage current $i_{leakage}$

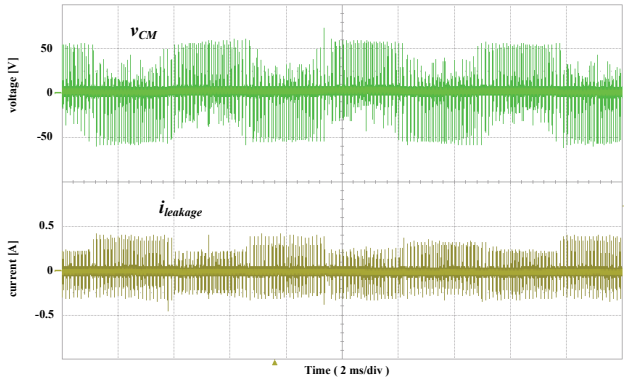

Fig. 22. The experimental waveforms when m_i=0.9 ; the common mode voltage, v_{CM} and the leakage current $i_{leakage}$

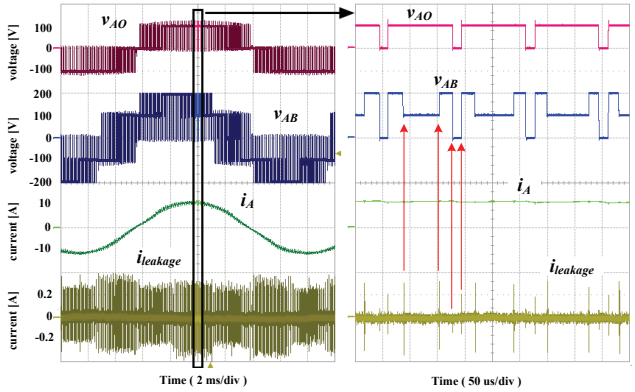

Fig. 23. The experimental waveforms when m_i=0.9; the waveforms during the time slot is expanded and shown in the right side

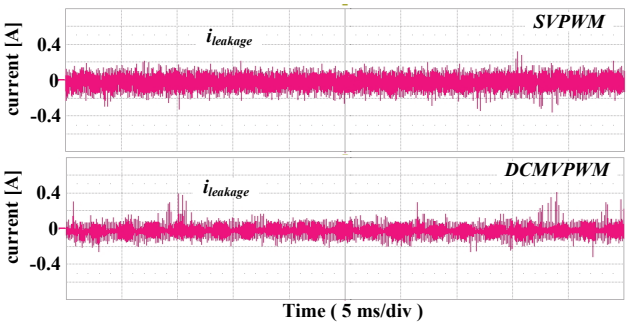

Fig. 24. The experimental waveforms of the leakage currents when m_i=0.9 in case of (top) SVPWM and (bottom) DCMVPWM

current. It should be noticed that as seen in the expanded figure of Fig. 23, the leakage current has very short pulses at every instants of switching state change. Because the dead time is limited to several micro-seconds, the leakage current due to the dead time effect is of high frequency nature.

Fig. 24 shows the experimental results of the leakage currents in case of SVPWM and DCMVPWM. Fig. 24 shows good agreement with the simulation results of Fig. 19. By using DCMVPWM, the leakage current is significantly reduced.

6.2 The overmodulation operation

Fig. 25 shows the experimental waveforms in the case of overmodulation of m_i=1.2. It is found that comparing the simulation and experimental waveforms of Fig. 20 and Fig. 25 the DCMVPWM is well operated to eliminate the leakage current even in overmodulation operation

The leakage current has some time intervals during which the leakage current is perfectly zero without any pulse train. This is because the CM voltage is constant during such halt time.

Fig. 26 shows the experimental waveforms when m_i=2.2, i.e., full maximized overmodulation. In the full over-

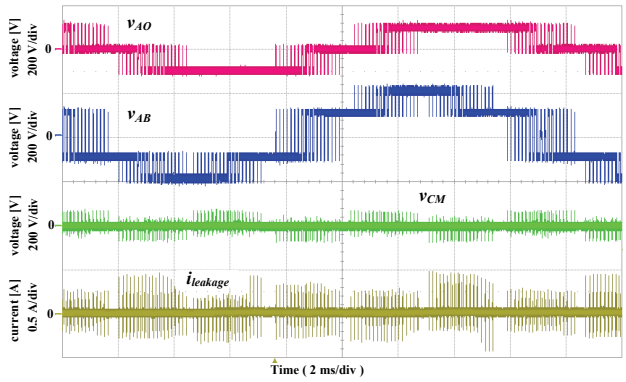

Fig. 25. The overmodulation experimental waveforms (m_i=1.2) ; the A-phase output voltage, v_{AO}, the A- to B-phase line-to-line voltage, v_{AB}, the common mode voltage, v_{CM} and the leakage current $i_{leakage}$

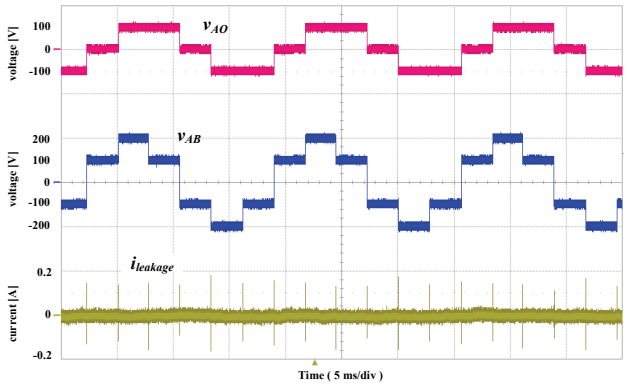

Fig. 26. The overmodulation experimental waveforms (m_i= 2.2) ; the A-phase output voltage, v_{AO}, the A- to B-phase line-to-line voltage, v_{AB}, and the leakage current $i_{leakage}$

modulation, the phase voltage becomes quasi-square waveform. Also the line to line voltage changes its voltage level every 60^o intervals. Thus the leakage current shows the short pulse every 60^o intervals. From Fig. 25 and Fig. 26, it is found that even in overmodulation, the DCMVPWM can eliminate the leakage current at sufficiently low level. If the dead time is shorten, the leakage current will be more decreased.

7. Conclusion

In this paper, the DCMVPWM for three-phase three-level inverter is investigated. The basic analytic equations such as the voltage gain and the switching frequency in overall operating ranges including overmodulation are discussed. Also, DCMVPWM is compared to SCMVPWM in order to find the advantages of the DCMVPWM. The switching frequency of DCMVPWM is much lower, about 33 % lower, than that of SCMVPWM while the DCMVPWM and SCMVPWM have the same constant

common mode voltage. Because the lower switching frequency means the smaller amount of the dead time, the DCMVPWM has the smaller output voltage losses than SCMVPWM. Finally, the leakage current reduction with minimized switching frequency in DCMVPWM is confirmed by carrying out simulation and the experiment. Because the dead time is inevitable, the leakage current cannot be completely eliminated even though the constant common mode voltage algorithm is employed

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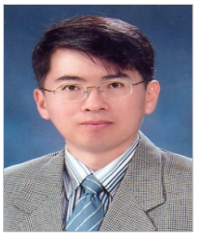

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